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EDN®

Show preview: Wescon/88

Designer's Guide to dc/dc converters—Part 3

Arbitrary-waveform generators

Resonant-mode control chips

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

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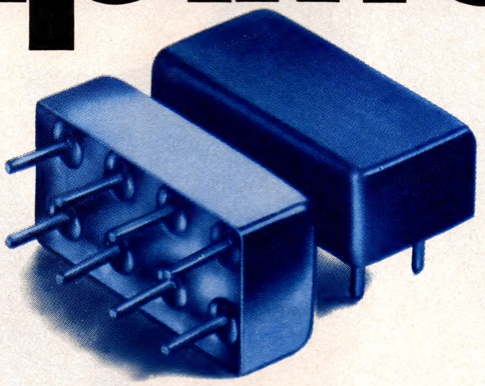
rugged plug-in amplifiers



0.5 to 1000MHz from $13.95 (10 to 24 qty)

Tough enough to meet full MIL-specs, capable of operating over a wide -55° to +100°C temperature range, in a rugged package...that's Mini-Circuits' new MAN-amplifier series. The MAN-amplifier's tiny package (only 0.4 by 0.8 by 0.25 in.) requires about the same pc board area as a TO-8 and can take tougher punishment with leads that won't break off. Models are unconditionally stable and available covering frequency ranges 0.5 to 500MHz and 0.5 to 1000MHz, and NF as low as 2.8dB.

Prices start at only $13.95, ***including*** screening, thermal shock -55°C to +100°C, fine and gross leak, and burn-in for 96 hours at 100°C under normal operating voltage and current.

Internally the MAN amplifiers consist of two stages, including coupling capacitors. A designer's delight, with all components self-contained. Just connect to a dc supply voltage and get up to 28dB gain with +9dBm output.

The new MAN-amplifier series...
another Mini-Circuits' price/performance breakthrough.

MODEL	FREQ. RANGE (MHz) f_L to f_u	GAIN dB min	GAIN dB flatness††	MAX. OUT/PWR† dBm	NF dB (typ)	DC PWR 12V, mA	PRICE $ ea. (10-24)
MAN-1	0.5-500	28	1.0	8	4.5	60	13.95
MAN-2	0.5-1000	19	1.5	7	6.0	85	15.95
MAN-1LN	0.5-500	28	1.0	8	2.8	60	15.95
◇MAN-1HLN	10-500	10	0.8	15	3.7	70	15.95
★MAN-1AD	5.500	16	0.5	6	7.2	85	24.95

††Midband 10f_L to $f_{u/2}$, ±0.5dB   †1dB Gain Compression   ◇Case Height 0.3 In.
Max input power (no damage) +15dBm; VSWR in/out 1.8:1 max.
★Active Directivity 18db

finding new ways...
setting higher standards

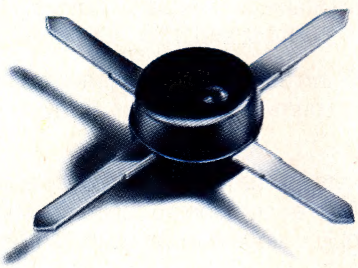
Mini-Circuits

A Division of Scientific Components Corporation
P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500
Fax (718) 332-4661 Domestic and International Telexes: 6852844 or 620156

CIRCLE NO 116

C118 REV. D

from 99¢



dc to 2000 MHz amplifier series

SPECIFICATIONS

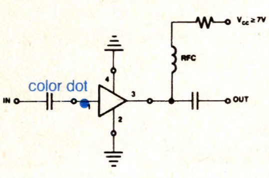
MODEL	FREQ. MHz	GAIN, dB 100 MHz	1000 MHz	2000 MHz	Min. (note)	• MAX. PWR. dBm	NF dB	PRICE $ Ea.	Qty.
MAR-1	DC-1000	18.5	15.5	—	13.0	0	5.0	0.99	(100)
MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8 □	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

NOTE: Minimum gain at highest frequency point and over full temperature range.
• 1dB Gain Compression
□ +4dBm 1 to 2 GHz

designers amplifier kit, DAK-2

5 of each model, total 35 amplifiers

only $59.95



Unbelievable, until now…tiny monolithic wide-band amplifiers for as low as 99 cents. These rugged 0.085 in.diam.,plastic-packaged units are 50ohm* input/output impedance, unconditionally stable regardless of load*, and easily cascadable. Models in the MAR-series offer up to 33 dB gain, 0 to +11dBm output, noise figure as low as 2.8dB, and up to DC-2000MHz bandwidth.

*MAR-8, Input/Output Impedance is not 50ohms, see data sheet. Stable for source/load impedance VSWR less than 3:1

Also, for your design convenience, Mini-Circuits offers chip coupling capacitors at 12 cents each.†

Size (mils)	Tolerance	Temperature Characteristic	Value
80 × 50	5%	NPO	10, 22, 47, 68, 100, 470, 680, 100 pf
80 × 50	10%	X7R	2200, 4700, 6800, 10,000 pf
120 × 60	10%	X7R	.022, .047. .068, .1μf

† Minimum Order 50 per Value

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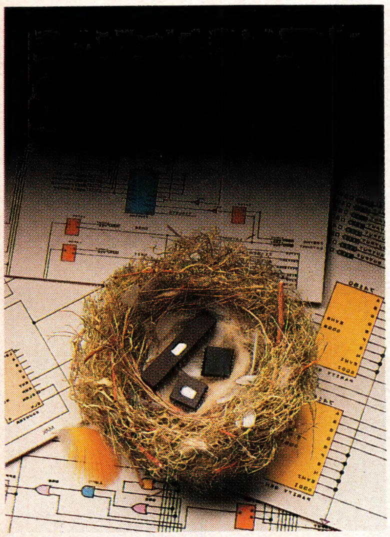
C113-Rev. D

EDN Magazine Edition

Volume 33, Number 23

November 10, 1988

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *The new PLD generation offers a dramatic increase in speed compared with devices introduced just one year ago. See pg 142. (Photo courtesy Altera Corp)*

SPECIAL REPORT

DESIGN FEATURES

Continued on page 7

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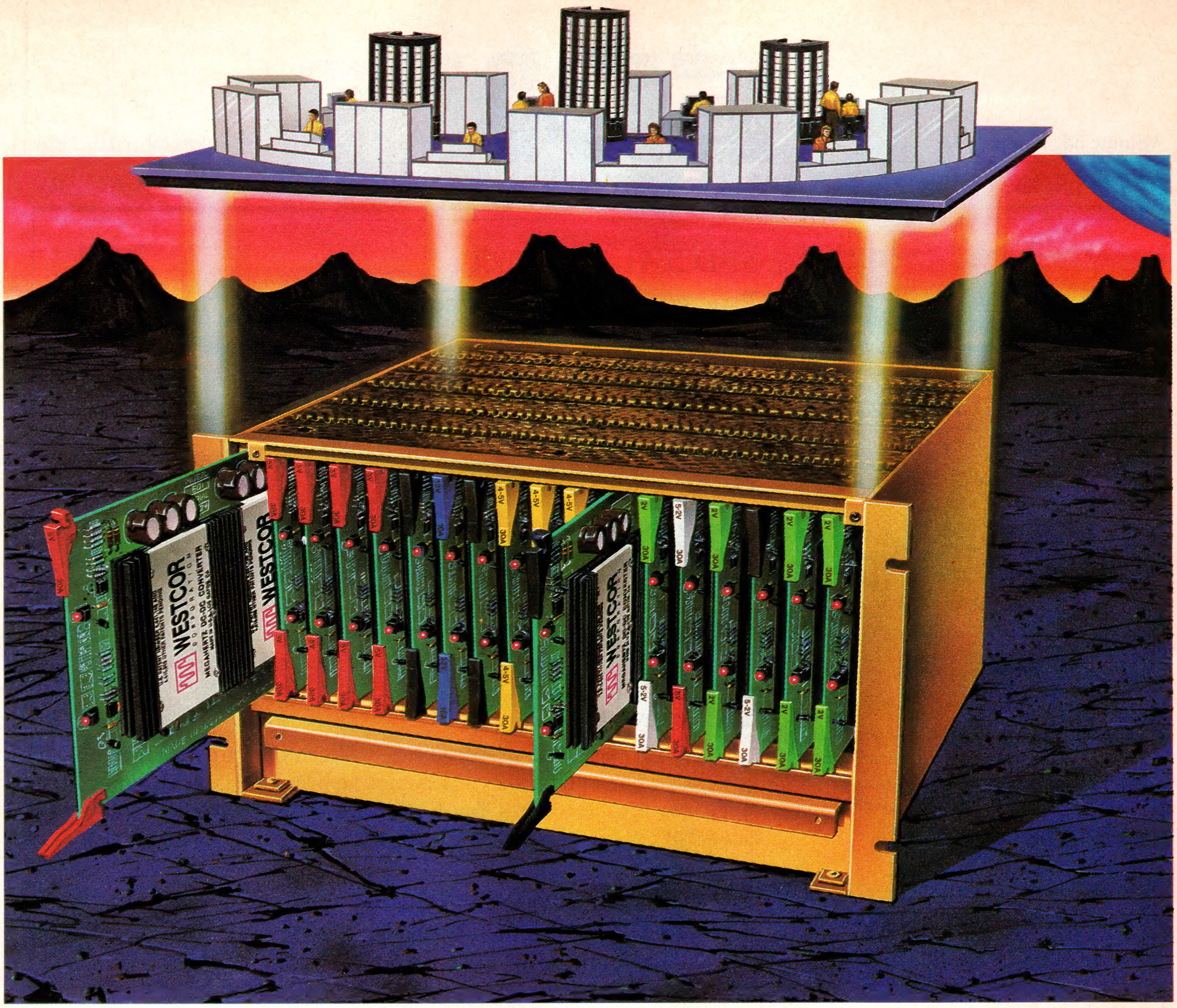
BPA ABP



A NEW WORLD OF HIGH POWER FLEXIBILITY

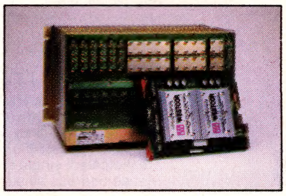
Westcor's PowerCage™ and PowerCards™ comprise a modular power supply system of galactic power (7200 watts max.), flexibility (36 outputs max.) and efficiency (80% typ.). More like an expandable computer mainframe in design and concept than a standard high power supply, the PowerCage offers space-age alternatives to users of outdated 5x8x11 inch box switchers.

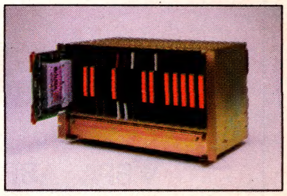
Measuring 19x10.5x11.25 inches deep the PowerCage fits into a standard NEMA rack and powers 18 slots for single or dual output PowerCards or dummy cards. PowerCage backplanes provide connections for easy configuration by the user.

Low profile (.8″) PowerCards supply single outputs from 2 to 75 VDC at up to 400 watts (outputs from 2 to 5 VDC limited to 60 amperes). Dual output cards source two isolated outputs each at half of the above ratings. Single output cards can be paralleled with current sharing to provide kilowatts via simple backplane configuration.

The nucleus of each PowerCage system is Westcor's patented 1 MHz, high power density, high reliability converter. Consider these benefits and features: 208 VAC 3 phase input; remote/local sense on all outputs; TTL power good signal and status LED's; designed to meet UL, CSA and VDE safety requirements; TTL inhibit; over-temperature, over-current, over-voltage protection; "hot" card insertion; full power at 50°C.

Future options include: DC input; IEEE-488 programmability; fault tolerant operation and battery backup. To discover a new world of high power flexibility, please contact us.





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CIRCLE NO 118

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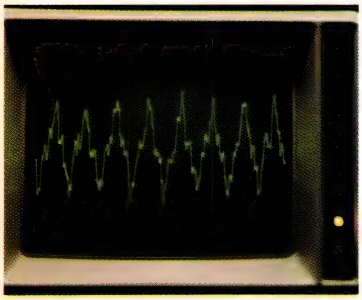
November 10, 1988



***Some vendors of arbitrary-waveform generators** believe their products will displace the more conventional fixed-function generators during the next decade (pg 65).*

TECHNOLOGY UPDATE

PRODUCT UPDATE

DESIGN IDEAS

Continued on page 9

Cahners Publishing Company, A Division of Reed Publishing USA □ Specialized Business Magazines for Building & Construction □ Manufacturing □ Foodservice & Lodging □ Electronics & Computers □ Interior Design □ Printing □ Publishing □ Industrial Research & Technology □ Health Care □ and Entertainment. Specialized Consumer Magazines: □ American Baby □ and Modern Bride.

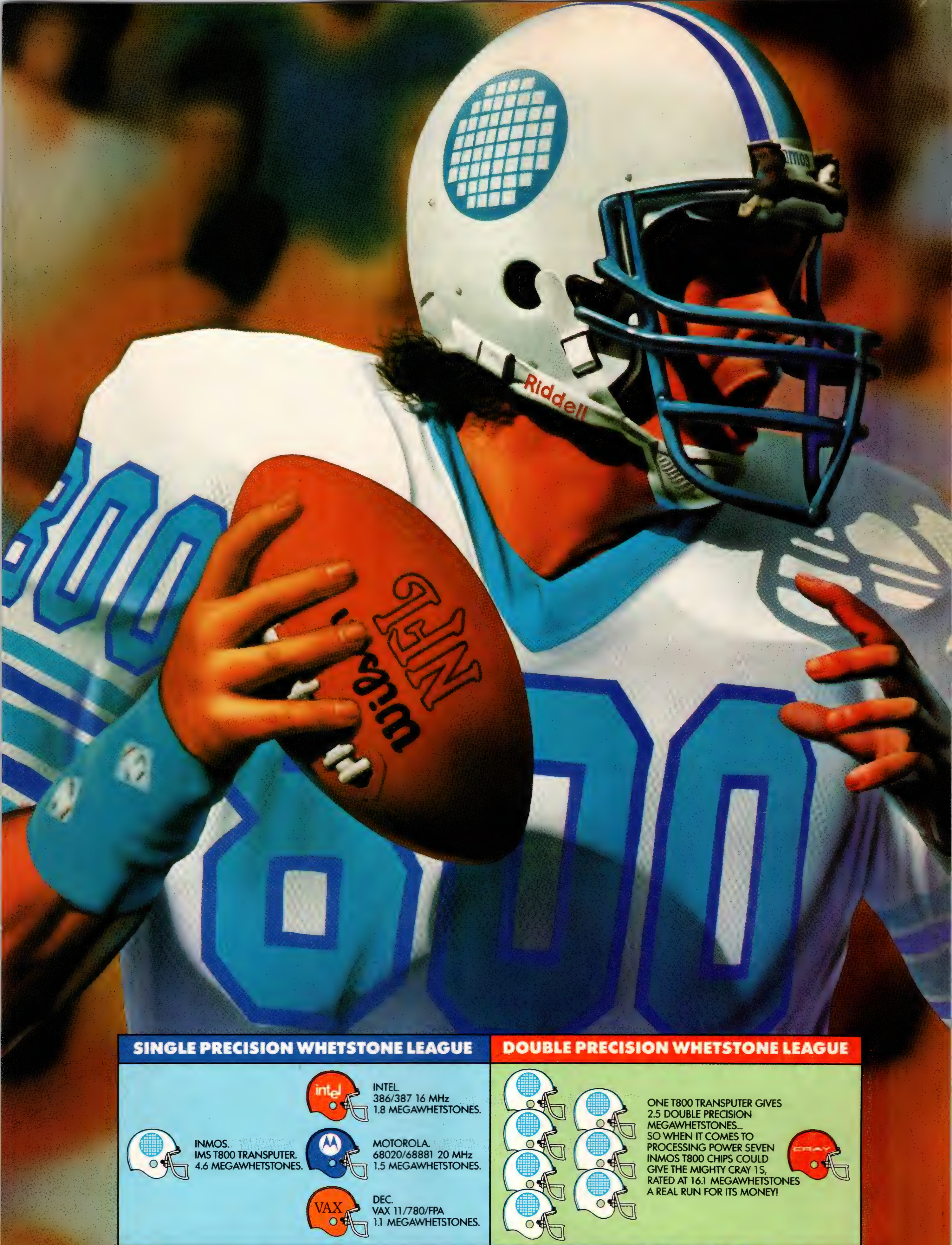
Continued from page 7

EDITORIAL 59

Analysts say that we'll be in a recession fairly soon, but we should approach all such forecasts cautiously.

NEW PRODUCTS

DEPARTMENTS



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SINGLE PRECISION WHETSTONE LEAGUE
INTEL.
386/387 16 MHz
1.8 MEGAWHETSTONES.
INMOS.
IMS T800 TRANSPUTER.
4.6 MEGAWHETSTONES.
MOTOROLA.
68020/68881 20 MHz
1.5 MEGAWHETSTONES.
DEC.
VAX 11/780/FPA
1.1 MEGAWHETSTONES.
DOUBLE PRECISION WHETSTONE LEAGUE
ONE T800 TRANSPUTER GIVES
2.5 DOUBLE PRECISION
MEGAWHETSTONES...
SO WHEN IT COMES TO
PROCESSING POWER SEVEN
INMOS T800 CHIPS COULD
GIVE THE MIGHTY CRAY 1S,
RATED AT 16.1 MEGAWHETSTONES
A REAL RUN FOR ITS MONEY!

MORE MULTIPROCESSOR MUSCLE. MORE RAW PERFORMANCE.

When you're out in the trenches fighting it out with ordinary microprocessors, running out of muscle is all too easy. That's why you should look to the new T800 Transputer from INMOS.

The T800 is the fastest 32-bit, single chip, floating-point microprocessor available today. A quick glance at its statistics will show why nothing else is in its league...

32-bit enhanced RISC processor...64-bit on-chip IEEE floating-point processor...4K Bytes on-chip 50ns static RAM...Four 20 MBits/sec interprocessor communication links...Eight independent DMA engines. All on a single chip capable of sustained 1.5 MFLOPS...and 4.6M Whetstones!

And, if that's not enough raw power, the T800's links allow multiprocessor systems to be constructed quickly and easily – giving you 6 MFLOPS with four T800's...30 MFLOPS with 20...150 MFLOPS with 100...In fact, there's no limit to the number of Transputers you can use!

Programming Transputers couldn't be easier, with compilers for C, Fortran and Pascal, and the world's first concurrent programming language OCCAM.

Want to turbocharge your current system? No problem. Our exclusive Link Adaptor IC's allow Transputers to be connected to other microprocessors or peripherals.

Other team members include the pin compatible T414 Transputer, offering lower cost, 10 MIP performance and 0.75M Whetstones. Lined-up to provide all the I/O processing you need, the T212 16-bit Transputer is the ideal high performance controller and the M212 Disk Processor combines disk controller hardware and a Transputer on a single chip, supporting both Winchester and floppy disks. And the C004 Link Switch makes the design of software reconfigurable multiprocessor systems as easy as kicking an extra point.

Whatever field you're in – from real-time distributed systems to high-performance graphics, from fault-tolerant systems to robotics, Transputer technology can give you scalable performance at a cost you can afford.

Transputers are manufactured using an advanced 1.5 micron CMOS process which keeps the power consumption under one watt. So your system stays cool while under fire.

Transputers to MIL-STD 883C will be available in the first half of 1988.

If this all sounds like your kind of game, put the ball in play by contacting your local INMOS sales office today. And get ready to score.

DESCRIPTION			PERFORMANCE		AVAILABILITY		PACKAGE
Part No.	Word Length	Clock MHz	Integer Drystones	Floating Point Whetstones	Commercial	Military	
IMS T800-20	32-Bit	20	9500	4.6 Million	Now	Q2 88	84 PGA
IMS T414-20	32-Bit	20	9500	0.75 Million	Now	Q2 88	84 PGA
IMS T212-17	16-Bit	17	8000	–	Now	Q2 88	68 PGA
IMS T212-20	16-Bit	20	9500	–	Now	Q2 88	68 PGA
IMS M212-17	16-Bit	17	8000	–	Now	–	68 PGA

NETWORK SUPPORT PRODUCTS			AVAILABILITY		PACKAGE
Part No.	Description	Communication Speed	Commercial	Military	
IMS C004	Software configurable 32 way link switch	10 + 20 MBits/sec	Now	Q2 88	84 PGA
IMS C011	Link to system bus	10 + 20 MBits/sec	Now	–	24 Pin DIP
IMS C012	Link to system bus	10 + 20 MBits/Sec	Now	Q2 88	24 Pin DIP

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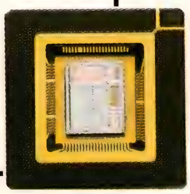

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SIEMENS

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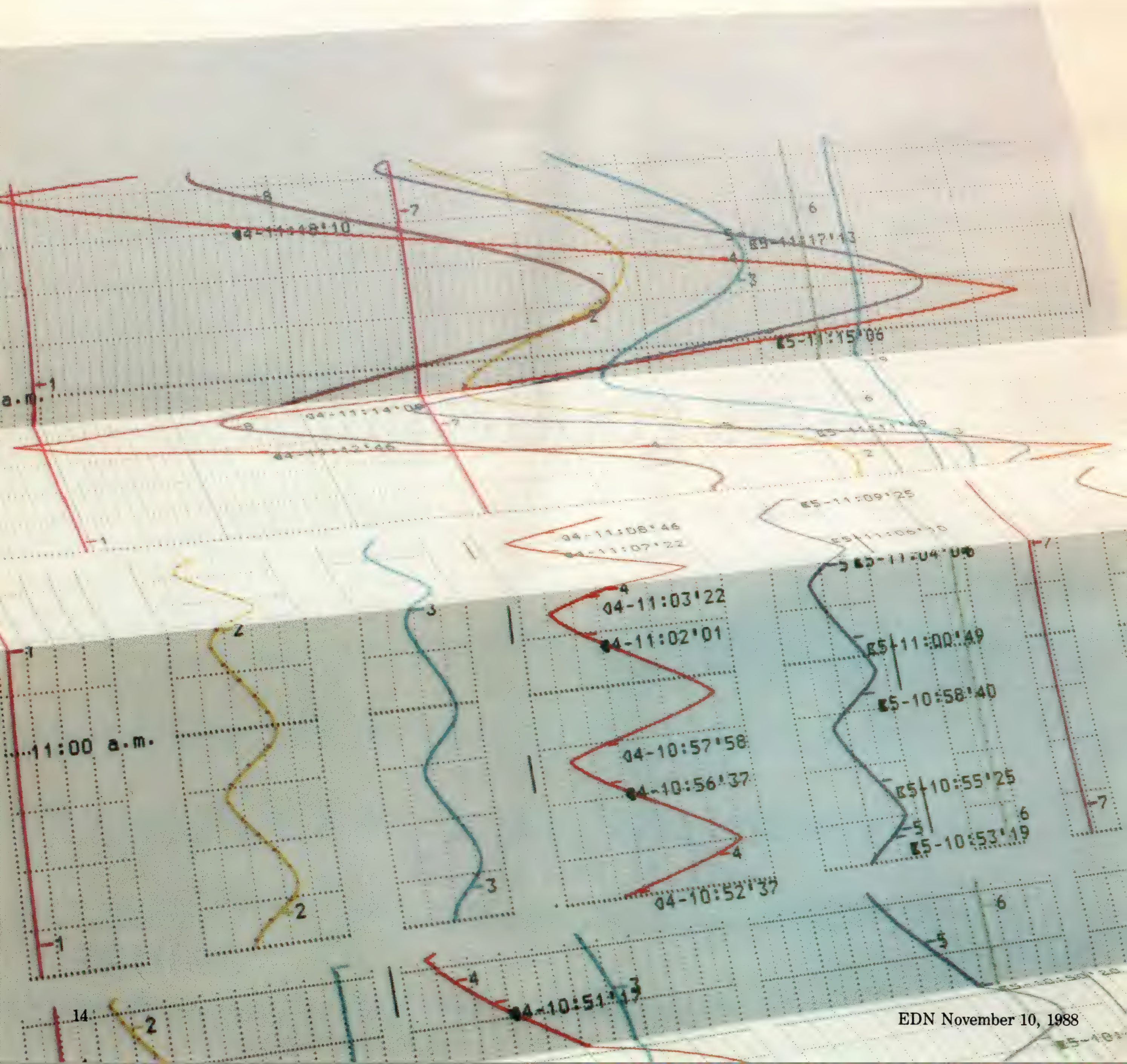
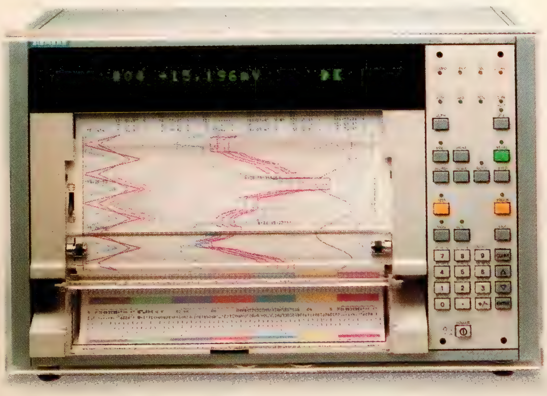


...Then move up to the new MULTIREG C1732 hybrid recorder.



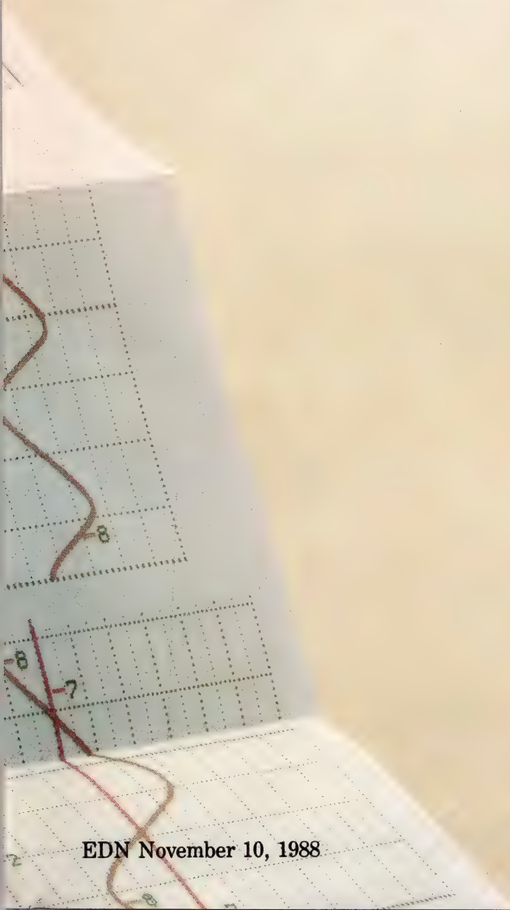
Once you needed expensive add-on devices to record periodic quantities captured by your measurement system. Not any longer...because our new MULTIREG® C1732 hybrid recorder registers direct current, D/C voltage, temperature, A/C voltage, and alternating current – all by itself.

With MULTIREG C1732, the move to unique recording convenience begins with your selection of up to 45 separate measurement areas. The system does the rest...by sampling some 32 measurement channels in a mere 1.5 s and plotting the results in 7 different colours. Including full graph annotation for easy interpretation.

But that's not all. MULTIREG also couples functions mathematically...and automatically...and displays the values in graphic form. Giving you a new perspective on complex relationships.

All this with just one hybrid recorder. Hard to believe, but it's true.
And our new MULTIREG C1732 is even available as an individual unit (PIEZOGRAPH 2).

MULTIREG C1732.
Measurement convenience that measures up.



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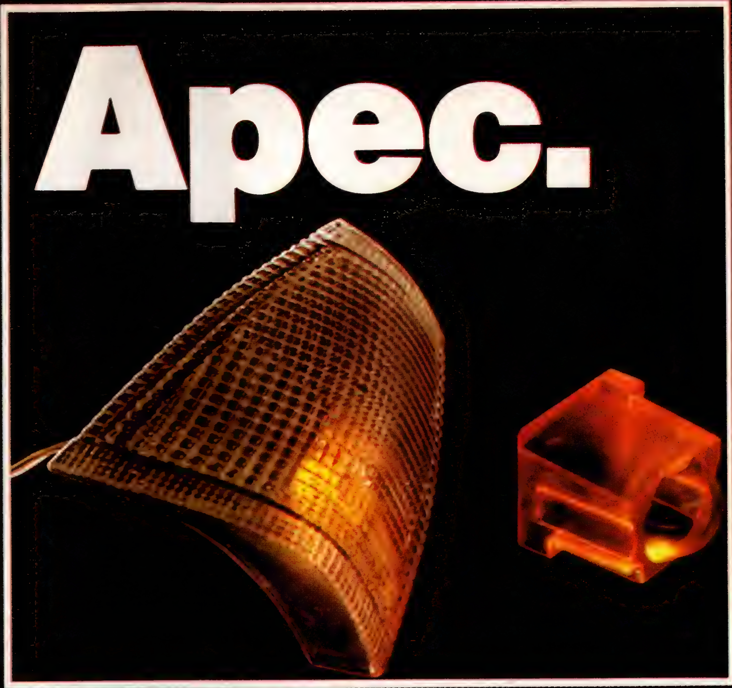
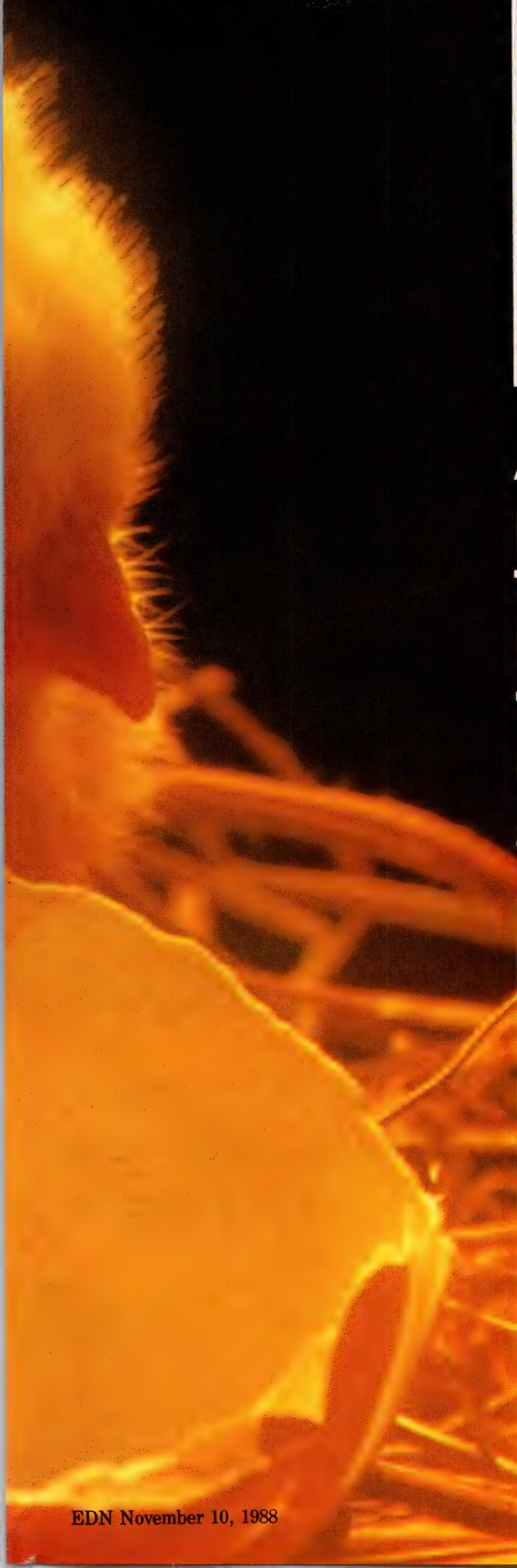
hday:

Apec.





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Please do not hesitate to contact us if you want assistance.

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☐ I am interested in speaking to your specialist.

If you need immediate advice please call Mr. Arnolds – Telephone: 02 14-30-34-25.

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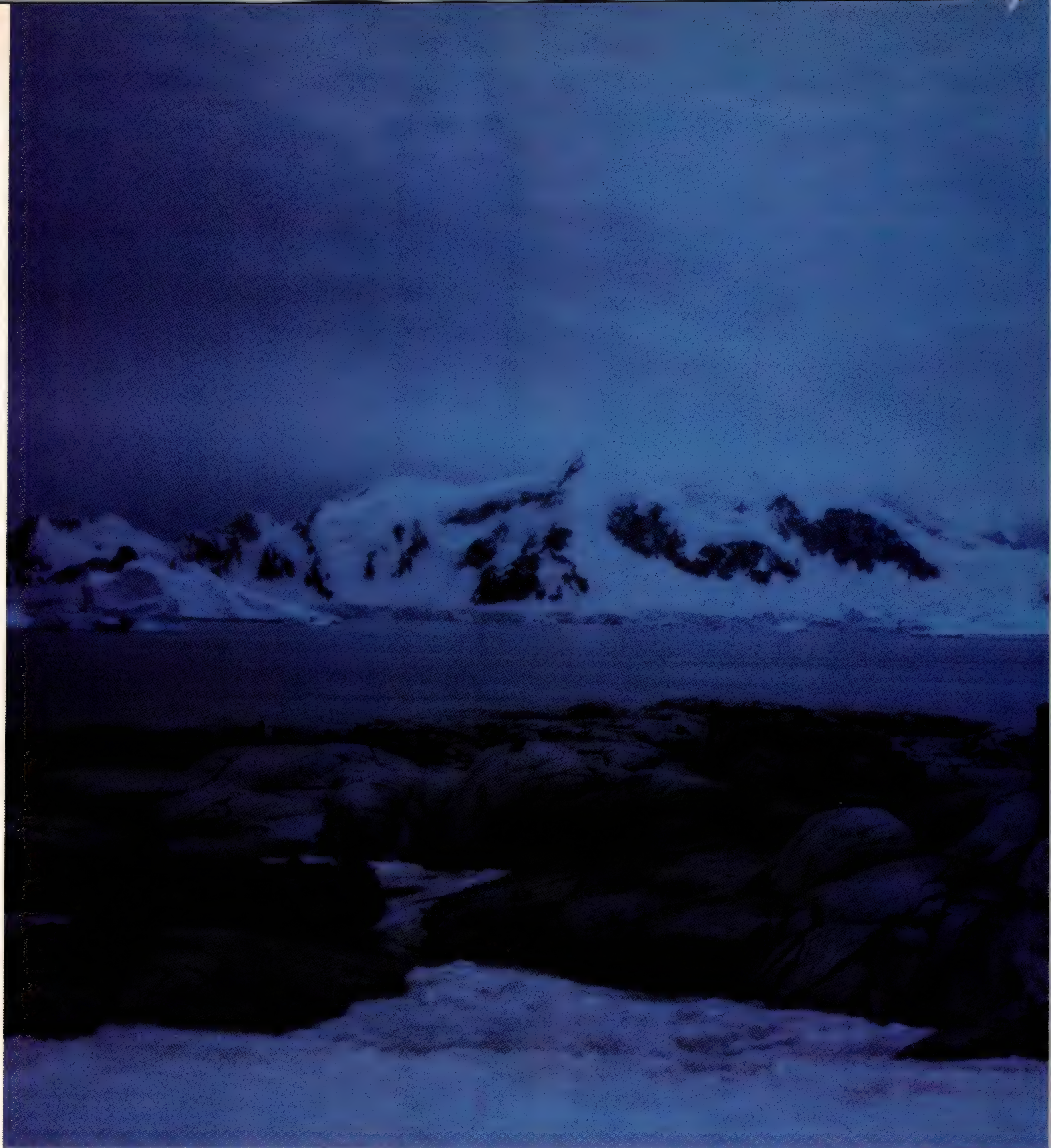

Even though we're the strongest group of companies in the electronics industry, there may still be a few people who don't know we exist.

CIRCLE NO 126

These High-Rel SRAMs offer you all these benefits:

- 100 ns access time at 25°C
- Low standby current: 1 mA typical
- Full Mil temperature range
- 32Kx8 organization
- 28 Terminal DIL Package
- Screened to Mil-Std-883 Class B.* So they're perfect for use in a wide range of military systems. And, as you'd expect from the leaders in High-Rel CMOS, we have a full line of SRAMs, including 64K (8Kx8) and 16K (2Kx8).

Tops in Rad-Hard RAMs, too.

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Our Rad Hard 16Kx1 CMOS/SOS RAM has an access time of 125 ns at 25°C and is available for immediate delivery to Class S type specifications.

CMOS/SOS is the ideal technology for rad-hard applications because:

- It's latch-up free under transient radiation
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So whatever your needs in SRAMs, aim high, and call the Top Guns today. For additional information, call toll-free 800-443-7364, extension 20. Or contact your local GE Solid State sales office or distributor.

*Rev. C, Paragraph 1.2.2

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NEWS BREAKS

EDITED BY JOANNE CLAY

DATA-ACQUISITION SOFTWARE GETS A BOOST FROM OS/2

Laboratory Technologies Corp's (Wilmington, MA, (508) 657-5400) $1500 Labtech Notebook data-acquisition program can now acquire data from multiple instruments simultaneously by running under the Microsoft (Redmond, WA) OS/2 multitasking operating system for IBM PCs and compatible computers. You can run as many as 11 copies of Labtech Notebook on one computer; each package can acquire data from a different instrument and store the data in separate disk files. In addition, you can run other application programs under OS/2 while Labtech Notebook is acquiring and storing data.

According to the company, several of OS/2's features made the transition to a multitasking environment easy. The firm cited such features as OS/2's true multitasking environment; a pre-emptive, priority-driven scheduler that supports time-critical processes; interrupt-driven I/O; protected memory and a 16M-byte physical address space; and direct access to high-bandwidth peripheral devices for application programs.—Steven H Leibson

REAL-TIME DSP OPERATING SYSTEM FOR THE TMS320C30

Spectron Microsystems (Santa Barbara, CA, (805) 967-0503) now offers a real-time operating system for the Texas Instruments TMS320C30 general-purpose DSP chip. The operating system, called SPOX, has a complete set of functions for controlling real-time software and can switch tasks in 10 μsec. Memory-management, stream I/O, and DSP math functions are also included. The real-time kernel, memory-management, and stream I/O code take up less than 4k words and can fit within the on-chip ROM of the TMS320C30.

SPOX also provides a set of development tools that make up a virtual DSP machine. These tools allow you to configure the system to simulate your target system before any hardware is built. You can test your algorithms and obtain feedback about the execution times of the routines you expect to use. You do the first stages of debugging on the host system, then you move to the target system for final testing. SPOX will be available in January 1989. It will come bundled with TI's XDS-1000 development system ($16,000) and will run on the IBM PC. It will be available for Sun and VAX systems by mid-1989.—David Shear

PC-BOARD DESIGN SOFTWARE HAS POP-UP MENUS, DIALOG BOXES

The Series II versions of Tango-PCB and Tango-Route pc-board design software from Accel Technologies Inc (San Diego, CA, (619) 695-2000) employ a user interface based on pop-up menus and dialog boxes and offer context-sensitive help information. The Tango-PCB pc-board-layout package supports six signal layers, power and ground layers, keep-out and board-outline layers, a connections layer, a title layer, drill-drawing layers, top and bottom silkscreen layers, an assembly layer, and solder-mask layers. The Tango-Route autorouter employs multipass, maze, and proprietary routing strategies to handle 4-layer boards. You can employ the Series II software to design pc boards with a maximum size of 32×32 in. The IBM PC-compatible software can drive Hercules, CGA, EGA, and VGA monitors and most popular plotters. Available now, the Tango-PCB package costs $595 and the Tango-Route autorouter costs $495. You can purchase the two packages together for $995.—Maury Wright

1.5-μm, TRIPLE-TECHNOLOGY LIBRARY MAKES ITS DEBUT

Sierra Semiconductor (San Jose, CA, (408) 263-9300) has introduced a 1.5-μm process that permits you to combine analog, digital, and EEPROM circuitry on one IC. The library contains 23 analog cells and 245 digital cells, and the process supports the design of 65-MHz phase-locked loops, 100-MHz analog comparators, 10-MHz resistor-string DACs, and 100-MHz video DACs. The manufacturer claims the process will allow for loaded gate delays of 1 nsec and system performance as high as 90 MHz at 100,000-gate densities. The company plans to add EEPROM cells and the COP800 core microprocessor to the library by January 1989.—Michael C Markowitz

80386 PC-DOS-COMPATIBLE COMPUTER FOR VXI BUS

The EPC-2 VXI Bus computer from Radix Microsystems (Beaverton, OR, (503) 690-1229) is a PC-DOS computer with a 1.4M-byte floppy-disk drive and a 40M-byte hard-disk system. It includes an 800 × 600-pixel, 16-color graphics controller that supports VGA, EGA, CGA, and monochrome boards. This embedded PC is designed to meet the more stringent environmental requirements of ATE and instrumentation systems, while still allowing you to develop applications in a PC software environment. The computer is more than just an embedded PC—it provides full VXI Bus slot-0 control and VME Bus slot-1 control. To help you develop your own VXI Bus instrumentation applications, the computer comes with EPConnect version 2.0 software tools.

With this computer, you can achieve data-transfer rates over the VXI Bus as high as 5M bytes/sec, which is significantly higher than the data-transfer rates you can obtain with IEEE-488 instrument control. The higher data-transfer rate can reduce test times dramatically in applications that limit throughput. The system provides a complete IEEE-488 interface, which includes a talker, a listener, and a controller. The computer module is housed in a dual-wide (2.4-in.) C-size VXI Bus module. The module is fully shielded (on six sides) and meets all VXI Bus EMI specifications, including close and far-field EMI emissions specs. It will be available by January 1, 1989, for $9550.—Doug Conner

INTEGRAL ZENER DIODE PROTECTS DARLINGTON POWER TRANSISTOR

A planar zener diode protects Motorola's (Phoenix, AZ; contact Jim Nappe at (602) 244-4912) MJE5420Z Darlington power transistor from voltage spikes exceeding 24V. The device, which costs $0.95 (1000), is therefore ideal for driving inductive loads. The transistor incorporates thermal-compensation circuitry to reduce the zener diode's thermal coefficient from 100 mV/°C to 6 mV/°C.
—Steven H Leibson

FAX MODEM IC OPERATES AT 9600 BPS

The R96MFX Monofax modem IC from Rockwell International (Newport Beach, CA, (714) 833-4700) operates at 9600 bps and comes in a 64-pin, quad-in-line plastic package that's pin-compatible with the company's existing 2400- and 4800-bps Monofax products. The hybrid device operates at 9600, 7200, 4800, 2400, and 300 bps; is compatible with the Group 2 and Group 3 facsimile standards; and features both a parallel-bus port and an asynchronous serial port for connection to a host processor. It sells for $75 (1000).—Steven H Leibson

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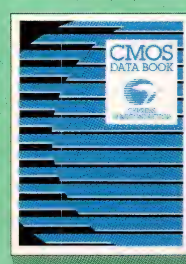

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SINGLE CHIP INTERFACES TO ISDN-STYLE VOICE/DATA LAN

Instead of introducing a standard S-interface device to connect terminal equipment to ISDNs, Philips' Components Div (Eindhoven, The Netherlands, TLX 51573; in the US: Signetics Corp, Sunnyvale, CA, (408) 991-2000) has introduced an interface chip, the PCB2310, which interfaces terminals to the company's proprietary IST-bus. Because the IST-bus accommodates as many as 31 voice or data terminals and allows terminal-to-terminal communication and terminal-to-ISDN communication via a simple gateway, the company believes that the IST-bus has significant advantages over the ISDN S-bus. (The S-bus only allows the connection of eight terminals and does not allow terminal-to-terminal communication other than via a PABX or central-office exchange.)

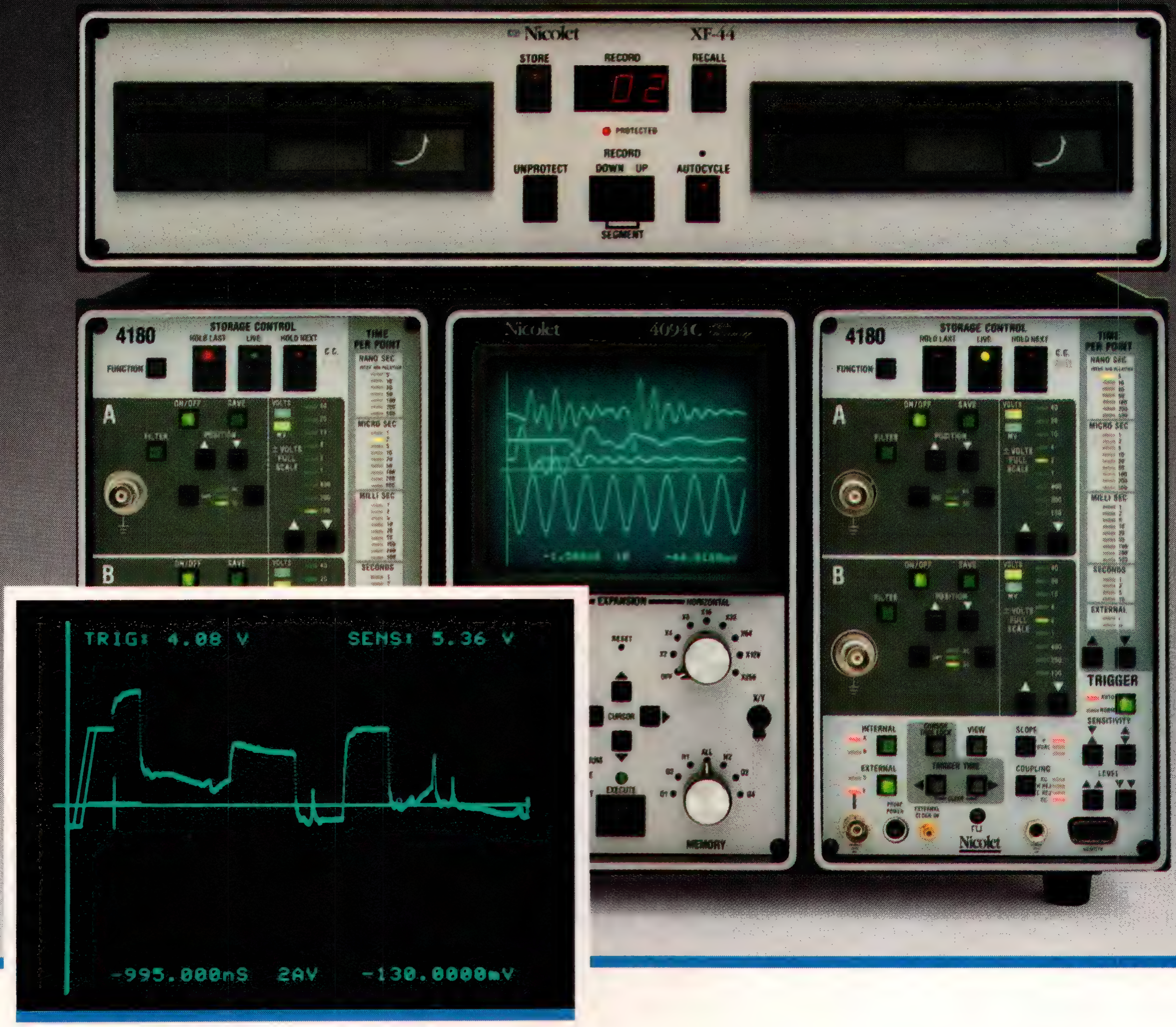
The IST-bus uses 2-wire twisted-pair cabling and operates with eight 64k-bps, circuit-switched, time-division-multiplexed B-channels and one 64k-bps packet-switched BD-channel that carries signaling information or data messages. In addition to its IST-bus interface, the PCB2310 has interfaces for a subscriber-line data link, a 2M-bps terminal highway, and an 8-bit microcontroller. Samples of the PCB2310 are available now. By 1992, the part is expected to sell for around $20 in high volume.—Peter Harold

SYMMETRICAL MULTIPROCESSOR TARGETS MISSION-CRITICAL USES

The Model 20 and Model 60 computers from BiiN (Hillsboro, OR, (503) 696-4800) implement a symmetrical multiprocessor architecture that incorporates fault redundancy and fine-grained software security in the computers' hardware. Both computers run the BiiN/OS operating system, which has an interface that conforms to both the IEEE's POSIX and AT&T's SVID standards. A fully configured Model 20/10 computer with one processor, 16M bytes of memory, a 180M-byte disk drive, a 150M-byte tape drive, and an Ethernet interface costs $55,000. A fully configured Model 60/20 computer with two processors, 128M bytes of memory, two 320M-byte disk drives, a 150M-byte tape drive, and an Ethernet interface costs $425,500. You can install as many as two processors in the Model 20 and eight processors in the Model 60.

With eight processors, the Model 60 allows you to dynamically select from one of three fault-tolerant operating levels: standard, fault-checking, and continuous. The standard mode allows each processor to run independently for maximum speed and relies on internal processor checks and error-corrected memory transfers to catch any errors that might occur. The fault-checking mode pairs processors so that all operations are performed in a dual-redundant manner. In this mode, a nonrecoverable error stops program execution. The continuous operating mode couples dual-redundant processor pairs, so a nonrecoverable error in this mode simply causes the computer to switch to the alternate pair without stopping program execution. BiiN is a joint venture of Intel Corp (Santa Clara, CA) and Siemens AG (Munich, West Germany)—Steven H Leibson

Flexible Triggering An Issue?



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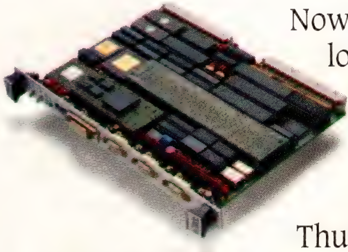

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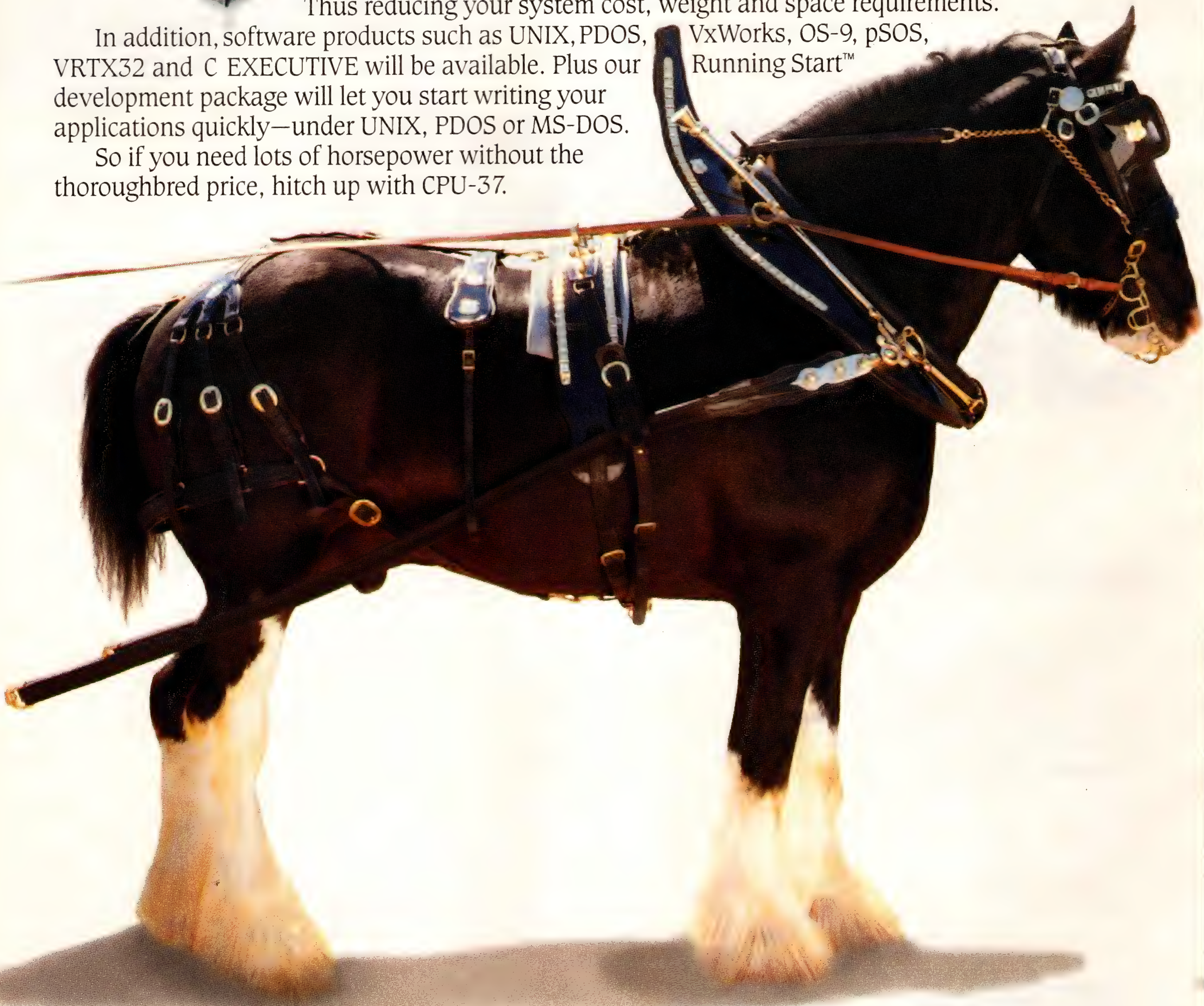

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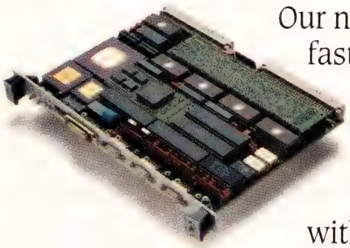

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SIGNALS & NOISE

IEEE lacks inspired leadership

So the IEEE bigwigs have taken some carefully worded potshots (Signals & Noise, EDN, July 7, 1988, pg 31) at Jon Titus's editorial "The IEEE faces extinction" (EDN, February 4, 1988, pg 53). Executive vice-presidential candidate Robert S Duggan Jr offers growth stats and a curt dismissal of those "noisy whiners" who stir up the mud. President Russell C Drew would have you believe that the IEEE now embraces the will of the majority via approval voting, and that it has championed engineers' professional needs for decades.

However, the self-serving umbrage from the IEEE doesn't detract from the editorial's critical assessment of the Institute's hierarchy. Who ever heard of approval voting before the board of directors made it official policy? Drew's claim that "the voting method for member election of officers and directors of the IEEE has *not* previously been specified in *either the constitution or the bylaws* . . . " is irrelevant. This is an important issue that affects every member directly, not some cosmetic change in the Policies and Procedures Manual. The paternal "Father knows best" attitude of Drew's letter is a personal insult to all IEEE members not privileged to sit on the board of directors.

It is true that the IEEE has been involved in professional activities, primarily through its US Activities Board, for many years. But the inspiration for these activities is directly traceable to the IEEE's dissident element, not to its traditional leadership. Faced with membership unrest about professional issues, the IEEE hierarchy looks upon token involvement as an end in itself. Drew states: "Pension-reform legislation has been an active target of the IEEE for over a decade." Ten years of effort, and most engineers still lose all their pension benefits every time they change jobs—it's not exactly a victory for the working engineer. The IRA bill of which the IEEE is so proud was really a tax break for all workers without pension plans, not just engineers. The legislation went nowhere until a broad coalition of support developed outside of—and in spite of—the IEEE's efforts.

The real tragedy where professional issues are concerned, inside and outside the IEEE, is the lack of inspired leadership. No person or group has the mandate to set realistic goals, organize the volunteers, and make the political alliances needed to pass legislation. Irwin Feerst, who has done more than most to focus attention on engineers' problems and the IEEE's shortcomings, has only followers and enemies—no peers. His attacks on other leaders involved with professional issues are legend. Engineers have too long seen their legitimate concerns either ignored or used as an incendiary device for personal vendettas. When will the political sophistication develop that demands something better?

Don Mennie
Technical Editing Consultant
Mendham, NJ

An apple for Feerst

The controversy over Irwin Feerst and his Committee of Concerned EEs has finally come to the point where he can make a difference. Hopefully, Irwin Feerst will win the position he has sought, and deserved, for so many years.

The professor who voiced his opinion in the Signals & Noise column of the June 9, 1988, issue (EDN, pg 32) seems grossly out of line. He is obviously unaware of the fact that Irwin Feerst has taught graduate-level courses at Adelphi University, courses that came highly recommended by previous students.

As one of his former students, I

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can say without reservation: Irwin Feerst can teach. There have been only a handful of professors I have had that could teach. Every professor I ever had was a very knowledgeable man; some were even brilliant, but they had one major fault—they couldn't teach. It is my opinion that before a professor is allowed to teach at any level, he or she should be required to take courses on how to teach, and then do a year of residency under the supervision of a certified teacher. Perhaps then professors would be better able to convey the facts they intend to present to their students.

With respect to the inference that foreign engineers are bad for our industry, my only comment is that unless your background is American Indian, you are of foreign ancestry.

On the subject of training foreign engineers, my feeling is about the same as that expressed by a sports columnist writing about the Soviet interest in baseball. Both Americans and Cubans will probably be training the Russians in the game, but the Cuban philosophy is to teach them enough to beat the US but not enough to beat the Cubans. Perhaps we engineers should adopt the same smart philosophy—train engineers to beat the competition, but not enough to beat us, then let them go their chosen way. This way, all are happy, and none should complain. It makes sense to me, anyway.

I quit the IEEE many years ago when it became obvious that the organization did not represent the working engineer, the true engineer. It still doesn't, but perhaps there is a light at the end of the proverbial tunnel. If so, I may rejoin.

David A Meyer
Professional Engineer
Verndale, MN

"Of what use is a baby?"

I see a problem with the Design Idea "Flip-flop multiplies input frequency" (EDN, July 7, 1988, pg 279). The 3-stage multiplier circuit shown simply produces a burst of very narrow pulses on every transition of the input signal. What good is that?

Instead of calling it a frequency multiplier, perhaps you should call the circuit a contact-bounce simulator.

Andrew Dart
Andy's Bureau of Standards
Duncanville, TX

Off-the-shelf idea

I'd like to offer your readers a simpler, less costly, and more versatile alternative to Irwin Cohen's Design Idea "Circuit screens narrow pulse widths" (EDN, May 26, 1988, pg 209). To wit, Motorola's MC14490 Hex Contact Bounce Eliminator

provides six channels of narrow-pulse discrimination in a 16-pin CMOS circuit whose filtering can be controlled by an RC pair or by an external oscillator.

Although it's intended for switch-debounce applications, this circuit can be used in a variety of digital-filtering applications. Any number of the six channels can be used independently or can be cascaded to expand the resolution of the pulse-width discrimination.

Ellery W Potash
VP Engineering
Intra Computer Inc
New York, NY

Errata

In the Special Report "PC-resident analog-I/O cards" (EDN, September 15, 1988, pg 150), the $3208 price for Interactive Microware's ADALAB-PC interface board is in error. In fact, the ADALAB-PC board costs $655. The $3208 price applies to a complete data-acquisition system called ALAB-PC-SYS2. This system includes the ADALAB-PC board, Adapt software, an IBM PS/2 Model 30 computer with a monochrome monitor, a dot-matrix printer, and curve-fitter and scientific software. EDN apologizes for any inconvenience this error may have caused.

The article also contains an incorrect address for The Markenrich Corp (pg 157). The correct address is:

The Markenrich Corp
1812 Flower Ave
Duarte, CA 91010
(818) 359-5223

WRITE IN

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The pay-off is a life test failure rate less than 50 FIT with more than 400,000 device hours. And a soft error rate less than 100 FIT. What's more, latch-up immunity is more than 200 mA. And ESD protection is greater than 2,000 volts.

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Because of its stable memory cell, the 256-kbit SRAM tolerates skewed address signals without disturbed bits.

Customers—like Cray Research—also report low system noise and cleaner, quieter, faster signals. This high noise immunity is due to on-chip decoupling and minimal di/dt.

And because of the chip's 10-ns write pulse with zero setup and hold, it's easy to design-in in a 15-ns write cycle.

Our ECL SRAMs are input/output compatible with existing 10K and 100K ECL parts. Industry-standard pin-outs enable multiple sourcing.

AND YOU GET MORE MODELS TO CHOOSE FROM

In addition to our high-performance SRAMs, we're working on a family of specialty ECL RAMs and ECL RAMs in advanced packaging.

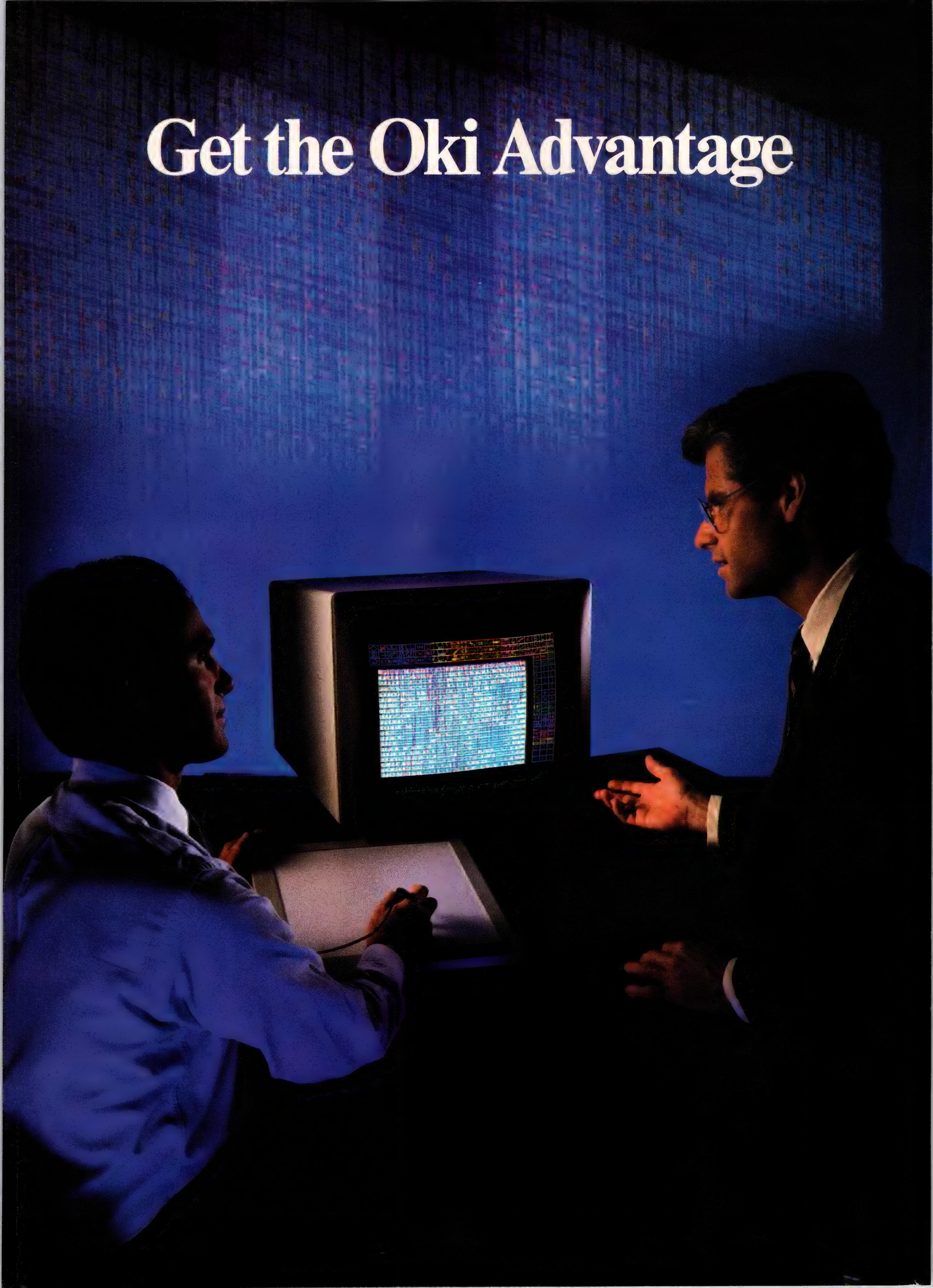
We also offer you the broadest array of memory product families of any domestic supplier—including TTL SRAMs, EPROMs, EEPROMs, and fuse-link PROMs.

This breadth of product line helps you minimize the number of suppliers you use. While National's large-volume manufacturing ensures availability.

CALL FOR OUR NEW BROCHURE

For more information on our new 256-kbit SRAM—or any other memory product—ask for a copy of our new memories brochure. Call us toll-free at (800) 252-4488, ext. 735.

National Semiconductor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An ASIC project is a major commitment of your budget and man hours. Give yourself the advantage of working with a powerful partner. Oki Semiconductor has the experience, resources, and commitment you can rely on to help ensure your ASIC VLSI success.

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Oki Semiconductor has complete ASIC capabilities, from full custom to semicustom ICs. Our three families of advanced CMOS ASIC products have been designed to meet all of today's high-density, high-speed device requirements.

▶ *Sea-of-gates:*
new sea-of-gates channelless arrays provide an available 100,000 gates and a minimum 40,000 gate circuit logic density of 640 picoseconds.

▶ *Channelled array:*
new 1.2 μ channelled arrays provide speed in the subnanosecond range together with a logic density of up to 30,000 usable gates.

▶ *Standard cell:*
the new 1.2 μ standard cell family offers density up to 60,000 gates and an average speed of 600 picoseconds, plus memory capability of 32K bits RAM and 128K bits ROM.

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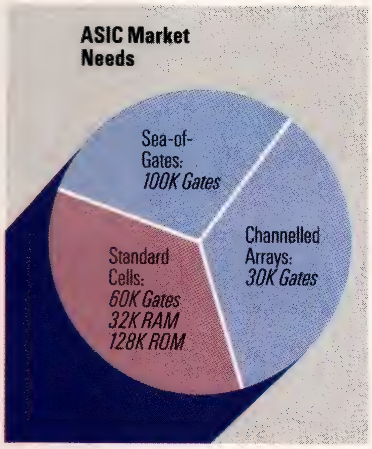
With automatic test-point generation built into each of these new products, test programs can be generated in a fraction of the time you'd normally spend—without sacrificing logic or speed. All three product families also use the same cell design library, for logic transparency.



Complete ASIC support

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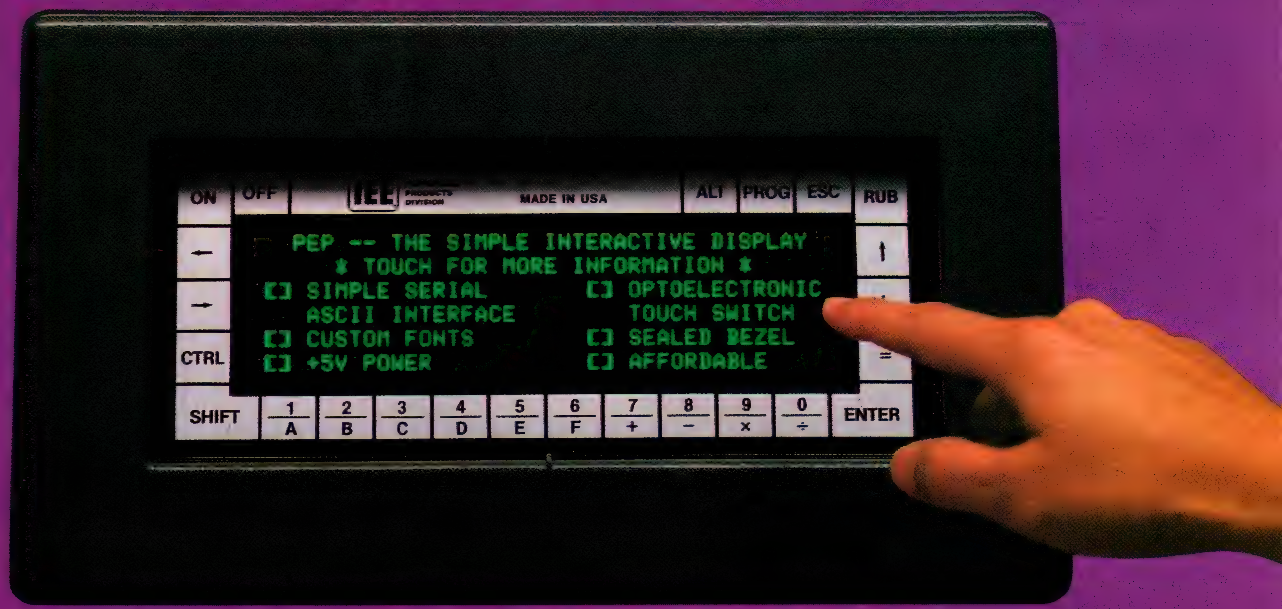
CIRCLE NO 133

Everything You Need In A Touchscreen Display



(hand not included)

"Everything" is no exaggeration when you're talking about **IEE's new PEP/VF™ Model 4283.** We started with a bright 6-line by 40-character vacuum fluorescent display that is easily filterable to a variety of eye-pleasing colors. On top of that we added an **opto-electronic** touchscreen for superior display appearance. But that's not all—the list goes on:

- Fits where a CRT can't—only 1.55″ deep from panel surface
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And all this at an affordable price!

So, call or write us today about our **PEP/VF** Interactive Display Module, and we'll give you a "hand"... figuratively speaking, of course!

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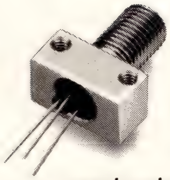
See us at WESCON '88 Booth #s 2254/55/56/57

CIRCLE NO 134

When you need the highest optical power, choose these peak performers from Honeywell.

HFE4854 and HFE4855.

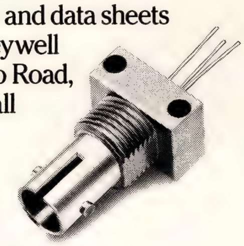


Announcing two top of the line Low Profile leaders. The HFE4854 and the HFE4855 are assembled using our new HFE4050 component. Both are constructed using high tolerance connectors and have the LED actively aligned to a fiber optic cable. These patented "Caprock" LEDs have a peak wavelength matched for use with Honeywell fiber optic receivers. Plus, they come equipped with standard optical connectors that accept 905/906 type SMA [HFE4855], or ST® [HFE4854] fiber optic cable connectors.

The new HFE4050 metal package, high power LED is featured in both the HFE4854 [ST style] and HFE4855 [SMA style] fiber optic connectorized components. They have the highest output power in the industry for standard 850 nanometer LEDs. In fact, they range from typical output powers of 145 μW [−8.4 dBm] to 410 μW [−3.9 dBm] into a 100/140 micron fiber optic cable at 100 mA forward current. Our new HFE4070 plastic package, high powered LED is featured in both the HFE4856 [ST style] and the HFE4857 [SMA style] connectorized components. They include a range from typical output powers of 40 μW [−13.9 dBm] to 115 μW [−9.4 dBm] into a 100/140 micron fiber optic cable at 50 mA forward current.

Once you've examined all the facts, you'll see why our Low Profile leaders have piqued so much interest. And you'll agree we're *the one choice for all your fiber optic needs*. That's because Honeywell Optoelectronics is one of the world's leading designers and manufacturers of fiber optic data communication components. With our proven track record and the experience of the over 100 year old, multinational Honeywell corporation you can rest assured we'll be there when you need us. Now. And in the future.

For additional information and data sheets of these products contact Honeywell Optoelectronics, 830 E. Arapaho Road, Richardson, Texas 75081. Or call **1-800-367-6786**. In Texas call 214-470-4271.



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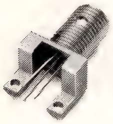
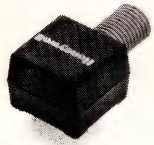
Transmitters
Receivers
LEDs
Photo Diodes

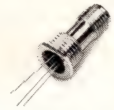


Fiber-DIP
Transmitters
Receivers
LEDs
Photo Diodes

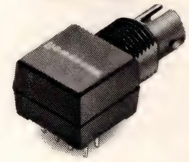


Modems:
Synchronous
Asynchronous

SMA 306 Style
Transmitters
Receivers
LEDs
Photo Diodes



Fiber-DIP
Transmitters
Receivers
LEDs
Photo Diodes



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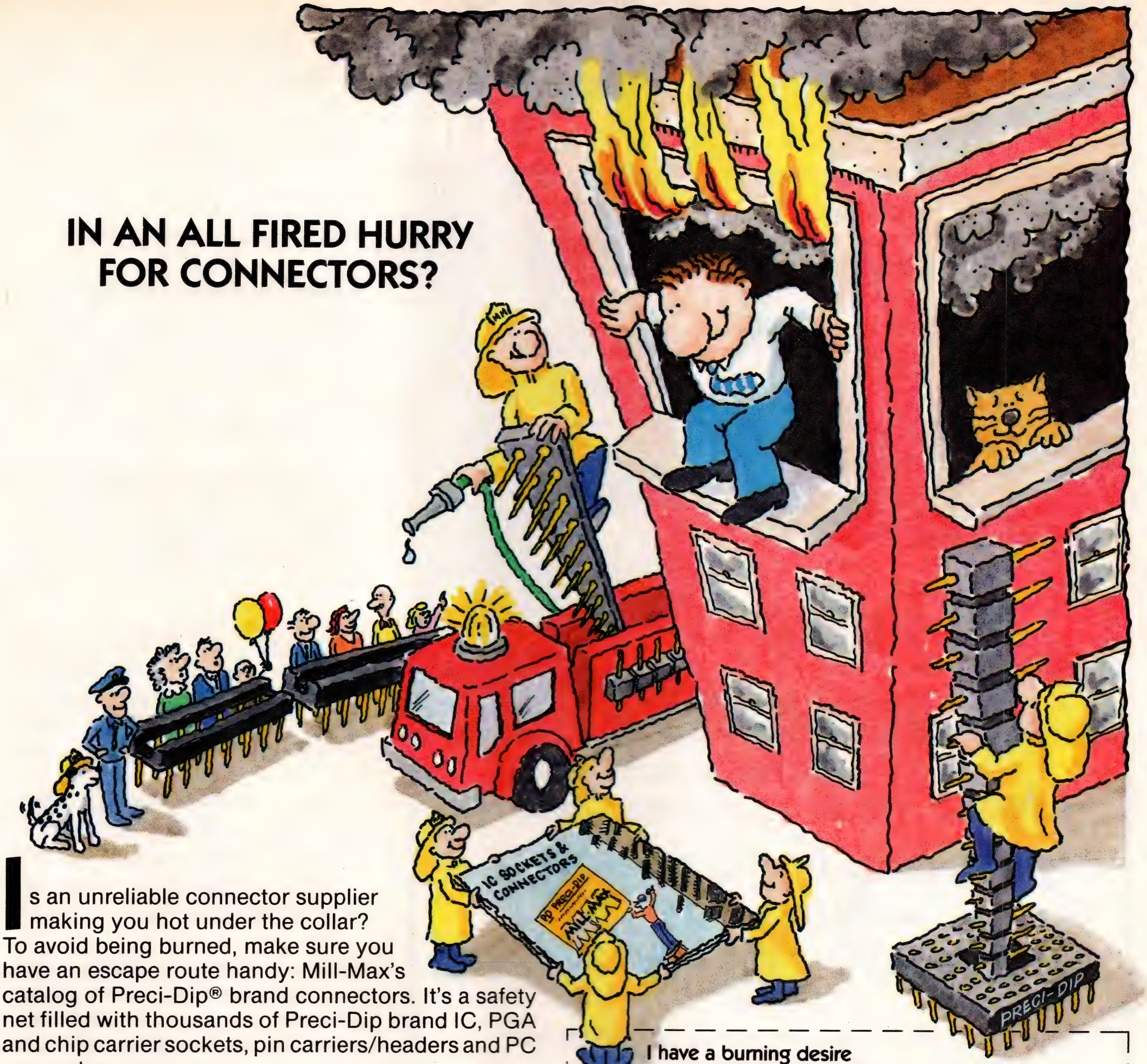
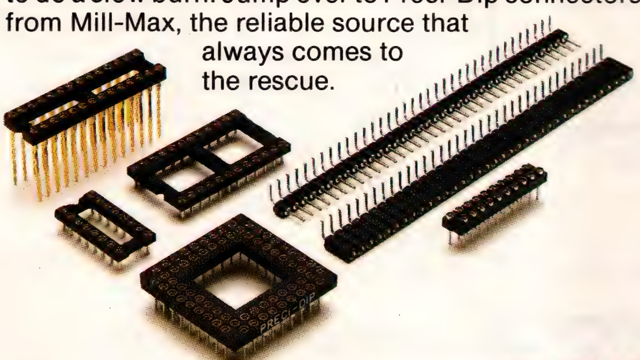
IN AN ALL FIRED HURRY FOR CONNECTORS?



Is an unreliable connector supplier making you hot under the collar? To avoid being burned, make sure you have an escape route handy: Mill-Max's catalog of Preci-Dip® brand connectors. It's a safety net filled with thousands of Preci-Dip brand IC, PGA and chip carrier sockets, pin carriers/headers and PC connectors.

With Mill-Max's large domestic manufacturing capabilities, plus our huge parts inventory which includes Euro-Dip connectors, we can pump out millions of products to satisfy any five alarm emergency. But we've also been known to go out on a limb to save small pet projects with our custom designs.

So don't let a tardy connector supplier cause you to do a slow burn. Jump over to Preci-Dip connectors from Mill-Max, the reliable source that always comes to the rescue.



I have a burning desire for the new Preci-Dip connector catalog.

Mail this coupon for a **free catalog**. Or, if you're in an alarming hurry, call **(516) 922-6000**, and we'll send it to your rescue.

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CASE Benchmarks: A Product Comparison Seminar, Denver, CO. Digital Consulting Inc, 6 Windsor St, Andover, MA 01810. (508) 470-3870. November 14 to 16.

Expert Systems: An Intensive Seminar on Choosing Applications and Tools, Chicago, IL. Digital Consulting Inc, 6 Windsor St, Andover, MA 01810. (508) 470-3870. November 14 to 16.

CASE and the Real World (seminar), Boston, MA. Digital Consulting Inc, 6 Windsor St, Andover, MA 01810. (508) 470-3870. November 15 to 16.

Pack Expo '88, McCormack Pl, Chicago, IL. Robert Newton, American Management Association, 135 W 50th St, NY, NY 10020. (212) 903-7936. November 15 to 17.

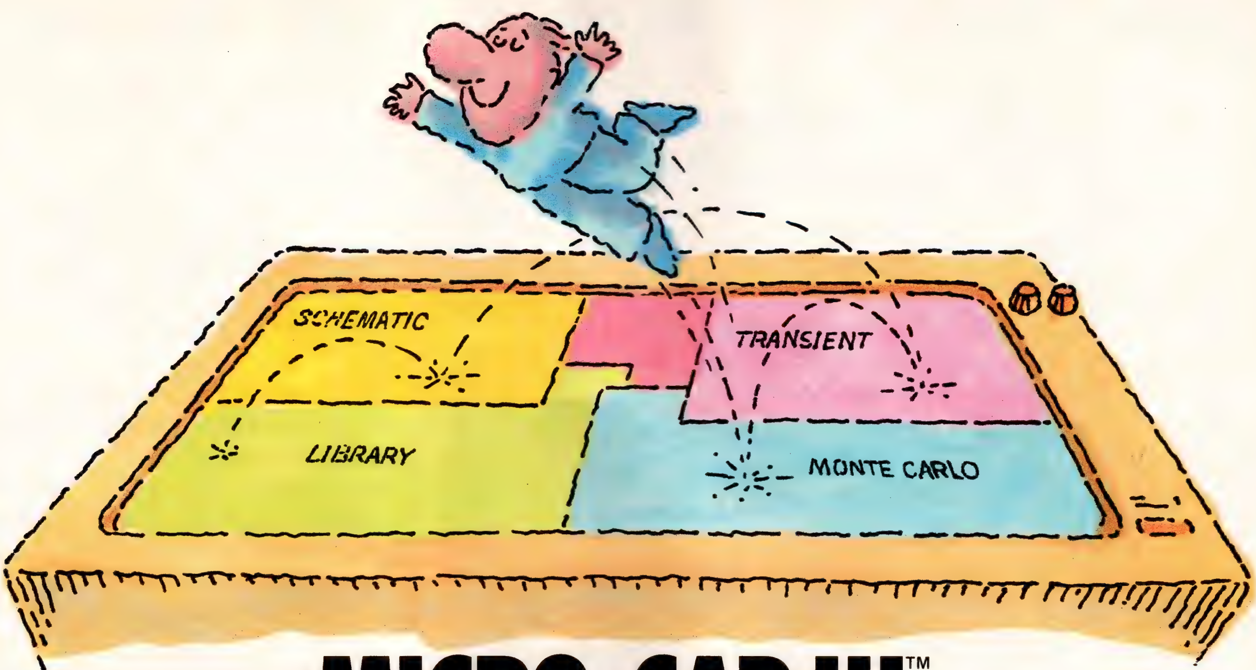
Fallcon '88 (35th Annual IEEE Fall Conference Electronics Exhibition), Cedar Rapids, IA. Martin Ambrose, conference chairman. (313) 395-3997. November 16 to 17.

CASE: A Manager's Guide (seminar), Washington, DC. Technology Transfer Institute, 741 Tenth St, Santa Monica, CA 90402. (213) 394-8305. December 6 to 8.

Fourth Aerospace Computer Security Applications Conference, Orlando, FL. IEEE Computer Society, 1730 Massachusetts Ave NW, Washington, DC 20036. December 12 to 16.

Programming and Interfacing the IBM PC for Data Acquisition and Control (short course), Orlando, FL. Purdue University School of Engineering and Technology at Indianapolis, 799 W Michigan St, Indianapolis, IN 46202. (317) 274-0806. December 12 to 16.

US-Hong Kong Technology Business Conference, Hong Kong. Asian American Manufacturers

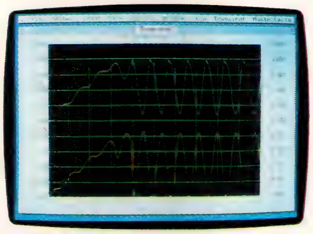


MICRO-CAP III.™ THIRD-GENERATION INTERACTIVE CIRCUIT ANALYSIS. MORE POWER. MORE SPEED. LESS WORK.

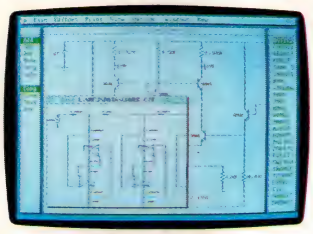
MICRO-CAP III,™ the third generation of the top selling IBM® PC-based interactive CAE tool, adds even more accuracy, speed, and simplicity to circuit design and simulation.

The program's window-based operation and schematic editor make circuit creation a breeze. And super-fast SPICE-like routines mean quick AC, DC, Fourier and transient analysis — right from schematics. You can combine simulations of digital and analog circuits via integrated switch models and macros. And, using stepped component values, rapidly generate multiple plots to fine-tune your circuits.

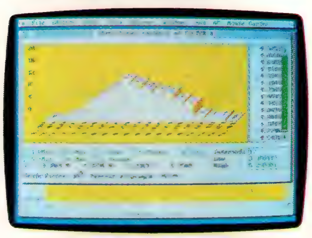
We've added routines for noise, impedance and conductance — even Monte Carlo routines for statistical analysis of production yield. Plus algebraic formula parsers for plotting almost any desired function.



Transient analysis



Schematic editor



Monte Carlo analysis

CIRCLE NO 138

Modeling power leaps upward as well, to Gummel-Poon BJT and Level 3 MOS — supported, of course, by a built-in Parameter Estimation Program and extended standard parts library.

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CALENDAR

Association, 800 Menlo Ave, Suite 115, Menlo Park, CA 94025. (415) 321-2262. December 19 to 23.

SC Global 89, San Francisco, CA. Superconductor Applications Association, 24781 Camino Villa Ave, El Toro, CA 92630. (714) 586-8727. January 11 to 13.

OE LASE '89, Los Angeles, CA. Society of Photo-Optical Instrumentation Engineering (SPIE), Box 10, Bellingham, WA 98227. (206) 676-3290; in Europe: SPIE, Koblenzer Strasse 34, D-5300 Bonn 2, West Germany, 49-228-36-15-46. TWX 172-283-747. January 15 to 20.

Fifth Annual Computer Graphics New York Show, NY, NY. Exhibition Marketing & Management Co, 8300 Greensboro Dr, Suite 110, McLean, VA 22102. (703) 893-4545. January 17 to 19.

The 1989 Optical Disk Systems Conference: From the Mail Room to the Board Room, Phoenix, AZ. CAP International Inc, 1 Longwater Circle, Norwell, MA 02061. (617) 982-9500. January 23 to 25.

ATE & Instrumentation Conference West, Anaheim, CA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. January 23 to 26.

Winter 1989 Unix Technical Conference, San Diego, CA. Usenix conference office, Box 385, Sunset Beach, CA 90742. (213) 592-1381. January 30 to February 3.

Electromagnetic Interference—Characteristics and Control (seminar), Center for Continuing Engineering Education, University of Wisconsin-Milwaukee, 929 N Sixth St, Milwaukee, WI 53203. (414) 227-3120. January 31 to February 2.

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Actions speak louder than words.
That's what we believe at Fujitsu. And that's why Sun Microsystems came to us to implement the SPARC™ architecture for the first time. Now, others are finally announcing or sampling their RISC products.

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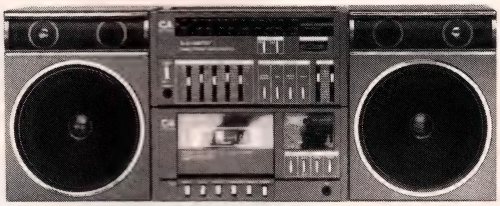
It's one thing to produce in the lab — and quite another to do it on the line. Day in, day out. Year after year.



We know, because we've been supplying RISC products in volume since 1986.

Our ability to ship this new technology is a result of many years of manufacturing experience, resulting in Fujitsu's ranking as the world's number one gate array supplier. We're a leading producer of memories as well.

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That's why we recommend the SPARC architecture of our MB86901 (S-25), and our other RISC devices. It provides a stable, cost effective migration path as we develop successive generations of microprocessors and peripherals to meet your future needs.

SPARC is the only RISC architecture that is available from multiple sources — to minimize your RISC risk. And the only solution that's been proven over time in the Sun Workstation — to guarantee its capability.

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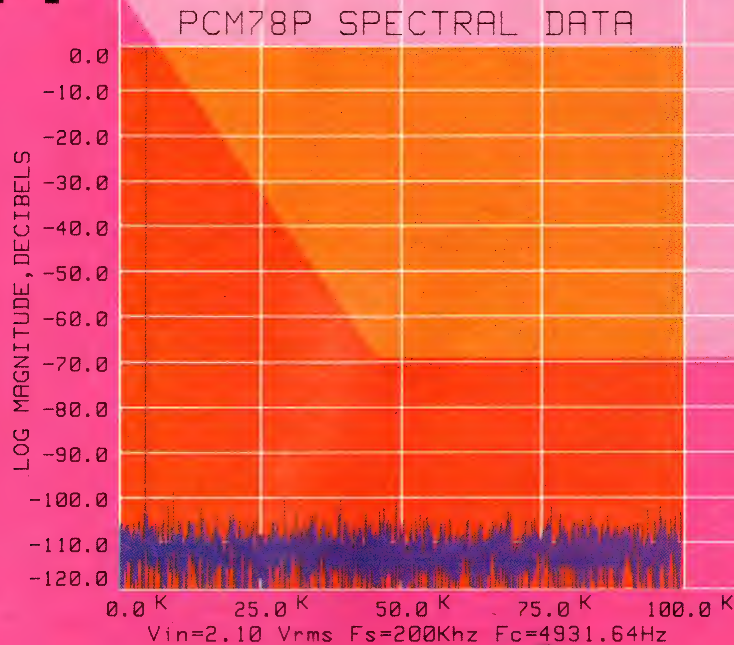
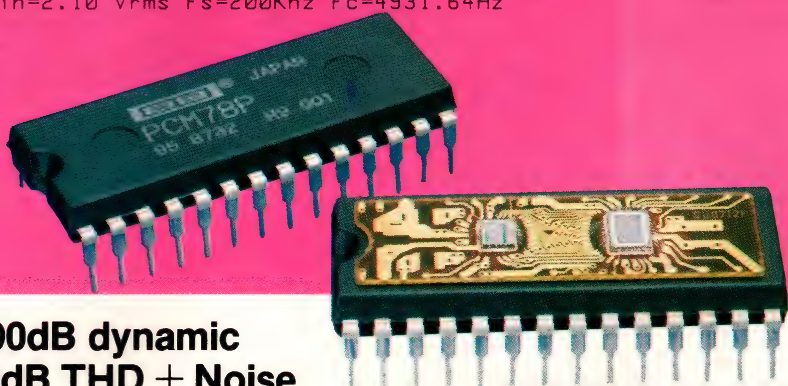
CIRCLE NO 143

New 16-bit ADC optimizes performance/price for precision dynamic applications.





PCM78P delivers wide 90dB dynamic range with ultra-low -88dB THD + Noise.

Our new PCM78P 16-bit A/D converter has been specifically designed and tested to excel in dynamic applications.

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PCM78P is almost a "drop-in" part; no external trimpots or reference needed, easy interfacing via the serial port and on-board latch. And its fast 4μs conversion time allows oversampling, reducing the complexity of antialiasing filters.

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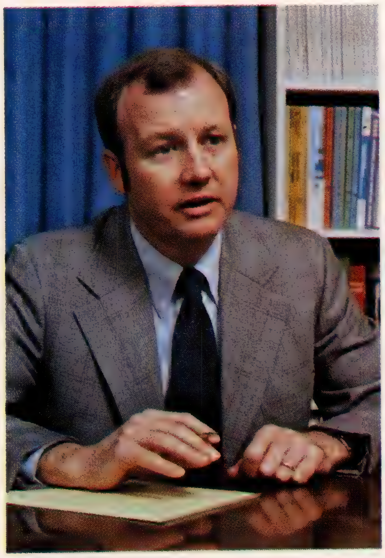
BURR-BROWN®

Approach forecasts with caution



Methods that fit equations to experimental data have been known for centuries, but using them to extrapolate beyond measured values requires great care. For example, you can use several equations to accurately predict the US's population growth for the last few decades. However, using these equations to calculate future population values can yield unusual results.

In fact, one equation shows that the US's population will plummet fairly soon. Perhaps the equation knows some secret about a nuclear war or a widespread famine. But it's more likely that the equation is at fault. People would spend their time better in checking data and equations than in preparing for the day of destruction.

Unfortunately, many people put great and often unquestioning faith in those who project or forecast future results. Back in 1984, many of the so-called industry analysts and forecasters were projecting robust growth for the personal-computer market. They spoke of continuing growth even as the computer market went bust in 1985. It should have been obvious in 1984 that 15 companies couldn't each capture 20% of the personal-computer market, yet few of us questioned the analysts as we prepared extra manufacturing capacity.

Likewise, many financial analysts were forecasting continuing growth in the stock market, right up until the stock-market crash in October 1987. It should have been obvious that the bullish stock market of the mid 1980s couldn't continue indefinitely, yet many of us believed the "experts" and invested more and more money. Prophecies of growth fueled themselves. Common sense no longer prevailed.

Now we hear analysts and seers predicting a recession in the semiconductor market within 15 to 18 months. But beware, that prophecy may come true simply because we assume it will, and because we plan accordingly. Thus, because "experts" tell us to expect a recession, we may cut back on important R&D spending, stop new projects, cut marketing plans, and shorten employee rosters. In response to predictions of gloom and doom, we may push ourselves further toward it without questioning the analysts' techniques and projection methods.

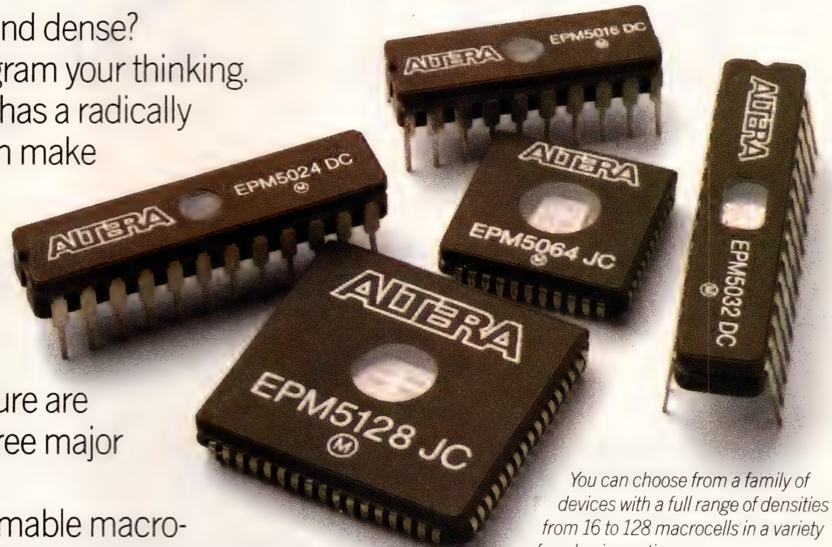
I don't mean that we shouldn't plan or that we shouldn't try to anticipate future markets and technical changes. However, we should be very wary about accepting what market analysts and forecasters tell us about the future. It's always worth questioning their methods and their data. Also, there comes a time to trust common sense and to ignore the seers and forecasters: This may be just the time to do that.

Jon Titus
Editor

Jesse H Neal
Editorial Achievement Awards
1987, 1981 (2), 1978 (2), 1977, 1976, 1975
American Society of
Business Press Editors Award
1988, 1983, 1981

If you believe EPLDs are constrained by their architecture, this should open your mind.

Introducing MAX. A totally new architecture that will change your thinking about EPLDs.



You can choose from a family of devices with a full range of densities from 16 to 128 macrocells in a variety of packaging options.

Still think that EPLDs can't be fast and dense?

Then prepare to erase and reprogram your thinking.

The new MAX family from Altera has a radically different EPLD architecture that can make your fastest, densest designs fly out the door in no time.

With twice the speed and three times the density of conventional EPLDs.

At the heart of the MAX architecture are Logic Array Blocks incorporating three major innovations:

First, streamlined, totally programmable macrocells with multiple control product terms.

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Finally, decoupled I/O that lets you use all your pins and flip-flops independently.

Tying it all together, a Programmable Interconnect Array (PIA) links MAX's multiple LABs efficiently.

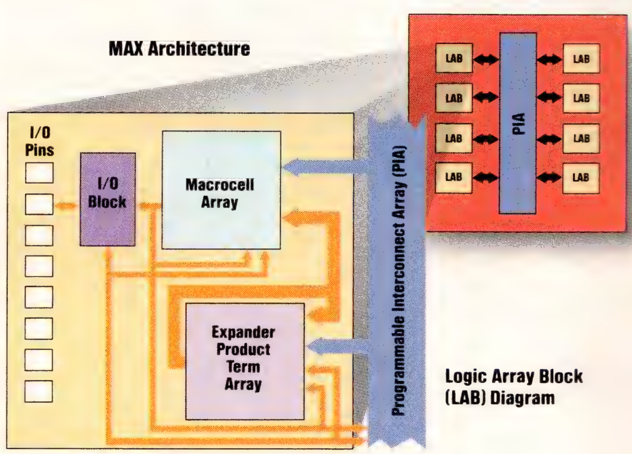
When you combine the MAX architecture with a high speed, 0.8 micron CMOS process, you get high density devices with extraordinary performance.

And to get those devices to market faster, there's MAX+PLUS.™ Logic synthesis makes it the most powerful, easy to use software ever developed for EPLDs.

That's why the MAX family is destined to become the new standard for logic design.

For more information, call Altera today: 1-800-545-3377.

And see how easy it is to change your thinking about EPLDs.



At the highest densities, MAX incorporates a Programmable Interconnect Array that gives you the high performance of small arrays with large array density.

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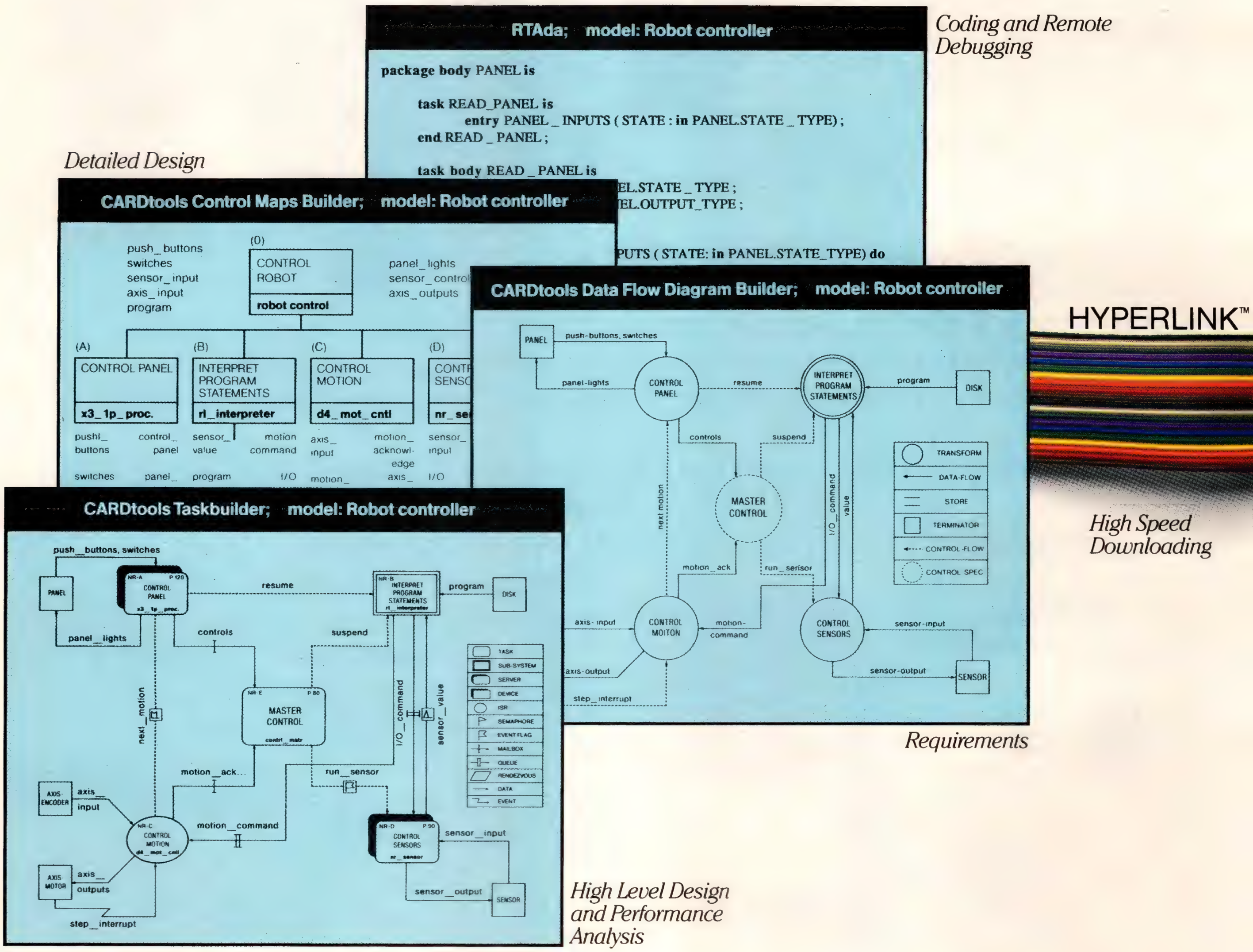
Do you have to design in



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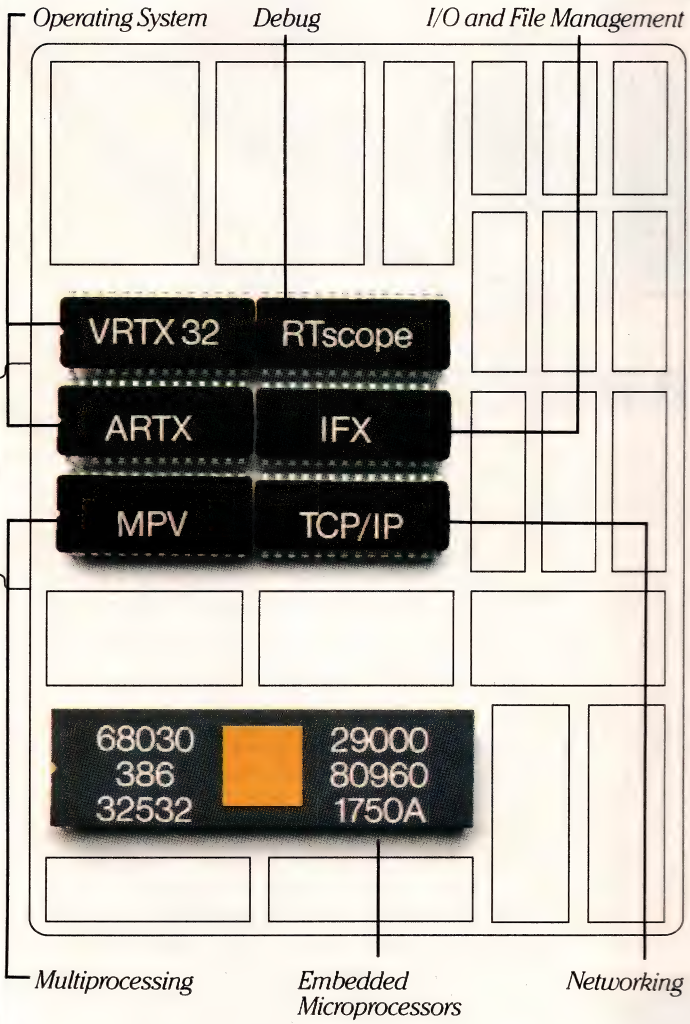

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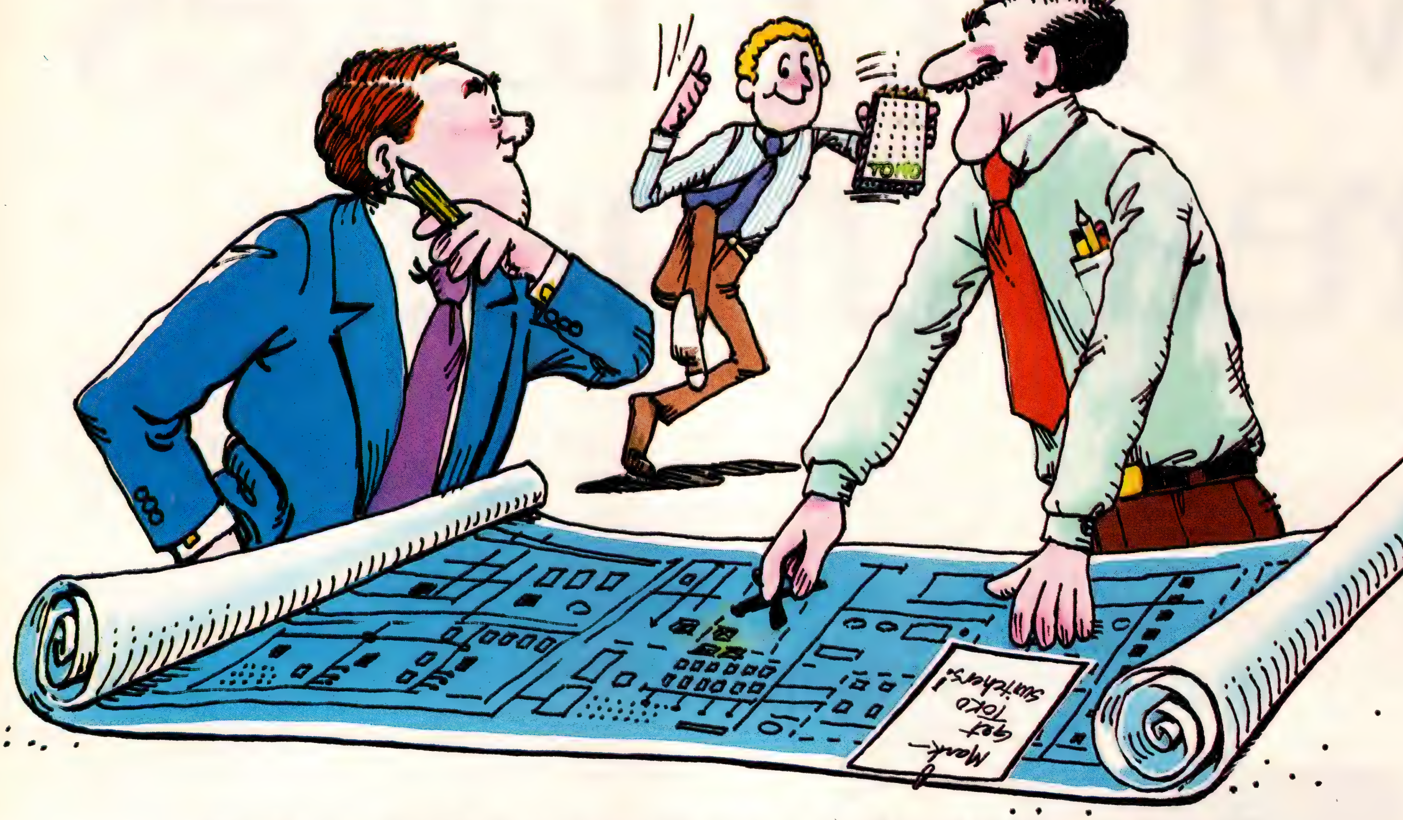

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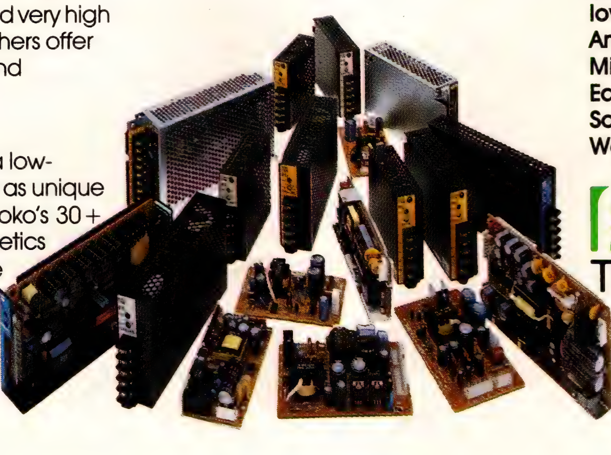
		15W		
EM	170-264	10W	3	6
		15W		
PU & PS	85-132/	10W	1	192
	110-175/	15W		
	170-264	30W		
		50W		
PE&PT	85-132/	15W	3 (PT)	60
	170-264	30W	1 (PE)	
		50W		
MW	85-264*	15W	3	7
		30W		
		50W		

*Automatic (no jumpers required)



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CIRCLE NO 147

ARBITRARY-WAVEFORM GENERATORS

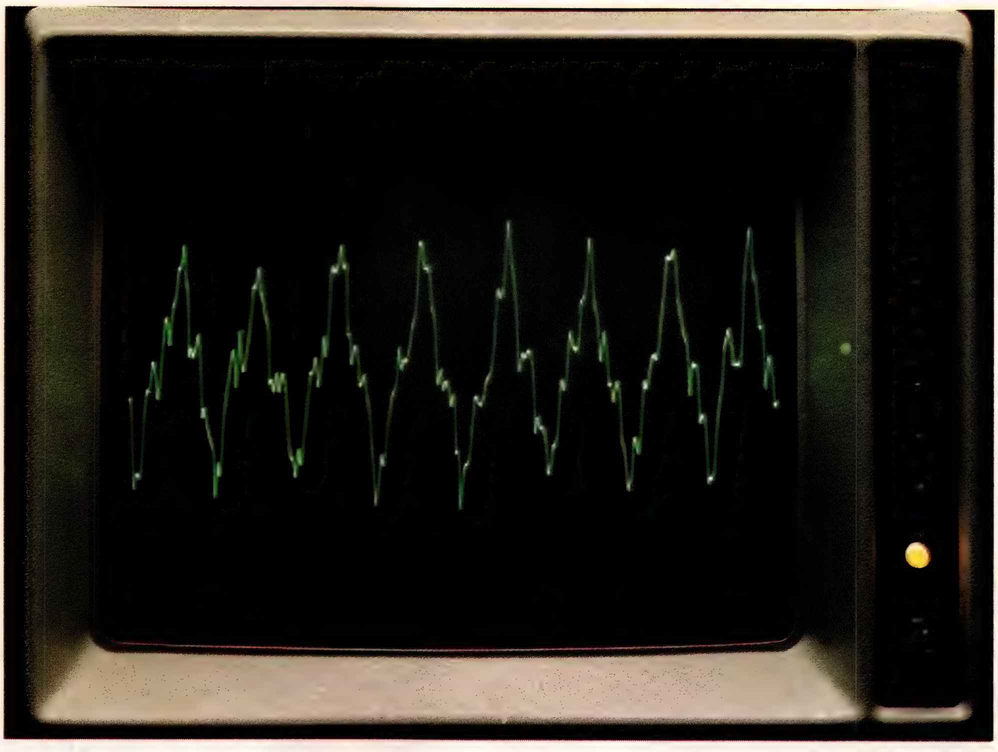
Instruments refine the art of signal generation

Arbitrary-waveform generators let you make your own kind of waves.

Dan Strassberg, Associate Editor

Arbitrary-waveform generators (or ARBs, in the shorthand of most vendors) are truly flexible tools for analog designers. Although the technology invites many plays on words—wave of the future, making waves, catching the wave—the puns have a serious aspect. For instance, a few vendors insist that ARBs represent the wave of the future; their capabilities are so desirable, they will totally displace the more conventional fixed-function generators during the next decade. ARBs do, of course, allow you to make waves: Some instruments produce standard waves, such as sine, square, and triangular ones, and all of them let you define custom waveforms as well. And, with the right software, most ARBs also let you catch a wave—record an interesting waveform from a system under test—and play it back repeatedly.

As with any instrument based on a relatively new technology, if you want to use it most effectively, you have to take the trouble to understand how it works. The distinction between arbitrary-waveform generators and fixed-function generators is not an . . . ahem . . . arbitrary one. Most ARBs use D/A converters to synthesize



***You can use the** HP 5182A waveform recorder/generator to reproduce random noise superimposed on a waveform captured from a floppy-disk read head.*

Announcing another
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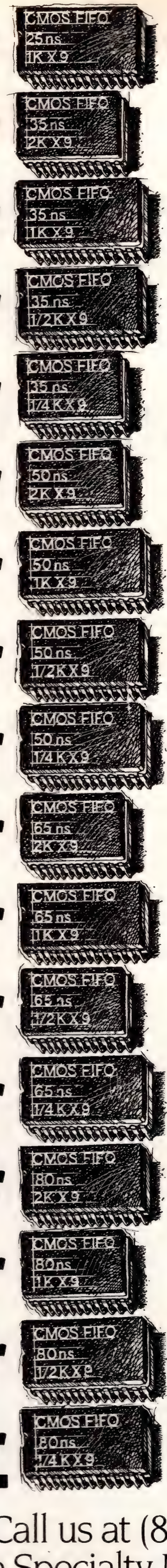

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CIRCLE NO 148

waveforms from the digital data stored in a waveform memory; fixed-function generators usually use purely analog circuit techniques. (Some ARBs that produce predefined and arbitrary waves use analog techniques to synthesize the predefined functions and use digital techniques to produce user-defined outputs. An example is the Tektronix AFG 5101/5501.)

Special facilities are needed

ARBs are complicated devices. To generate an output that is acceptably free of anomalies, DAC-based waveform generators have to have special facilities. For example, ARBs usually include multipole filters to smooth the DAC output; otherwise, a DAC-synthesized ramp would appear to be a staircase when you examined it closely. ARBs also often include deglitchers to remove transient aberrations from DAC outputs.

Nonetheless, when using an ARB, you need to keep in mind that an arbitrary-waveform generator is a sampled-data system and that its fundamentally digital nature may profoundly affect its performance in certain applications. One instance is where an ARB supplies a signal to a system that is sensitive to low levels of high-frequency noise. The specification that holds the key to the suitability of a particular generator for noise-sensitive applications is, of course, its S/N ratio. Generally, high-end ARBs specify their S/N ratio, but certain lower-priced units don't.

Most arbitrary-waveform generators **(Table 1)** can send data from their waveform memories to their DACs at rates no faster than about 40M words/sec. However, Analogic Corp just introduced two generators that can go substantially faster; Models 2040 and 2045 each specify a maximum data rate of 800M points/sec. Analogic claims that this

TABLE 1—REPRESENTATIVE ARBITRARY-WAVEFORM GENERATORS

VENDOR	MODEL	PRICE	FREQUENCY RANGE[1] (% OF P-P OUTPUT)	NON-LINEARITY[5]	WAVEFORM STORE[7]	MAX P-P OUTPUT VOLTS IMPEDANCE (Ω)	COMMENTS
ANALOGIC	2020-25	\$5985	DC TO 25 MHz	±0.025	N	10/50	
	2020-100	\$9495	DC TO 100 MHz	±0.025	N	10/50	
	2040	\$13,500	DC TO 800 MHz	0.2	N	1/50	SEE TEXT
	2045	\$14,500	DC TO 800 MHz	0.2	N	5, 1/50[8]	SEE TEXT
ARRAY ANALYSIS	MFI-1000	\$3620	DC TO 25 MHz	0.5	D, N	12.8/<1	USES EXTERNAL PC
GAGE APPLIED SCIENCES	COMPUGEN 840	\$1995	DC TO 20 MHz	1	D, N	±5/50	PC BUS PLUG-IN CARD
HEWLETT-PACKARD	3314A	\$4485	0.001 Hz TO 20 MHz	0.2	N	10/50	
	3325B	\$4590	0.1 Hz TO 10 kHz[2]	0.05	N	12/N/S	
	5182A	\$27,500	<100 μHz TO 10 MHz	N/S[6]	D, N	10.23/50	
	8175A OPT 002	\$14,265	DC TO 50M BPS[3]	1 AT 100 kHz	D, N	16/>50k	
	8904A	\$2600	DC TO 600 kHz	N.S.	N	20/50	SEE TEXT
KRON-HITE	5910C	\$3350	0.0001 Hz TO 10 MHz	1	N	30/50	
	5920	\$3995	0.0001 Hz TO 10 MHz	1	N	30/50	
LECROY	9100	\$11,900	DC TO 100 MHz	±1	N	10/50	
	9101	\$9900	DC TO 100 MHz	±1	N	10/50	
	9109	\$12,900	DC TO 100 MHz	±1	N	10/50	
ORION	OMNILAB 9420	\$8900	0.008 Hz TO 17 MHz	0.5	D	8/50	PC-BASED, BRIEFCASE-SIZE UNIT. ALSO ACTS AS LOGIC ANALYZER, DSO.
QUA TECH	WSB-10	\$795	DC TO 5 MHz	0.018	D	5.12/50	PC BUS PLUG-IN CARD.
TEKTRONIX	AFG 5101 AFG 5501	\$3395 \$3995	1 μHz TO 5 MHz[4]	N/S	N	9.99/50	AVAILABLE PACKAGED AS MODULE OR AS STAND-ALONE INSTRUMENT.
WAVETEK	75	\$2295	0.02 Hz TO 2 MHz	N/S	N	10/50	
	175	\$5095	0.001 Hz TO 5 MHz	N/S	N	10/50	
	275	\$3850	0.00375 Hz TO –3.75 MHz	N/S	N	10/50	
	680-10	\$2950	100 μHz TO 20 MHz	N/S	N	20/50	INSTRUMENT ON A CARD.

NOTES:

1. FOR SOME VENDORS, THIS COLUMN CONTAINS THE MAXIMUM RATE AT WHICH A GENERATOR CAN OUTPUT NEW DATA POINTS. FOR OTHERS, THE FIGURE IS THE MAXIMUM SINE-WAVE OUTPUT FREQUENCY — A VALUE ROUGHLY HALF THE MAXIMUM POINT RATE.
2. MAXIMUM FREQUENCY GIVEN IS FOR ARBITRARY WAVES. UNIT PRODUCES SINE WAVES TO 21 MHz, SQUARE WAVES TO 11 MHz, AND RAMP AND TRIANGULAR WAVES TO 11 kHz.
3. DAC HAS 10-BIT WORD, SO IF YOU SUPPLY 10-BIT VALUES, THIS RATE CORRESPONDS TO DC TO 5M POINTS/SEC.
4. RANGE GIVEN IS FOR ARBITRARY WAVES AT 2 POINTS/WAVEFORM. ANALOG GENERATOR IN SAME UNIT OPERATES FROM 0.012 Hz TO 12 MHz.
5. UNLESS OTHERWISE SPECIFIED, NONLINEARITY IS FOR 1-kHz TRIANGULAR WAVE.
6. NOT SPECIFIED.
7. D = DISK DRIVE, N = NONVOLATILE MEMORY
8. DISK DRIVE REQUIRES HP 9122D.
9. TWO OUTPUTS.

Arbitrary-waveform generators

capability makes the 2040 and the 2045 four times as fast as the previous record holders—LeCroy's 9100, 9101, and 9109. Both the new Analogic units and the three LeCroy instruments use 8-bit DACs. These DACs have a resolution lower than that of the DACs in most slower generators, including those in Analogic's 2020-25 and 2020-100, which use 12-bit DACs.

Bits aren't everything

It is easiest, but not necessarily most meaningful, to characterize an ARB in terms of the number of bits its DAC can resolve, the maximum clock rate at which it can send new data words to the DAC, and the size (depth) of its waveform-storage memory. Taken together, the maximum clock rate and the memory depth hint at an ARB's maximum output frequency. The maximum rate at which an ARB can output a waveform is equal to its maximum clock rate divided by the number of points that define the waveform.

Suppose you are synthesizing sine waves. If you can operate the generator so that the output filters remove substantially all of the higher-frequency components present in the square (or nearly square) wave produced by the DAC, you may only need slightly more than two points per cycle—that is, the generator will produce acceptable sine waves to a frequency just below the theoretical maximum (the so-called Nyquist frequency). If you can't use the filters in this manner, for many applications eight points per cycle will be adequate. So, if a generator has a maximum clock rate of 50M points/sec, its maximum sine-wave output frequency will lie between 6.25 MHz and a little over 20 MHz.

In fact, the combination of an ARB's DAC resolution, the characteristics of its output filters and amplifiers, and the level of distortion you can tolerate will determine the highest frequency at which the generator produces an acceptable sinusoidal output. If your application can tolerate only very low levels of distortion, you may need more than eight points per cycle, and you may not be able to accept a generator that uses 8- or 10-bit DACs; you may need one with 12-bit D/A converters. (Units that use 16-bit DACs will most likely appear within the next year.) You'll probably be better off, though, if you try to determine from the vendor's data sheet what the level of distortion will be in your application; it's difficult, if not impossible, to predict output distortion from DAC resolution alone.

***You have a choice** of modular or standalone mounting with the Tektronix AFG 5101/5501. Using an analog source, the arbitrary-waveform generator produces sine, square, and triangular waves.*

Evaluating vendor claims

Some vendors of arbitrary-waveform generators claim that ARBs produce ramps with linearity surpassing that of fixed-function generators. In actuality, there is nothing inherent in the technology of most ARBs that would yield linearity better than that of purely analog generators. It is possible—though not easy—for a manufacturer to build linearity correction into an ARB. If you work at it, you can make the generator produce predistorted waveforms to correct for nonlinearity in the DAC or amplifier chain.

Another vendor contention is that ARBs produce waveforms with sharper corners than those that analog generators produce. Again, there is nothing innate in ARB technology to make this claim true; the waveform corners' sharpness is a function of the bandwidth of the analog-signal path.

A third claimed advantage of ARBs over analog generators is an

***By summing and modulating** functions selected from a library, the HP 8904A can create a very wide variety of waveforms, albeit not any imaginable waveform.*

CIRCLE NO 149

ARB's ability to produce waveforms with discontinuities. Unlike the other two claims, this claim has some validity. Even though most analog function generators can develop a square wave—the quintessential discontinuous waveform—ARBs offer greater flexibility in producing discontinuous waveforms.

The sharpness of the discontinuities you can produce with a particular ARB depends, however, on the characteristics of the amplifiers and the filters that follow the DAC. To enhance the generation of discontinuous waves, some ARBs permit you to switch their filters out of the signal path. When you operate an ARB with its filters off, however, its S/N ratio will decrease.

Pick your package

Within the category of arbitrary-waveform generators, you'll find instruments that conform to several packaging conventions. The most usual are the rack-and-stack or stand-alone types (a category that Tektronix insists on calling "monolithic" despite the inevitable confusion with IC fabrication technology). You'll also find submodular instruments designed to mount in proprietary cages; instruments on a card that plug into the IBM PC bus; and a briefcase-size, PC-based, multifunction unit that, in addition to generating waveforms, performs the functions of other instruments (for example, a logic analyzer and a DSO) Recently, a VXI Bus-based module designed to mount in industry-standard cages made its debut. (Tektronix manufactures this ARB, but at the time of publication the vendor had not yet established the model number or the price.)

Arbitrary-waveform-generator performance and pricing are nearly as varied as the instruments' packaging. Base pricing varies tremendously, from $795 to over $27,000, but you'll find many units that fall in the $3000 to $5000 range.

When you compare ARBs with fixed-function generators, arbitrary-waveform generators exact a price premium. This premium buys you a rich set of features and a lot of versatility, but in choosing between an ARB and a fixed-function generator (or in deciding which ARB is best for you), you have to keep the dictates of your application uppermost in your mind.

In certain applications ARBs are indispensable. A good practical example is disk-drive testing, where a generator can replicate long data patterns such as the ones you would see at the output of a read head reading an entire data track. Other appropriate applications include the simulation of vibration waveforms, telecommunications-systems testing, radar-system testing, and elec-

__A clock rate of 125 MHz and__ 12-bit resolution are desirable features of the HP 8770S system. It also makes use of a workstation for waveform definition.

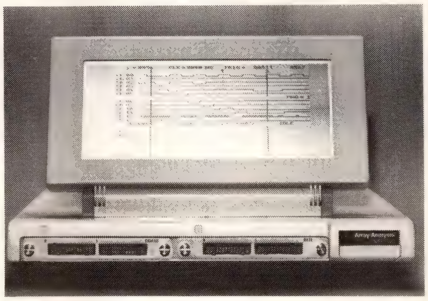
__The 5920 arbitrary-waveform generator,__ available from Kron-Hite, boasts an autoprogrammer that executes conditional steps and loops and a master clock whose typical accuracy is 0.01%.

tromagnetic-pulse simulation. In analog circuit design, especially in filter characterization, the ability of multiple ARBs to produce outputs that exactly correspond in phase as well as in frequency can be very valuable. You can, of course, also use ARBs to replace less-versatile fixed-function generators.

Consider an example

One example of an ARB's versatility is the capability to produce a sinusoidal swept-frequency output whose amplitude varies very little—or not at all—with frequency. Most ARBs use linear-phase output filters to attenuate the high-frequency noise components that their DAC outputs contain. These types of filters' response exhibits the smallest overshoot at waveform discontinuities. Such filters do not, however, provide the flattest sinewave amplitude response.

If you want an ARB to produce a sinusoidal output whose amplitude is independent of frequency, you can make its DAC produce a waveform whose amplitude increases with frequency the opposite of the way the filter's response rolls off. This technique has its limitations of course: If, at high frequencies, you try to obtain too big an amplitude boost, at low frequencies you'll only be using a small portion of the DAC's dynamic range.



***Waveform generation** is only one of the capabilities of Array Analysis' modular MFI-1000.*

You'll probably want to use your ARB to generate simple waveforms like sine waves and triangular waves, but if that's all you plan to use the generator for, you can save yourself money by purchasing a fixed-function instrument. Generating complex waveforms is an ARB's forte and defining some waveforms can require hundreds or even thousands of points. A generator's memory depth can limit the complexity of the waveforms it can generate. However, some vendors (LeCroy for example) make instruments that can repeat segments within a waveform, thus allowing them to create waveforms that, in effect, contain many more points than their memories can hold.

The list of techniques that you can use to define waveforms for the different generators is nearly as long as the list of generators itself:

- Defining the ordinate (Y value) for each abscissa (X value) point;
- Defining the ordinates at a subset of the abscissa points and using a connect-the-dots approach to linearly interpolate between points;
- Defining the ordinates at a subset of the abscissa points and using polynomials to connect the points with a smooth curve—the so-called spline-fit technique;
- Defining by equations;
- Combining segments extracted from previously defined waveforms—as stan-

For more information . . .

For more information on the arbitrary-waveform generators described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

Analogic Corp
8 Centennial Dr
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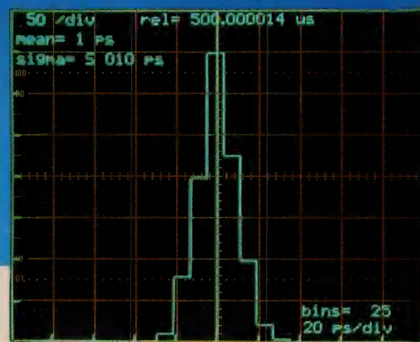

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Arbitrary-waveform generators

dard functions from a library or as user-defined functions;

- Summing waveforms;
- Modulating one waveform by another;
- Digitizing waveforms sketched on a graphics tablet;
- Playing back prerecorded waveforms;
- Combining some or all of the above techniques.

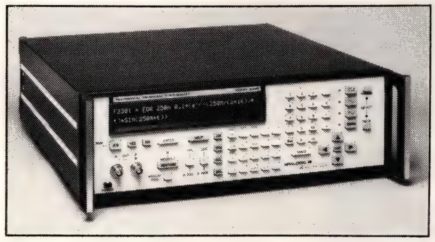
This list does not include the ability that most generators have of gating their outputs on and off, often under control of an externally derived signal; of producing waveform bursts; and of varying their output frequencies, sometimes under control of an arbitrary function of time.

To facilitate the use of these techniques, some vendors have devised special waveform-description languages that run on external computers. Others have implemented the waveform-generation capability in firmware, thus allowing (or requiring) you to use the generator itself for waveform definition.

Go for a drive

Learning how simple or difficult a particular instrument's definition process will be for you really requires a "test drive." Watching a demonstration by someone familiar with the operation of a particular instrument can be misleading by making a fairly complex operation look simple.

When an ARB catches a wave—accepts digitized waveforms, whether from a graphics tablet or from a waveform digitizer—the waveforms are loaded into the generator in one of two ways. Some generators include disk drives, and others require you to load memory via an RS-232C or an IEEE-488 port. Certain instruments have nonvolatile, battery-backed waveform memory, whereas others require that you reload the waveform memory each time you apply power. If a generator has a volatile waveform memory and no disk drives, each time you use it you must be prepared to round up the other instruments necessary to download waveforms into the generator's memory.



An 800-MHz clock rate, *which the vendor claims is the fastest of any arbitrary-waveform generator, is the most notable attribute of Analogic's 2045.*

If your work involves analog circuits, telecommunications technology, electromechanical systems, electromagnetic-pulse research, or any of several similar disciplines, the chances are that you can benefit from an arbitrary-waveform generator. ARBs aren't for everyone, however. Although you can expect the cost of the DACs and the digital components that ARBs use to continue to decline, yielding lower-cost generators in the future, for now you must be prepared to pay a price for flexibility and versatility. The likelihood is small that selecting an ARB over an analog generator will cause you insurmountable technical problems, but no substitute exists for learning the advantages and limitations of the instrument you are thinking of purchasing before you spend your company's money. EDN

References

1. Strassberg, Dan, "PC-based logic analyzers," *EDN*, October 13, 1988, pg 134.

Article Interest Quotient
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2kVA DC Motor Speed Control. 1 Integrated Circuit. 1 Leader.

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For more information on the VB100 and all the other devices in the SGS-THOMSON VIPower range, contact the sales office or distributor nearest you.

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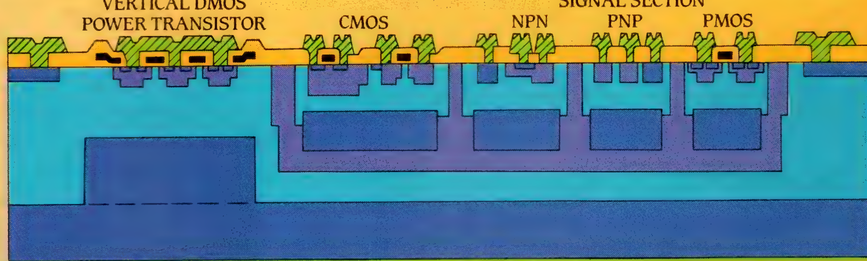
SGS-THOMSON's VIPower Overpowers the Competition



M2: Power MOS/BCD Technology

VIPower (Vertical Intelligent Power) gives you high voltage and high power output circuit complexity. In fact, when you consider that VIPower is designed to produce intelligent devices with output stages ranging from a 1200V bipolar to massive 100A Power MOSFETs, it is truly without equal!

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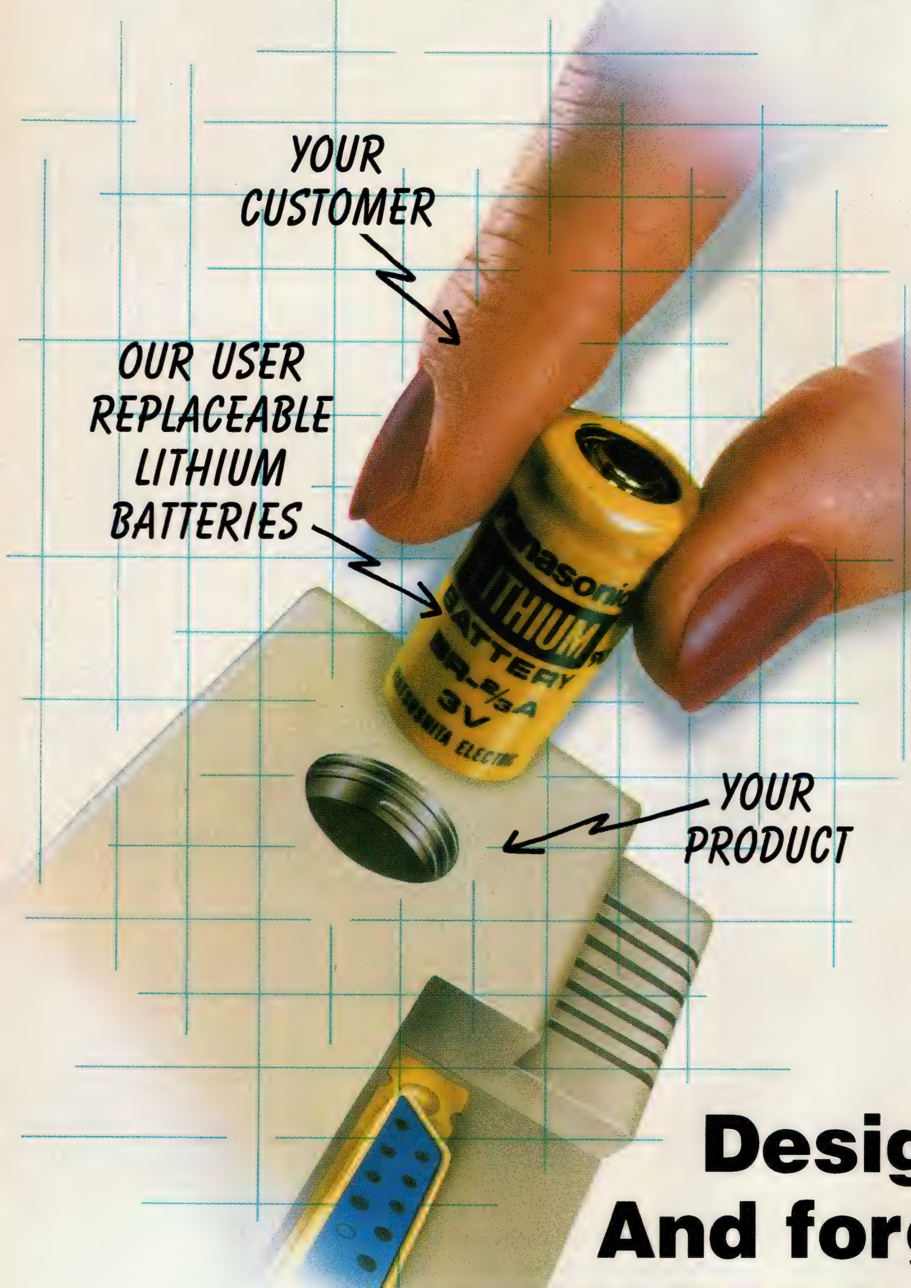

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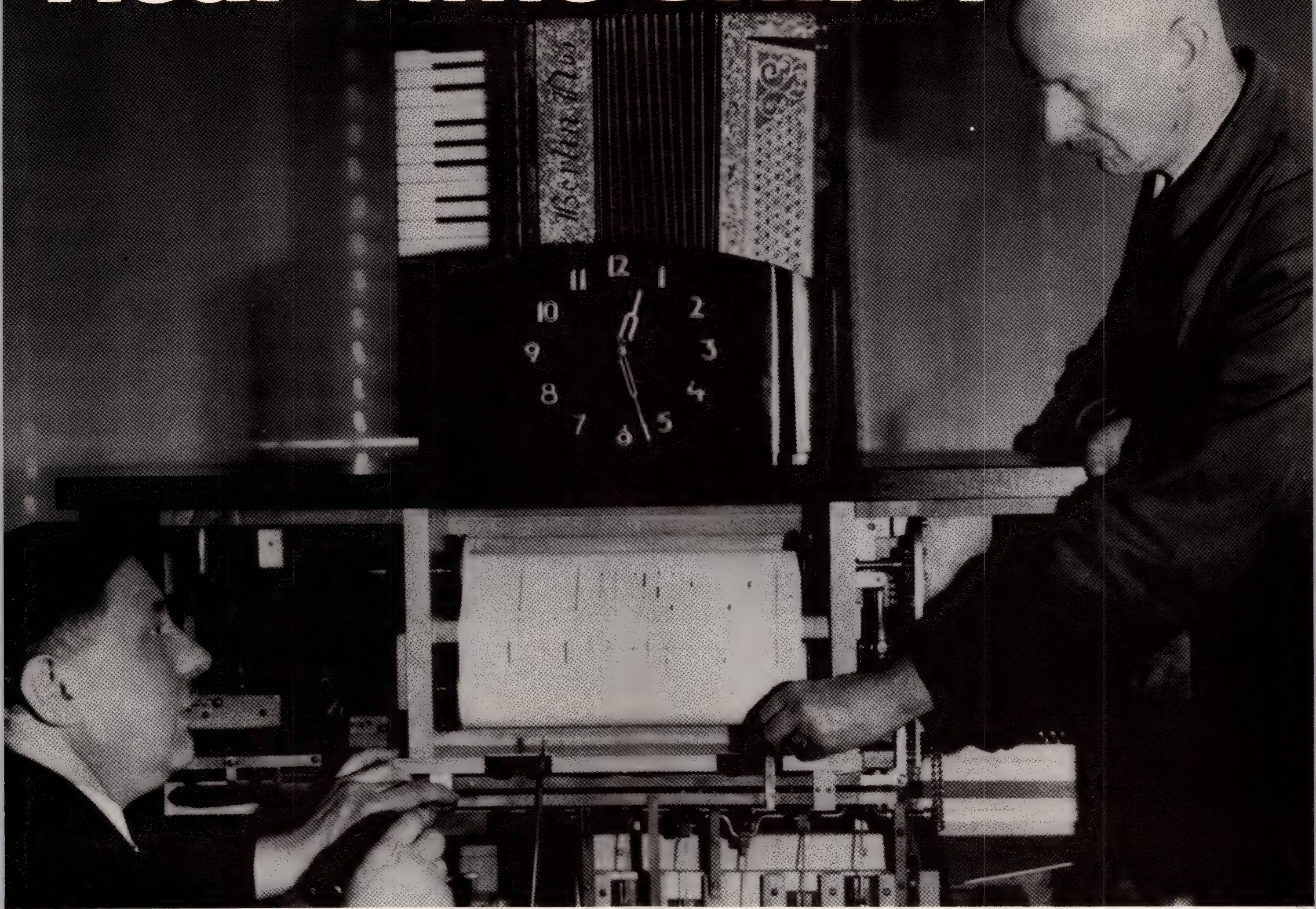

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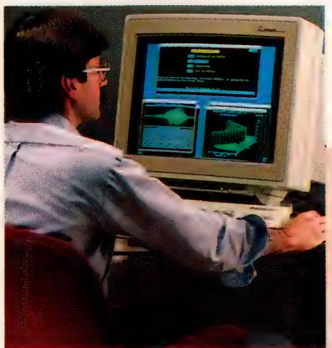

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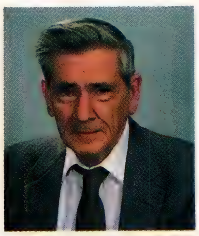
ICs use resonant-mode conversion techniques



Designers of high-frequency switching power supplies are beginning to explore resonant-mode conversion to overcome the disadvantages of pulse-width-modulation techniques.

Dave Pryce,
Associate Editor

While systems designers continue to fuel the demand for cost-effective power supplies that provide ever higher power densities, designers of switching power supplies are taking aim at these targets with some potent high-frequency ammunition. Although high-frequency power conversion offers the advantage of smaller power supplies having high power densities, there are disadvantages to the conventional pulse-width-modulation (PWM) techniques used with most high-frequency switchers.

Among these disadvantages are added losses in the power switches during turn-on and turn-off, increased EMI and RFI, and increased power losses caused by parasitic capacitance and leakage inductance. To overcome these disadvantages, designers of high-frequency switchers are beginning to explore resonant-mode conversion, a form of frequency modulation (FM).

Compared with PWM circuits, resonant-mode switching circuits offer a number of advantages. For example, because the resonant circuit generates a sine wave, designers can operate the power switches at zero-current and zero-voltage points in the resonant waveform, greatly reducing the power loss in the switches. **Fig 1** illustrates representative waveforms of current and voltage for PWM control and resonant-mode control.

Equally important, the sine wave

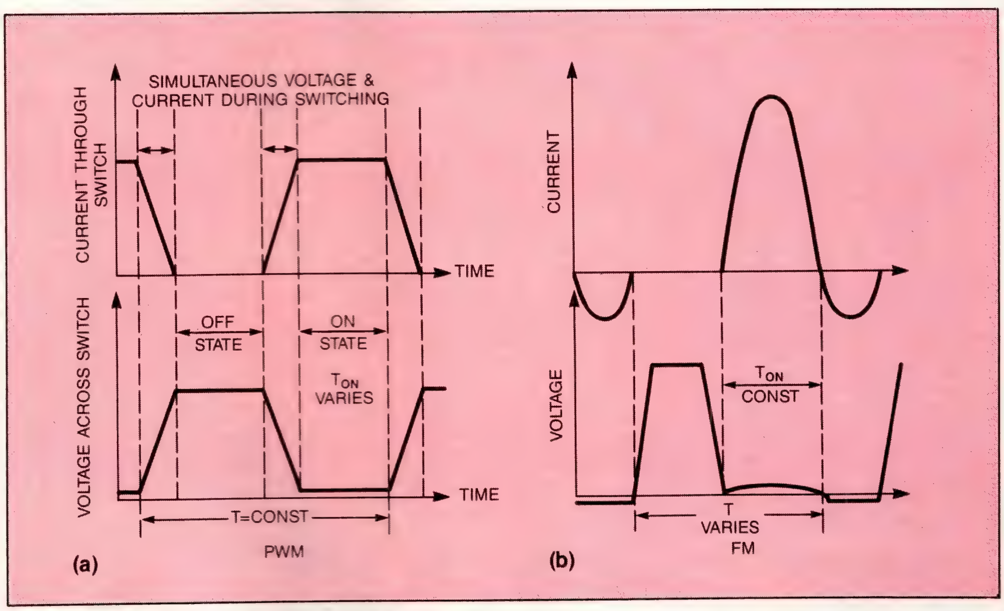
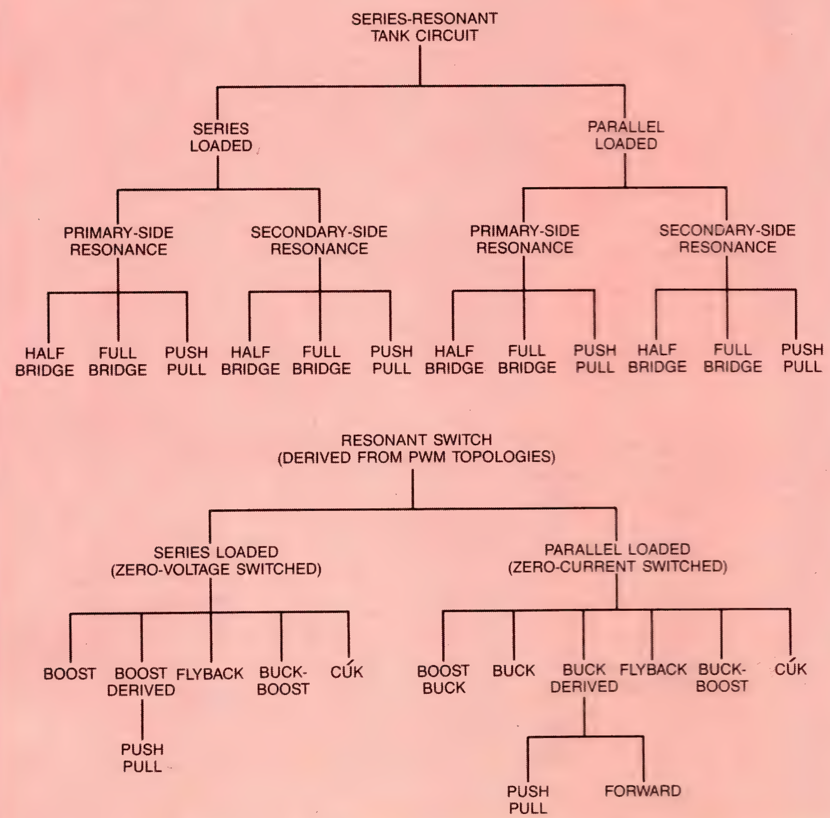


***Fig 1—The power-switch waveforms for PWM (a) and FM (b) converters** exhibit significant differences. With PWM (pulse-width-modulation) conversion, there is simultaneous conduction of voltage and current during part of the switching cycle. FM (resonant-mode) conversion generates a sine wave, which can be switched at zero current.*

Resonant-mode conversion

TABLE 1—RESONANT-MODE TOPOLOGIES



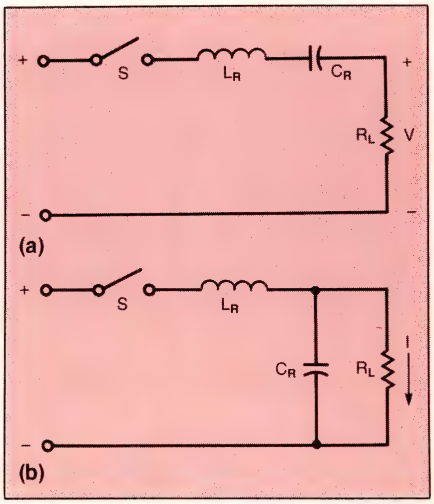


Fig 2—Resonant-mode converters can vary in their method of output loading. *Series-loaded converters **(a)** act as current sources. Parallel-loaded converters **(b)** act as voltage sources.*

produced by the resonant circuit minimizes the generation of high-frequency harmonics, which, in turn, reduces EMI and RFI. Moreover, because the resonant circuit has relatively large inductance and capacitance values, parasitic reactive elements have less effect on the overall circuit performance. In fact, designers sometimes utilize the junction capacitance of the switching transistor or the leakage inductance of the transformer as part of the tuned circuit.

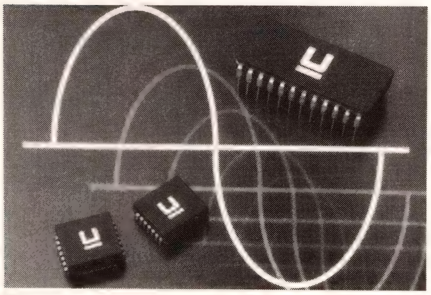
Although myriad variations are possible (see **Table 1**), all resonant converters have one thing in common—a tuned (resonant) L-C tank circuit. Activated by a dedicated resonant-mode controller, the converter's switching transistor drives the resonant circuit with a square-wave pulse of voltage or current. The action of the resonant circuit's circulating current converts the square-wave pulse to a sine wave. Depending on circuit requirements, some or all of this circulating energy is used to supply power to the load.

The quality factor, Q, of the resonant circuit determines the actual purity of the sine wave, but Q is not the major consideration. Of more importance is the impedance of the resonant circuit compared with that of the transformer or the load. This relationship is largely determined by the circuit configuration.

Fig 2 shows two basic circuit configurations—the *series-loaded* converter and the *parallel-loaded* converter. As the name implies, the series-loaded converter has its load in series with the resonant-circuit elements and acts as a current source with a high-impedance output. Conversely, the parallel-loaded converter has its load connected across the resonant-circuit elements and acts as a voltage source with a low-impedance output.

To some extent, the choice of a basic circuit configuration depends on the application. For example, supplies used to drive a capacitive load are usually better served with a series-loaded converter that acts as a current source. Other supplies, such as those used to supply varying amounts of current to a 5V bus, usually employ a parallel-loaded converter. **Fig 3** shows two commonly used circuits for resonant-mode control—a series-loaded flyback converter and a parallel-loaded half-bridge converter.

All resonant-mode control circuits keep the pulse-width constant and vary the frequency, unlike conventional control schemes, which use fixed-frequency pulse-width modulation. There are two possible modes of variable-frequency control that define the flow of current in



These resonant-mode control chips *from Unitrode provide sine-wave switching for regulating the output of switch-mode power supplies.*

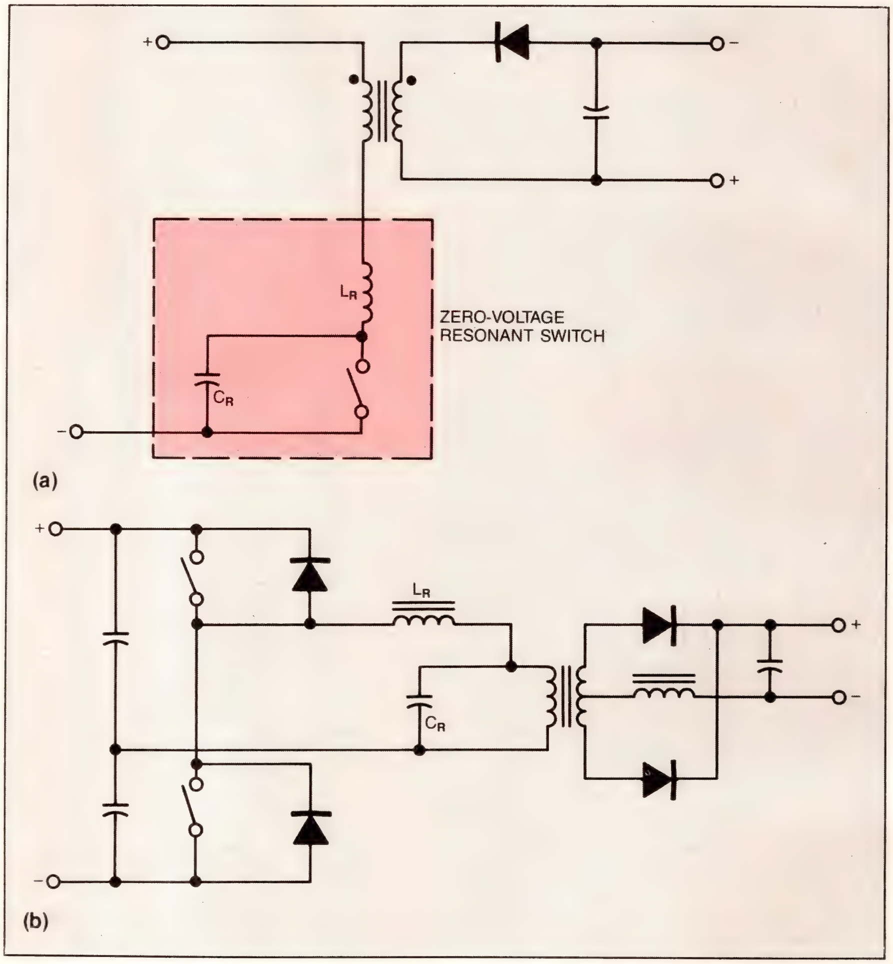


Fig 3—Both of these basic converter circuits use primary-side series resonance. *The flyback converter* ***(a)*** *is series loaded. The half-bridge converter* ***(b)*** *is parallel loaded.*

the resonant circuit: continuous and discontinuous.

In the continuous mode, the circuit operates either above or below resonance. The controller shifts the operating frequency either toward or away from resonance, using the slope of the resonant circuit's impedance curve to vary the output voltage. But, because the peak currents and/or voltages tend to be very high, this mode of operation is not commonly used.

Discontinuous mode is popular

In the discontinuous mode, the control circuit generates pulses having a fixed on-time, but at a varying frequency determined by the demands of the load. This mode of control—often called *quasiresonant*—does not generate continuous current flow in the tuned circuit and usually operates at a maximum frequency that is below resonance. You can use the discontinuous mode of control with practically all power conversion topologies, including the flyback, forward, and bridge types.

Although many conference papers delivered over the past several years have described the theory and applications of resonant-mode power conversion, it is only recently that designers have had access to cost-effective control circuits that integrate the key functions. Three manufacturers offer these dedicated ICs: Gennum Corp, Cherry Semiconductor, and Unitrode Integrated Circuits.

Gennum Corp (previously Linear Technology Inc) of Canada was the first company to introduce a resonant-mode controller. Gennum's LD405 chip became available about 18 months ago. In June of this year, the firm introduced the GP605—an improved version of the LD405 that's not pin-compatible with the LD405. Both the LD405 and the GP605 are packaged in plastic DIPs and cost $3.76 (1000). The GP605 is also available in an SOIC package for $4.35 (1000).

Cherry Semiconductor, in an exchange agreement for its CS3842A PWM control chip, obtained the manufacturing rights for the Gennum LD405 almost a year ago. Cherry sells its CS3805 version for $3.65 (1000) in a plastic DIP. Many believe that Cherry will also offer a version of the Gennum GP605.

Unitrode Integrated Circuits, an innovative supplier of PWM control chips, introduced its UC3860 family of resonant-mode control chips in June of this year. The UC3860 can supply about four times the drive current and operate at higher frequencies than the devices from Gennum and Cherry. It is also more expensive. In a plastic DIP, the UC3860N costs $11.12 (1000); in a plastic leaded chip carrier, it costs $12.25 (1000).

Resonant-mode conversion

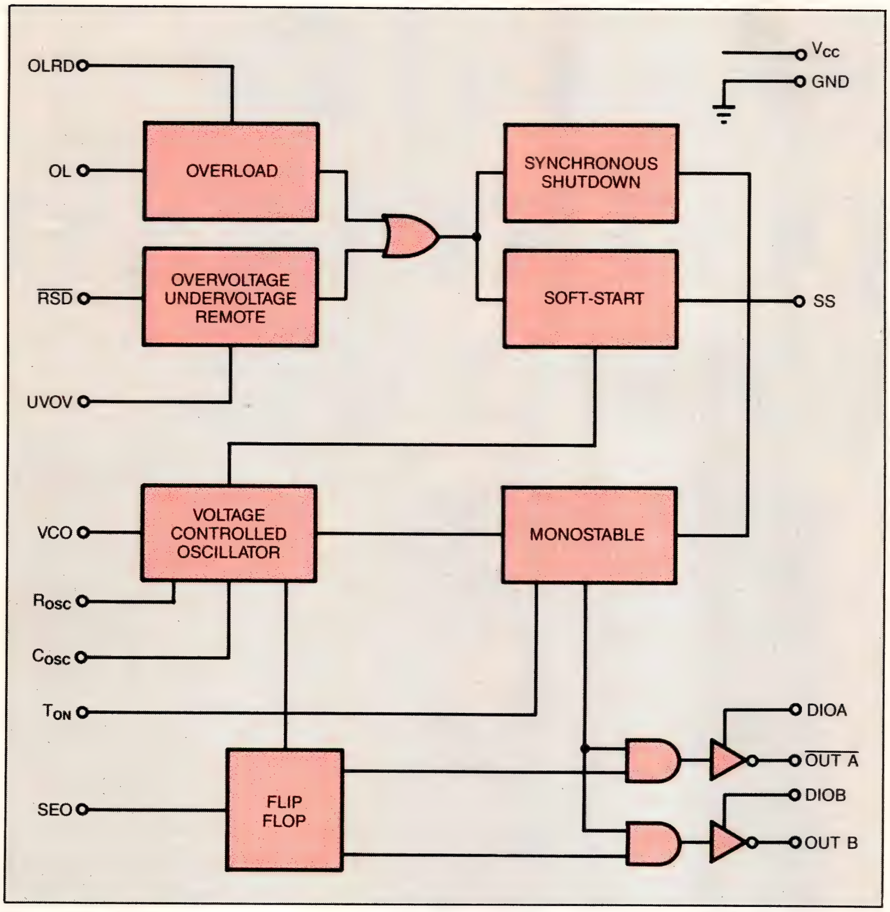


Fig 4—The LD405 resonant-mode controller operates at frequencies to 1 MHz. *The Gennum Corp device is second-sourced by Cherry Semiconductor as the CS3805. Gennum's GP605 is similar but has built-in Schottky diodes, a 5V reference, and a special power-ground pin.*

Although varying in detail and complexity, all of these resonant-mode control chips provide the same basic functions. All contain a VCO that varies the operating frequency, a monostable circuit that establishes the pulse on-time, and a steering circuit that determines the output drive mode (single ended or complementary). The chips also provide many of the same basic protection features—such as soft-start, undervoltage lockout, and overload protection—albeit in different ways and with varying degrees of sophistication.

Devices operate to 1 MHz

The Gennum LD405 (**Fig 4**) and the Cherry CS3805 are pin-compatible and electrically equivalent devices. With these chips, the pulse width is held constant while the frequency is varied over the operating range. The chips feature a drive-current capability of 200 mA, a frequency range of 10 kHz to 1 MHz, synchronous overload shutdown with delayed restart, synchronous overvoltage/undervoltage protection with remote shutdown, a soft-start function, and single-ended or complementary outputs that can drive power MOSFETs.

The operating frequency range (min and max) of the LD405 is set by an external resistor and capacitor at the VCO pins. A monostable circuit sets the T_{on} time (pulse width) via an external parallel-connected resistor and capacitor.

Although you can set the maximum frequency of the LD405 as high as 1 MHz, internal delays limit the maximum duty cycle. For example, at $F_{max}=1030$ kHz and $T_{on}=500$ nsec, the maximum duty cycle is 51.6%. At $F_{max}=394$ kHz and $T_{on}=2000$ nsec, the maximum duty cycle is 78.9%. Because energy conversion takes place only during the on-time, the duty-cycle limitation lowers the practical F_{max} value.

You can change the output drive of the LD405 via the SEO pin. Grounding this pin enables a flip-flop that controls the output AND gates, sending the drive to $\overline{\text{OUT A}}$ and $\overline{\text{OUT B}}$ in a push-pull mode. Opening the SEO pin puts the chip into the single-ended mode. In this mode, the frequency is doubled in comparison with that of the individual outputs in the push-pull mode. Because the outputs are identical in the single-ended mode, you can connect them in parallel for increased drive capability. The on-time is independent of the mode of operation.

Among the other features of the LD405 is an overvoltage/undervoltage (OVUV) window comparator that you can set externally. The soft-start function provides a relatively slow change from the minimum VCO frequency to the value set by the VCO input. The soft-start initiates with each start-up, as well as after any forced shutdown. Shutdown is achieved either by grounding the remote shutdown pin (RSD) or by applying a voltage in excess of 3.2V to the overload pin (OL).

Each time the overload block shuts down the chip, it does so in a *hiccup* mode that lasts from 0.5 to 2 seconds; the exact timing is set by an external capacitor at the OLRD pin. This type of overload protection is especially effective on prolonged overloads—the converter still automatically recovers

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Resonant-mode conversion

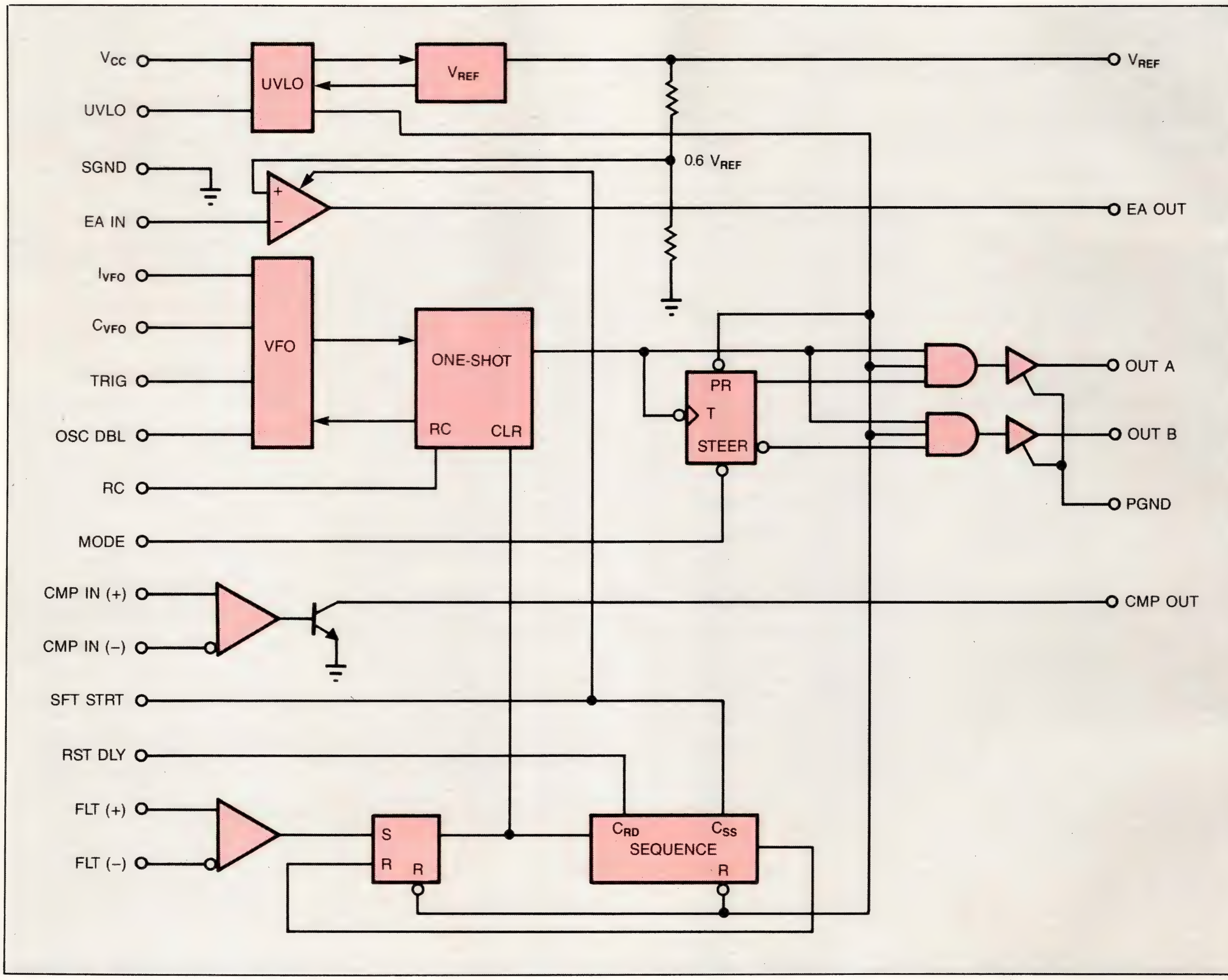

Fig 5—The UC3860 resonant-mode chip operates at frequencies to over 2 MHz. *The Unitrode device can supply 2A (peak) of drive current to a power MOSFET. In addition to the standard functional blocks and protection features, the UC3860 contains an on-chip error amplifier and an uncommitted comparator.*

once the voltage on the OL pin drops below the threshold level.

Because every shutdown in the LD405 is synchronous with the monostable circuit, the controller never interrupts T_{on} in the middle of a pulse. This feature is particularly important for resonant power supplies because an interruption in the resonant cycle might cause excessive voltage spikes, which could damage the semiconductor switching devices.

Gennum provides an excellent 25-page application note on the operation of the LD405, which includes both the theory of operation and a schematic for a 125W resonant-mode power supply. Gennum's GP605, although essentially identical to the LD405, has some subtle but important differences. The GP605's frequency range extends from 1 kHz to 1.2 MHz, compared with 10 kHz to 1 MHz for the LD405. The GP605 also features on-chip Schottky diodes; a special power-ground pin; and an internal 5V regulator, which is brought out to external pins. Because of these differences, the LD405 and GP605 are not pin compatible.

The basic architecture of the UC3860 **(Fig 5)** from Unitrode is similar to the LD405 and GP605 from Gennum and the CS3805 from Cherry. Each of these devices contains essentially the same functional blocks and protection features, although the implementaion varies. The difference between the UC3860 and the other three lies not so much in function as in performance.

For example, the UC3860 can operate at a maximum frequency of at least 2 MHz, compared with 1 MHz for the LD405 types. The UC3860 provides 800 mA of output-

Resonant-mode conversion

drive current, compared with 200 mA for the other devices. And the UC3860's low propagation delays permit a duty cycle of over 90% at a frequency of 1 MHz and about 78% at 3 MHz. More important, the UC3860 can handle peak currents of 2A, and its 24-pin DIP has a dissipation rating of 1.25W at an ambient temperature of 50°C. The Cherry/Gennum 16-pin devices are rated at 900 mW at 50°C.

What also sets the UC3860 apart from the other chips is an error amplifier and an uncommitted comparator. The on-chip error amplifier has a typical unity-gain bandwidth of 5 MHz ($R_{IN}=2\ k\Omega$) and an open-loop gain of 80 dB. It can function as a gain block when used with optocouplers to get across the isolation boundary in switching power supplies. Moreover, the error amplifier in the UC3860 works with the chip's VFO to obtain predictable minimum and maximum operating frequencies.

The addition of the uncommitted comparator provides additional versatility. For example, you could use the comparator as an overvoltage

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detector or as a zero-current-crossing detector. You could also use the comparator's open-collector npn transistor to shunt the UC3860's RC pin with a second resistor, causing a reduction in the pulse width of the one-shot timer.

Apparently designed as a *universal* resonant-mode controller, the UC3860 provides higher levels of performance and greater versatility than do the chips from Cherry and Gennum. The major drawback of the UC3860 for many potential users may be its cost, which is about three times that of the LD405/CS-3805 types.

However, Unitrode may not be after the yet-to-be-defined mass market. In contrast to the Cherry and Gennum chips, which are available only in the commercial temperature range (0 to 70°C), the UC3860 is also available in industrial (−25 to +85°C) and military (−55 to +125°C) temperature ranges. Unitrode is a major supplier to the military, and it is here that the UC3860 may find its greatest application—smaller and lighter supplies are continually demanded and cost is not a major factor.

Resonant-mode technology will not soon supplant the PWM techniques used in the vast majority of switching power supplies, but there is a definite trend toward higher operating frequencies in these supplies. Engineers are starting to look at the resonant-mode method of control for this application because it offers higher operating frequencies and has other inherent advantages over PWM techniques. Designers will have a choice of several dedicated resonant-mode chips in their pursuit of power supplies having higher power densities. **EDN**

Acknowledgment

The writer wishes to thank Fred Sykes of Gennum for the information he provided on resonant-mode topologies and for his many helpful comments. Thanks also to Bill Andreycak of Unitrode for his valuable comments on resonant-mode control and on the special features of the UC3860 chip.

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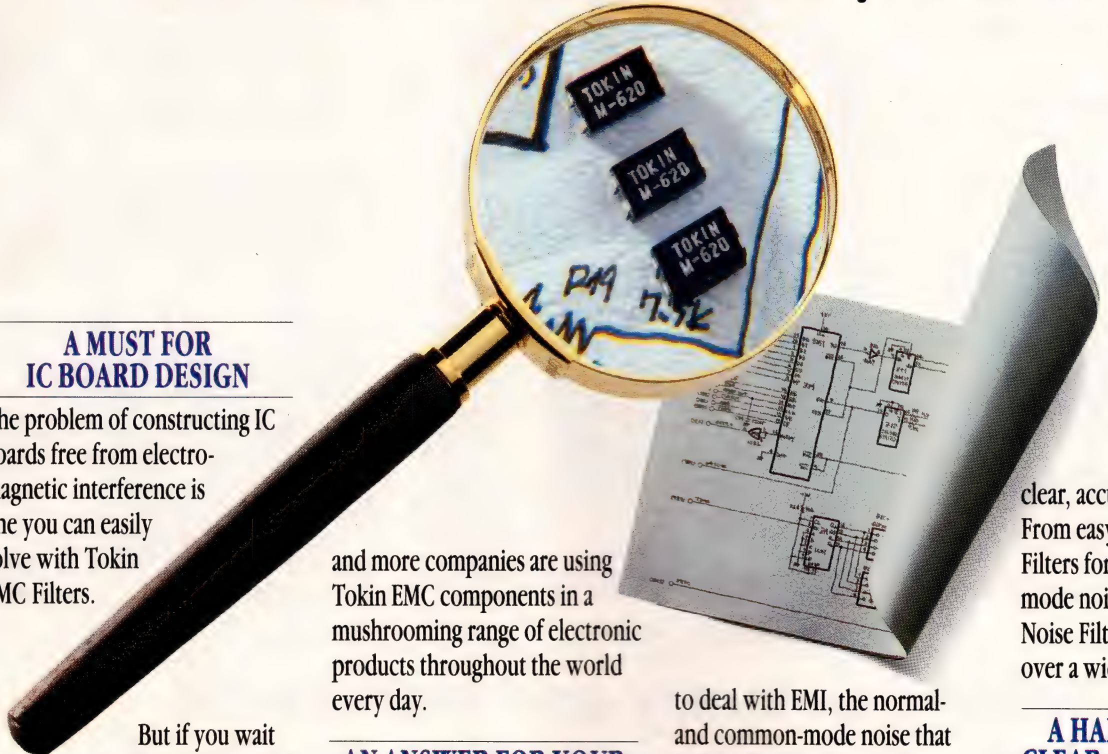

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Specifications (EMC Chip Filters)

Model	Circuit	Frequency Range (MHz)	Impedance (Ω)	Rated Current (mA)
M608	1 circuit; Common-mode	5~200	≧300 (at 100MHz)	100
M614	1 circuit; Common-mode	5~100	≧700 (at 50MHz)	100
M620	1 circuit; Common-mode	5~50	≧1,000 (at 30MHz)	100
M720N	20 circuits; Normal-mode	50~300	≧50 (at 200MHz)	50

Specifications (DIP Noise Filters)

Model	Circuit	Rated Current per Line (mA)
D-03C/ D-03C1	8 circuits; Common-mode	100
D-05N1	8 circuits; Normal-mode	100
D-07C1	8 circuits; Common-mode	300
D-08C2	4 circuits; Common-mode	2,300
D-08C2A	4 circuits; Common-mode	500
D-16C	4 circuits; Common-mode	100
D-20C	8 circuits; Common-mode	500
D-40C	3 circuits; Common-mode	300
D-42C	5 circuits; Common-mode	300
D-45C	8 circuits; Common-mode	300
D-47C	10 circuits; Common-mode	300
D-55C	5 circuits; Common-mode	300
D-58C	8 circuits; Common-mode	300

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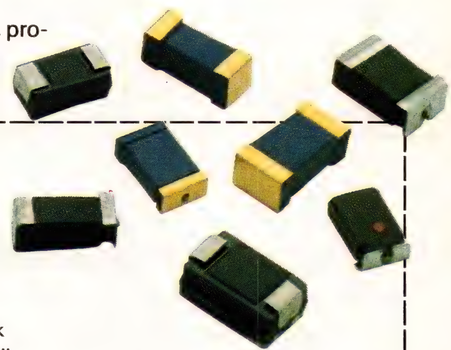

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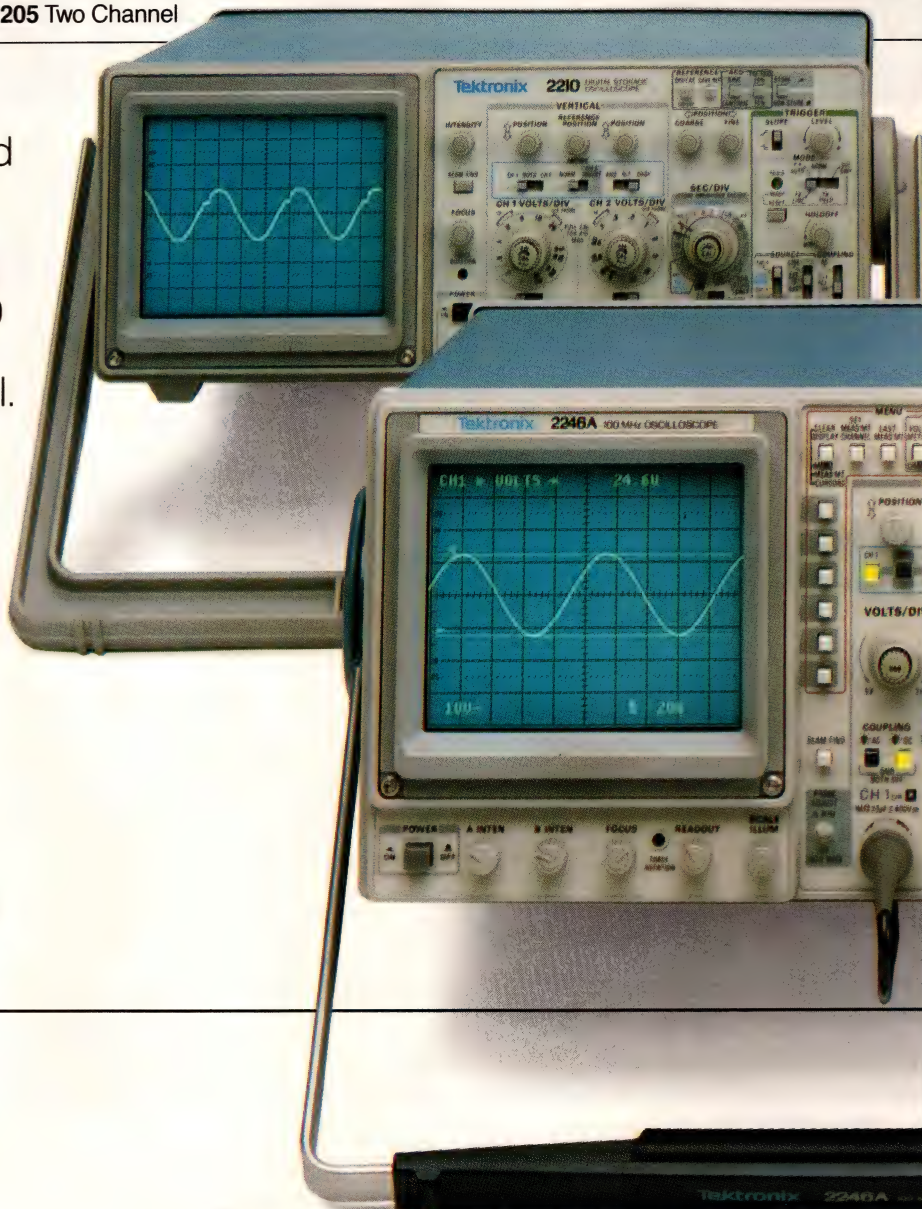

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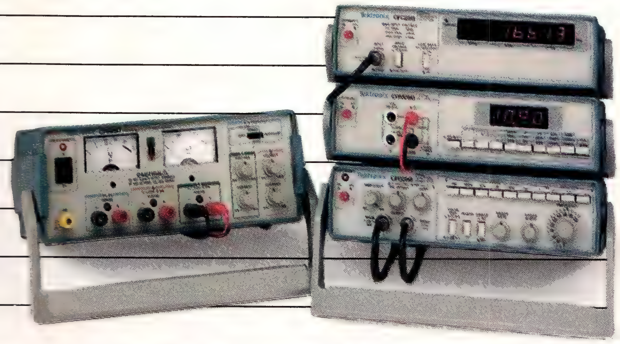

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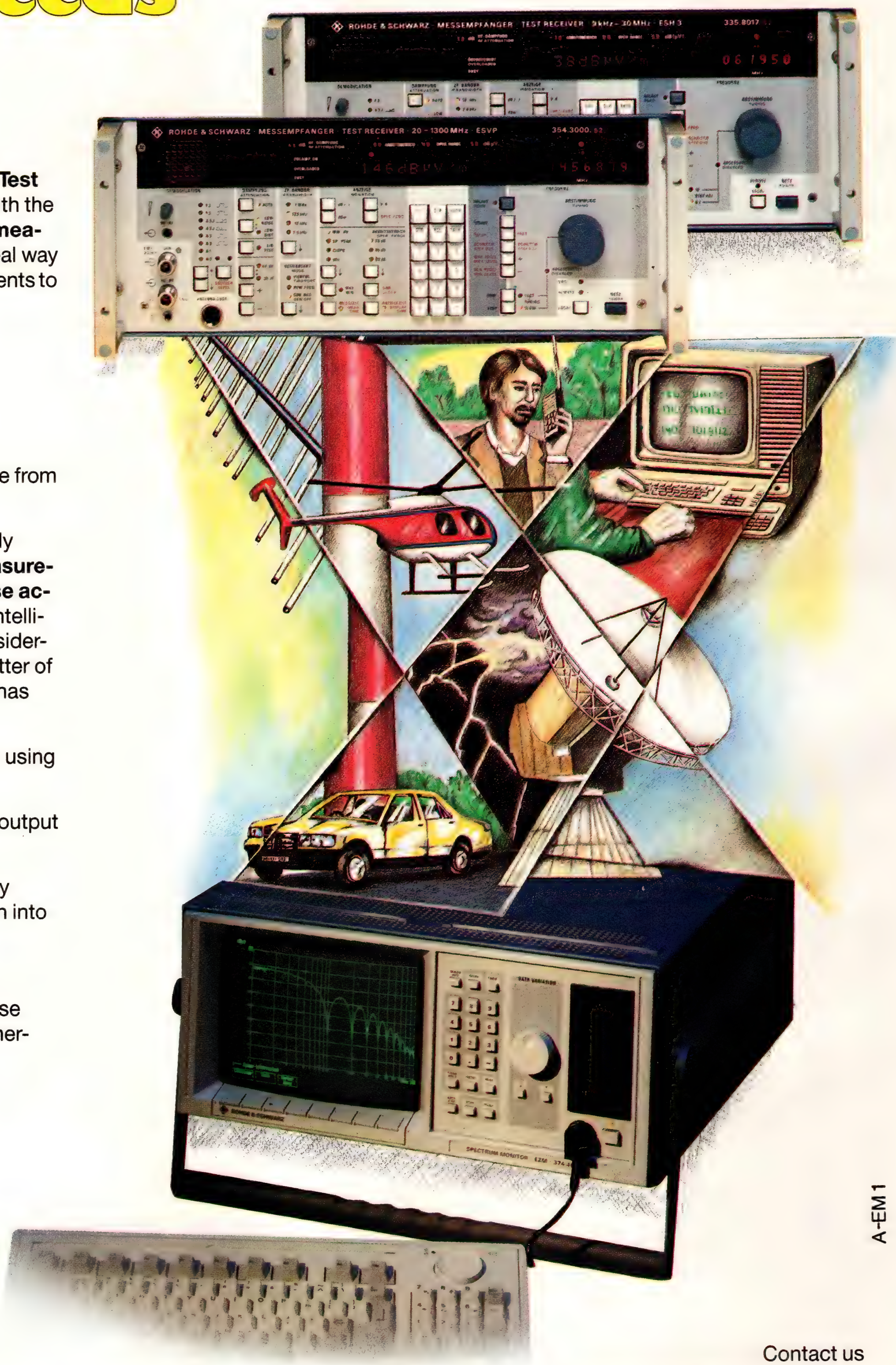
CIRCLE NO 166

EMC-testing to meet your needs



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Erasable programmable logic device offers high density and buried registers

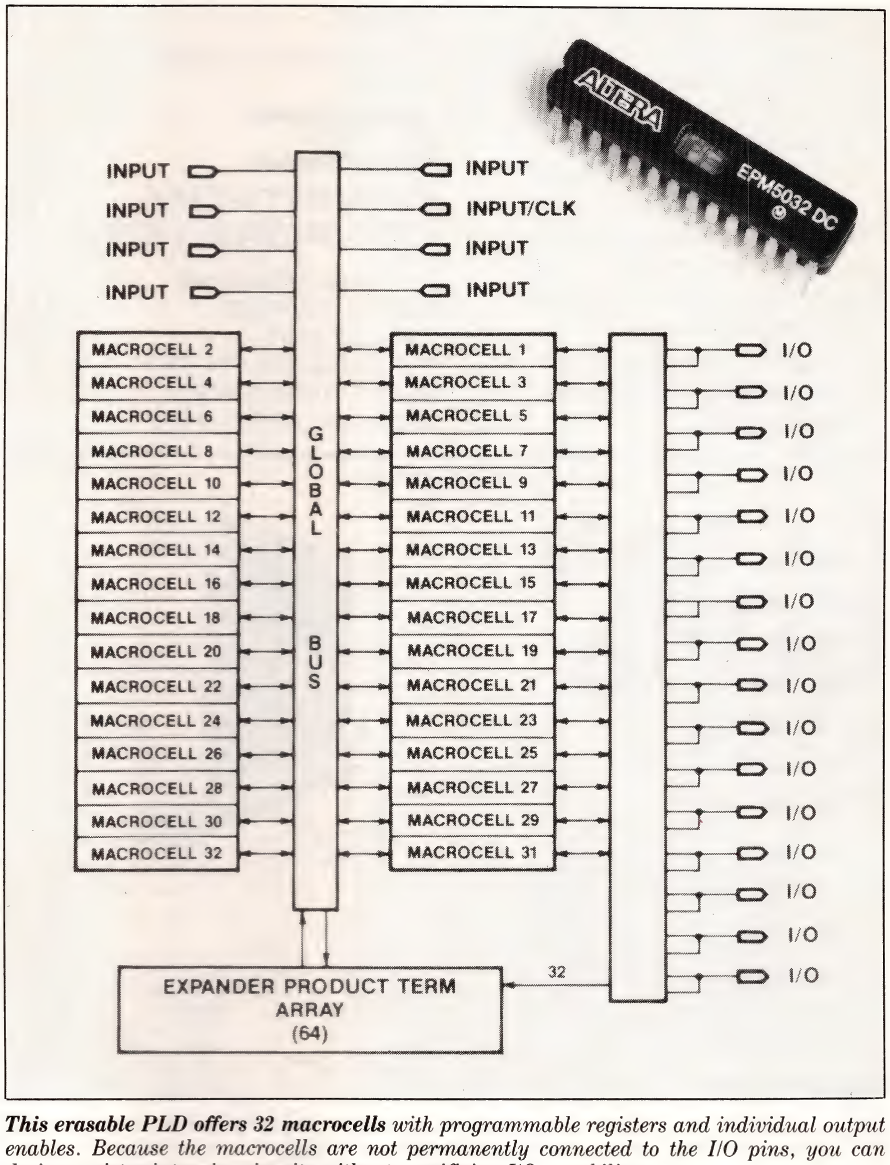
If you're tired of wasting I/O pins on your programmable logic device in order to generate registered delays, consider using the EPM5032 erasable PLD. This device offers 32 macrocells with flip-flops that are not permanently connected to I/O pins.

The EPM5032 is the first member in a series of erasable PLDs based on a multiple-array matrix (MAX) architecture. The key elements of the architecture are its macrocells, an expander product array, and an internal global bus.

The device has 8 dedicated input pins and 16 programmable I/O pins. You can use the programmable pins as dedicated inputs or outputs, or as bidirectional ports. The output of each macrocell is fed back to the internal bus independently of the I/O structure and need not be connected to an output pin, thus allowing you to create buried registers without sacrificing I/O pins.

Each macrocell consists of a programmable register and eight product terms. Three of the product terms form an AND-OR array, which is then XORed with a fourth product term to produce the register input. The XOR gate allows you to control the polarity of the signal to the register.

The other product terms are AND arrays that create the register control signals. You can configure the register in each macrocell as a D-, T-, JK-, or SR-type flip-flop or bypass it altogether. You can select either a system clock or a product term to clock the register, use product terms to preset and clear the register's output asynchronously, and use a product term as the macrocell's output enable.



This erasable PLD offers 32 macrocells *with programmable registers and individual output enables. Because the macrocells are not permanently connected to the I/O pins, you can design register-intensive circuits without sacrificing I/O capability.*

You have a wide variety of signals to choose from in forming the macrocell's product terms. Each term has access to the internal global bus, which offers true and complemented forms of the dedicated inputs, the output of each macrocell, the I/O pins, and from 32 to 64 expander product terms. The exact number of expander terms available depends on your I/O usage. For every I/O pin used as

an input, you lose two expander product terms.

The expander product terms are an AND-INVERT array selecting from the same global bus as the macrocell terms. Because the expander term outputs are available as term inputs, you can use the expanders for either combinatorial or registered logic. By cross-coupling terms, you can implement as many as 32 asynchronous latches with the expander.

The device is fabricated in 0.8-μm CMOS EPROM technology. This fabrication results in a propagation delay time (t_{pd}) of 20 nsec and a clock frequency greater than 60 MHz for the highest speed grade. And because the device is erasable, it is 100% tested before leaving the factory.

By taking advantage of its development tools, you can use the device to its fullest capabilities. These tools include a hardware programming module and schematic capture, logic synthesis, and interactive timing simulator software. All the software runs on an IBM PC/AT or PS/2 model 50, and the programming module includes a plug-in interface board for your computer.

The device is available in a 300-mil windowed ceramic 28-pin DIP. A one-time-programmable plastic DIP version will be available in early 1989. The 20-nsec ceramic version costs $31.20; the 25-nsec version sells for $26 (100). The price of the development software and programming hardware is $4995; and the software alone costs $3400.—***Richard A Quinnell***

Altera Corp, 3525 Monroe St, Santa Clara, CA 95051. Phone (408) 984-2800.

Circle No 741

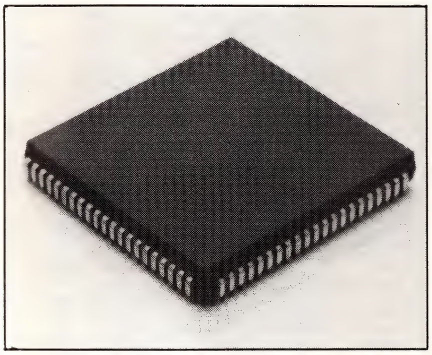
CIRCLE NO 169

Chip integrates eight UART channels and includes token-passing arbitration logic

Eight UART channels, each with 8-character transmit-and-receive FIFO buffers, make the SYC6208P84 IC ideal for applications in multiplexers that require multiple serial-interface channels. The OCTART (8-channel UART) IC supports full-duplex communications on each channel at speeds as high as 38.4k bps. Furthermore, the chip employs channel-arbitration and interrupt-prioritization logic based on token-passing concepts.

An on-chip microcontroller handles the internal operation of the OCTART. Each OCTART channel includes an 8-character-deep transmit-data FIFO buffer, an 8-character-deep receive-data FIFO buffer, and an 8-deep, 3-bit receive-status FIFO buffer. The status FIFO buffer stores 3 bits of information such as good transfer, parity error, or overrun, corresponding to each character in the receive FIFO buffer. In addition, you can program each channel to automatically recognize four user-specified characters. The OCTART flags recognition of one of the characters via the status FIFO buffer.

The 8-character-deep transmit-and-receive FIFO buffers offer a performance edge when compared with UARTs that have 2- to 4-character-deep FIFO buffers. For example, during receive operations you can program the OCTART to interrupt only the controlling CPU after receiving 5, 6, 7, or 8 characters. Therefore, the deeper FIFO buffer results in fewer CPU interrupts and more characters transferred per interrupt. The chip also includes a time-out feature on each channel, ensuring that all channels are serviced within a reasonable amount of time.



Eight UART channels with deep FIFO buffers *make the 84-pin-PLCC OCTART IC suitable for use in multiplexers that require multiple serial-interface channels.*

An external controlling µP communicates with the OCTART via on-chip RAM-based registers that are dual ported between the on-chip microcontroller and the external data bus. The external µP can read status information from and write control information to the registers. In addition, the µP can write to the input location, and read from the output locations of each channel's FIFO buffers.

You can program the parameters of each channel independently—in fact, you can program a single channel for different send-and-receive baud rates. Other programmable parameters include 5- to 8-bit word lengths, 1 or 2 stop bits, and odd-, even-, no-, or force-parity operations. The status registers provide information on the incoming DSR (Data Set Ready), CTS (Clear To Send), and CD (Carrier Detect) modem signals for each channel.

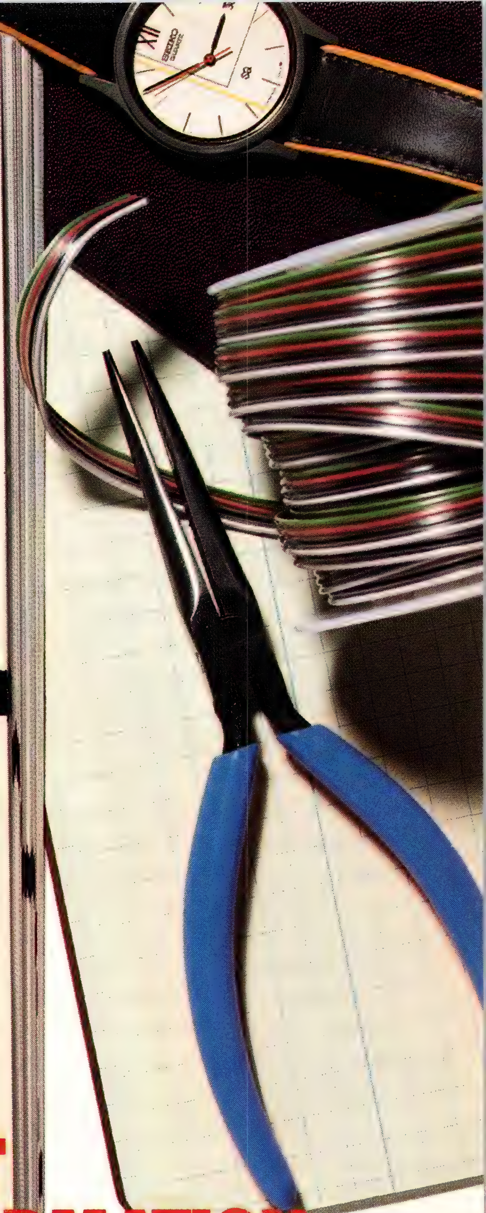
The on-chip channel-arbitration and interrupt-prioritization logic employs three token-passing loops to ensure that all OCTART channels are serviced on a rotating basis. The token passes to each channel, and only while holding the token can a channel interrupt the controlling µP. The three separate token paths separately prioritize, transmit, receive, and modem-change operations.

In each loop, the eighth channel passes the token physically outside the IC via an output signal. For single OCTART applications, you must tie the token-output signal to the IC's token-input signal, thereby passing the token back to the first channel. You can also cascade multiple OCTART chips by connecting the token-output signal of one chip to the token-input signal of the next chip. The token-output signal of the last OCTART in the chain must be reconnected to the token-input signal of the first OCTART.

The OCTART IC consumes less than 0.5W and is packaged in a CMOS 5V-only PLCC. The chip costs $61 (1000) and will be available in volume by the end of the year.—***Maury Wright***

Systech Corp, 6465 Nancy Ridge Dr, San Diego, CA 92121. Phone (619) 453-8970. TLX 4990407. FAX 619-453-0238.

Circle No 743



ANALOG DEVICES

15μV max Offset Voltage Ultralow Drift Op Amp

AD707

FEATURES
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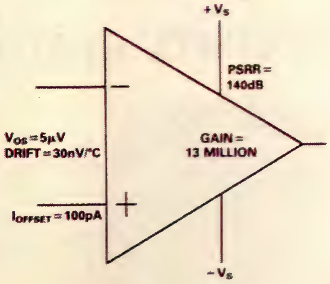
- **8V/μV min Open-Loop Gain**
- **0.32μV/V max CMRR**
- **1μV/V max PSRR**
- **1nA max Input Bias Current**
- **1nA max Input Offset Current**

Dual Version Available: AD708



PRODUCT DESCRIPTION

The AD707 is a low cost, high precision op amp with state-of-the-art performance that makes it ideal for a wide range of precision applications. The offset voltage spec of less than 15μV is outstanding for a bipolar op amp, as is the 1.0nA maximum input offset current. The top grade is the first bipolar monolithic op amp to offer a maximum offset voltage drift of 0.1μV/°C, and offset current drift and input bias current drift are both specified at 25pA/°C maximum.

The AD707's open-loop gain is 8V/μV minimum over the full ±10V output range when driving a 1kΩ load. Maximum input voltage noise is 350nV p-p (0.1Hz to 10Hz). CMRR and PSRR are 130dB and 120dB minimum respectively.

The AD707 is available in versions specified over commercial, industrial and military temperature ranges. It is offered in 8-pin plastic mini-DIP, small outline, hermetic cerdip and hermetic TO-99 metal can packages. Chips and Mil Standard/883 parts are also available.

APPLICATION HIGHLIGHTS

1. The AD707's 13V/μV typical open-loop gain and 0.1μV/V typical common-mode rejection ratio make it ideal for precision instrumentation applications.
2. The precision of the AD707 makes tighter error budgets possible at a lower cost.
3. The low offset voltage drift and low noise of the AD707 allow the designer to amplify very small signals without sacrificing overall system performance.
4. The AD707 can be used where chopper amplifiers are required, but without the inherent noise and application problems.
5. The AD707 is an improved pin-for-pin replacement for the OP-07, OP-77 and the LT1001.

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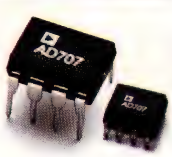

If your analog applications demand precision performance, then you should demand our new AD707 – the world's best dc precision op amp.

The AD707 is the first bipolar monolithic to offer a maximum offset voltage drift of only 0.1μV/°C, and 15μV maximum offset voltage. These features, combined with its ultralow 0.35μV p-p voltage noise, allow the AD707 to amplify extremely small signals without sacrificing system performance.

The AD707 also provides an open-loop gain of 13V/μV, the highest of any precision op amp, and unsurpassed 140dB CMRR and PSRR. So it's ideal for a wide range of precision applications, including instrumentation and automatic test equipment.

All this precision makes it easy for you to work within tight error budgets. And because the AD707 is available at a low cost, you can easily work within your design budget, too.

For an even more accurate description of what the AD707 can do for you, call your nearest Analog Devices sales office.

ANALOG DEVICES

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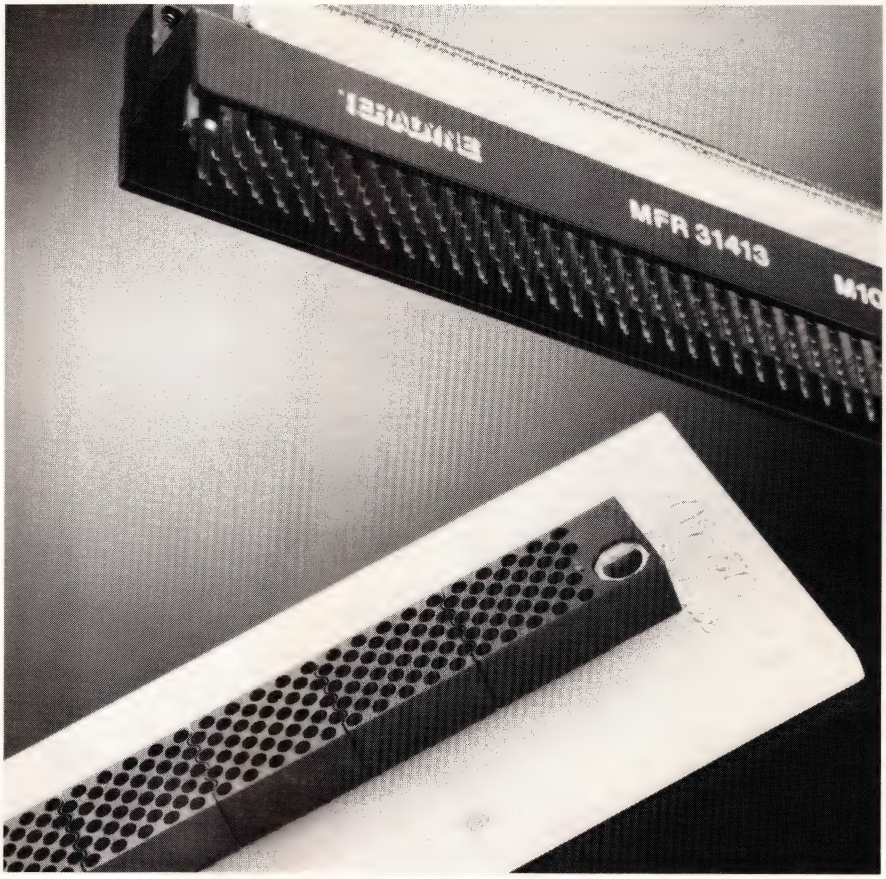
Backplane interconnection system designed for high-density applications

The VHSICon UHD is a complete high-density backplane interconnection system designed primarily for advanced VHSIC-based military/avionic applications. The system includes a controlled-impedance, multilayer, pc-type backplane (KS1050 Series) and a UHD connector system, which consists of a backplane segment and a daughter board segment. The backplane half of the connector mounts via solderless, compliant, press-fit contacts. The bare pc backplane can be designed to contain as many as 30 layers.



Featuring 396 contacts in a body only 5.44 in. long, *VHSICon UHD connectors are designed to accommodate the needs of high-density military/avionics applications.*

Featuring connectors that measure 5.44 in. long × 0.58 in. wide, the VHSICon UHD conforms to the dimensions of SEM (Standard Electrical Module) format E. The connectors employ a miniaturized version of the tuning-fork and blade contact system and provide 396 contacts on a staggered, 8-row, 0.100 × 0.050-in. grid. The contact-grid pattern provides an efficient trace-routing layout on the backplane—a major concern when increased density results in decreased contact-pad spacing.

The daughter board and backplane connectors feature 10 modular sections; each section contains 40 tuning-fork or blade contacts. This modularity not only eases field repair and service problems, but also enables you to easily specify connector arrays that are longer or shorter than 396 contacts (10 sections).

Daughter board connectors are available in two versions: with flexible-circuit terminations (FM1050) or rigid terminations (M1050) at the connector/daughter board interface. In both cases, the terminations are attached to each side of the daughter board using surface-mount techniques. The blade contact is also identical in both versions—only the terminating end that attaches to the module is different.

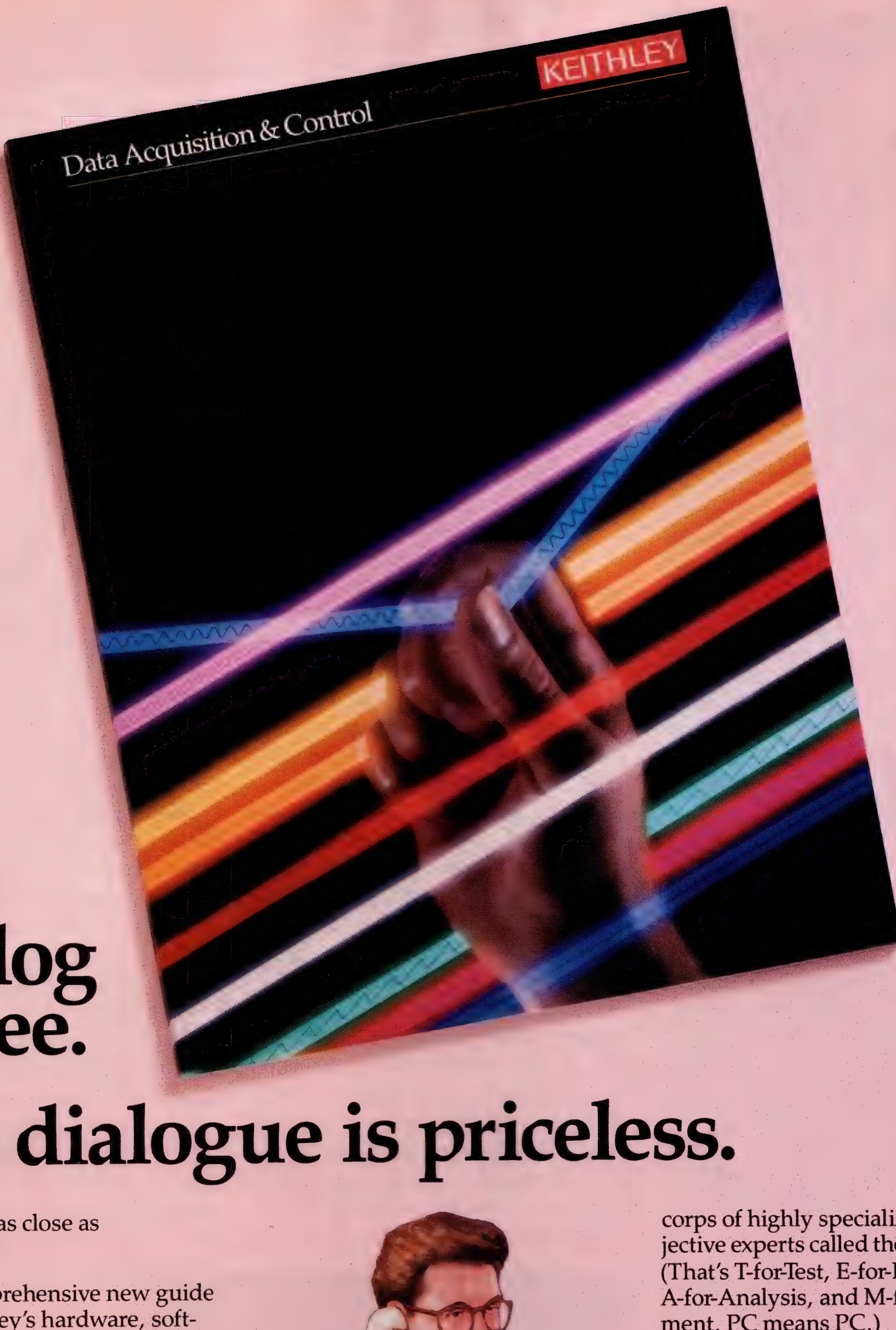
Key specifications of the daughter board and backplane connectors include a continuous current rating of 2A, a voltage rating of 600V, and a contact resistance of 30 mΩ. The connectors operate over −55 to +105°C and feature a contact life (with specified plating) of 500 cycles. The backplane and daughter board are constructed of beryllium copper and brass, respectively. The daughter board's body is made of extruded aluminum 6061-T6, and the contact plating consists of 50 to 70 μ in. of gold over 100 to 250 μin. of nickel.

VHSICon UHD connectors accept size 16 coaxial and/or size 16 or 20 fiber-optic contacts. Depending on your specifications, the manufacturer configures the connectors with or without these special contacts. The connectors are supplied as part of the complete interconnection system. Excluding the backplane, the connectors cost $1 to $2 per mated line.

—Tom Ormond

Teradyne Connection Systems Inc, 44 Simon St, Nashua, NH 03060. Phone (603) 889-5156. FAX 603-889-8185.

Circle No 740



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Data Acquisition & Control Division, Keithley Instruments, Inc.

KEITHLEY

CIRCLE NO 171

Drive weighs 8.5 oz and offers 100M-byte capacity

The BP-100 Winchester disk drive employs a single platter with two recording surfaces to store 100M bytes of formatted data. Targeting laptop and portable computers, the 3½-in. drive consumes less than 1W. The drive's closed-loop voice-coil actuator offers a 29-msec average seek time.

With no metal frame or controller, the drive stands 0.7 in. high and weighs 8.5 oz. Many applications of compact drives call for mounting the plastic-encased HDA (head-and-disk assembly) and controller separately. The HDA includes metal only in the motor assemblies. A metal frame adds 0.5 oz and makes the BP-100 compatible with the standard 3½-in. form factor.

The drive consumes less than 1W of power when operating continuously. The company also plans to reduce power consumption to approximately 0.5W in the near future by offering a power-down mode. The power-down mode conserves power by removing power from the drive during periods of inactivity.

You can choose from SCSI (Small Computer Systems Interface) or IBM PC/AT controllers for the drive. Both controllers employ RLL data encoding and a 7.5M-bps read-channel data rate. The drive spins the platter at 1600 rpm. A sector servo and the voice-coil actuator result in the 29-msec average seek time. Worst-case seeks require 45 msec, and the drive specs 5 msec for track-to-track seeks.

The drive achieves the 100M-byte capacity with a track density of 1720 tpi and a recording density of 57,000 bpi. The thin-film heads fly over glass-substrate sputtered media at less than 5 μin.

You can operate the hermetically sealed drive in 0 to 95% humidity. The drive can withstand a 100g shock without sustaining damage and can operate during 1g vibration. The operating temperature ranges from 0 to 45°C.

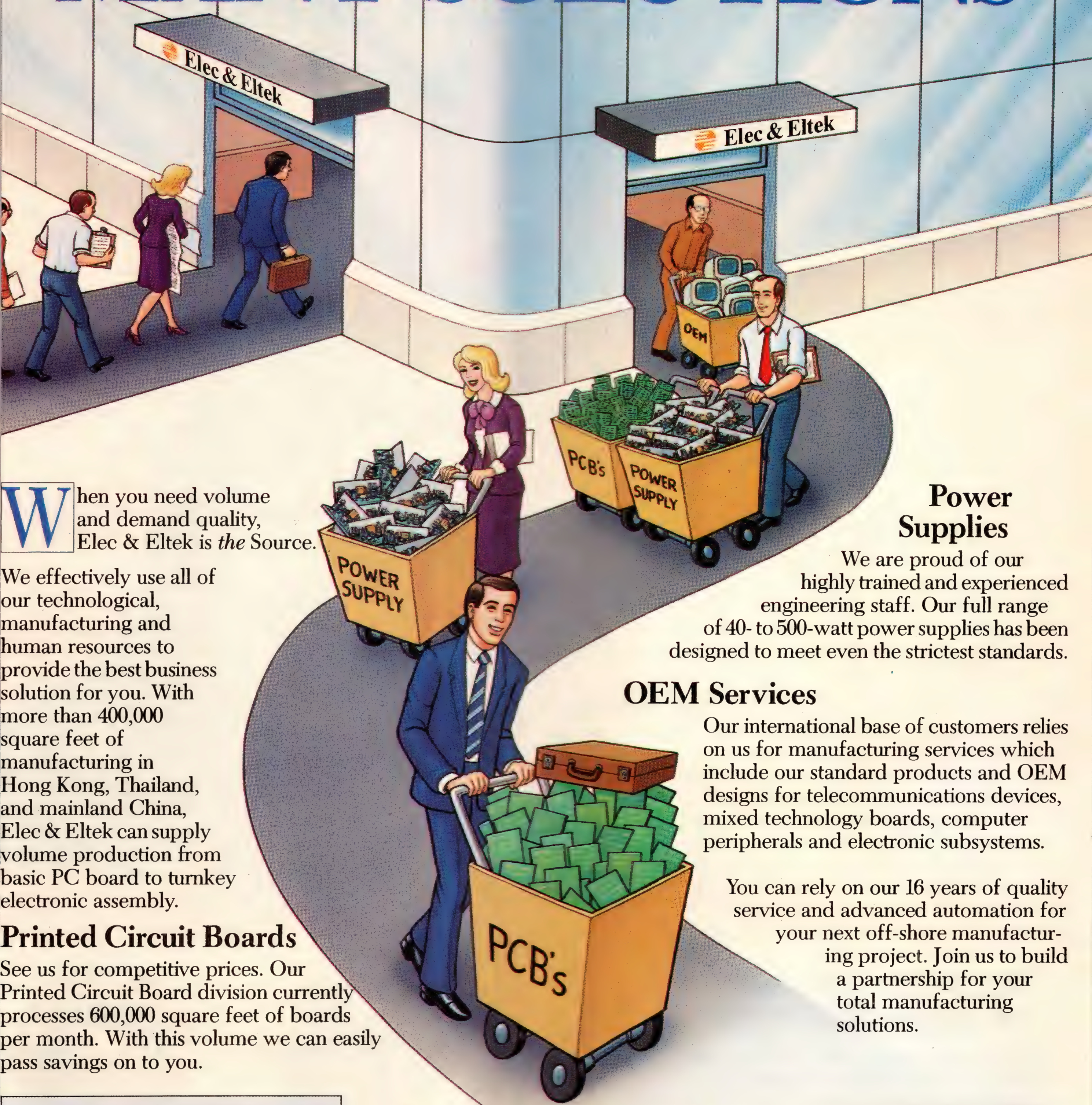
With controller included, the BP-100 costs $595 (1000). The drive will be available in volume at the beginning of the year.—***Maury Wright***

Areal Technology Inc, 3050 Scott Blvd, Santa Clara, CA 95054. Phone (408) 970-8536. FAX 408-970-0884.

Circle No 742

Consuming 1W during continuous operation, *the 8.5-oz 100M-byte BP-100 disk drive is suitable for use in laptop and portable computers.*

ONE SOURCE MANY SOLUTIONS



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CIRCLE NO 172

FOR FURTHER INQUIRIES, PLEASE WRITE TO:

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Sam Shine, Proprietor

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Samtec people believe that our customers deserve the finest products and services. Whatever you need—catalogs, samples, cross-reference guides, quotations, shipment dates—you'll get SUDDEN SERVICE that other vendors can't (or won't) match. Give us a try. You won't be disappointed.

Bobbi Smith
Sales

Brian Thurston
Engineering

This keyboard only *feels* expensive.

FKB4700 Series Keyboards

If you design PCs and workstations, you know how users like the crisp, clean feel of a tactile keyboard. But you also know hard it is to justify the added cost.

Now there is a way to specify a tactile keyboard — and save money, too. Just choose the new FKB4700 keyboard from Fujitsu.

Unique switch makes the difference

Only Fujitsu's FKB4700 keyboards incorporate a unique coil spring, rubber dome switch design. This design combines the simplicity of a membrane keyboard with a full 20-gram tactile response. And it's reliable: over 10 million keystrokes — per key.

Compatible with industry standards

FKB4700 keyboards are available in standard 101- and 102-key layouts. Custom layouts, too. And all are UL478, CSA220 and FCC approved. So, make your customers happy — and your accounting department, too.

Ask your Fujitsu representative for complete information and specifications on the FKB4700, the tactile keyboard that only *feels* expensive.

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CIRCLE NO 176

DESIGNING POWER SUPPLIES
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HAS GIVEN
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A VIEW FROM THE TOP.

At Computer Products, we are committed to understanding the needs of our customers. No other power supply company is so sensitive to the issues that are central to you. And no other power supply company is so responsive to those issues. Computer Products. Your partner in power.

THE GLOBAL RESOURCE YOU NEED.

Over 1900 people throughout North America, Europe and Asia. $100 million in power supply sales. And 187 distributor locations worldwide—the strongest distributor network of power supply products in the world.

It means one-stop shopping. It means reliable, scheduled delivery anywhere, anytime. And it means a resource you can depend on from Minneapolis to Munich.

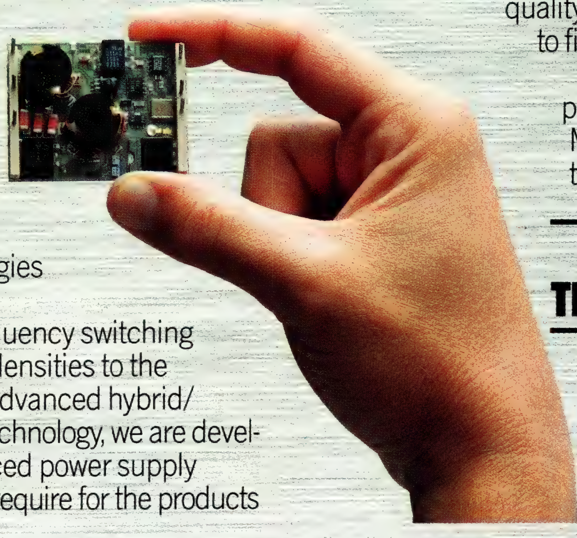
THE STANDARD AND CUSTOM PRODUCTS YOU WANT.

A major benefit of Computer Products is that we are the source for the industry's widest selection of power supply products.

Open frame linears, open frame switchers, encapsulated power modules, cased switchers, high-power switchers, and DC/DC converters. Including a wide selection of Mil-Spec switching power supplies and DC/DC converters. 2400 standard models to choose from—plus modified standard or custom versions which are derived from our proven designs.

POWER SUPPLY TECHNOLOGY THAT PUTS YOU AHEAD.

Computer Products concentrates on the big picture in power supply technology. You benefit from products that are precision-engineered using the most advanced and reliable technologies available.



From high frequency switching and high-power densities to the industry's most advanced hybrid/surface-mount technology, we are developing the advanced power supply designs that you require for the products of tomorrow.

QUALITY AND RELIABILITY YOU CAN TRUST.

It's part of our total company commitment to being a world class manufacturer. We believe in never-ending improvement in the quality of our products and processes. From Statistical Process Control (SPC) through Just-In-Time (JIT) production we are improving every phase of the manufacturing process.

Unlike many power supply companies, our offshore manufacturing facilities are our own. Not those of hard-to-control subcontractors. Our uniform worldwide quality standards can be strictly controlled from start to finish by our own program of quality at the source.

We deliver an unrivaled level of reliability in power supply performance. Including units with MTBF's over 400,000 hours and conformance to the stringent Mil-Q-9858A requirements.

COST OF OWNERSHIP THAT IMPROVES YOUR PROFIT.

Designed-in reliability, attention to scheduling requirements and exceptional after-sale servicing. All natural outgrowths of our awareness of the critical issue of cost of ownership.

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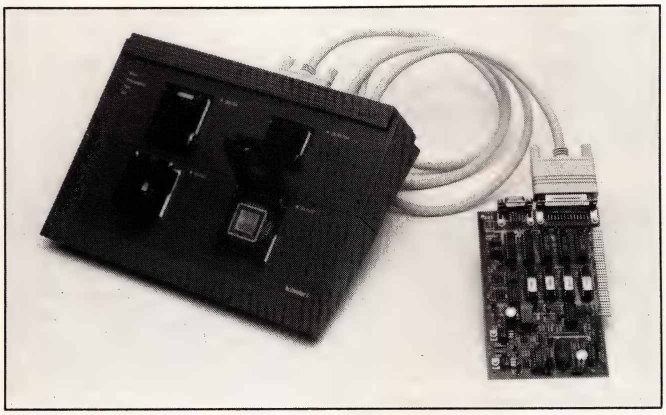
CIRCLE NO 178

READERS' CHOICE

Of all the new products covered in EDN's **July 21, 1988,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, refer to the indicated pages in our **July 21, 1988,** issue, or use EDN's Express Request service.

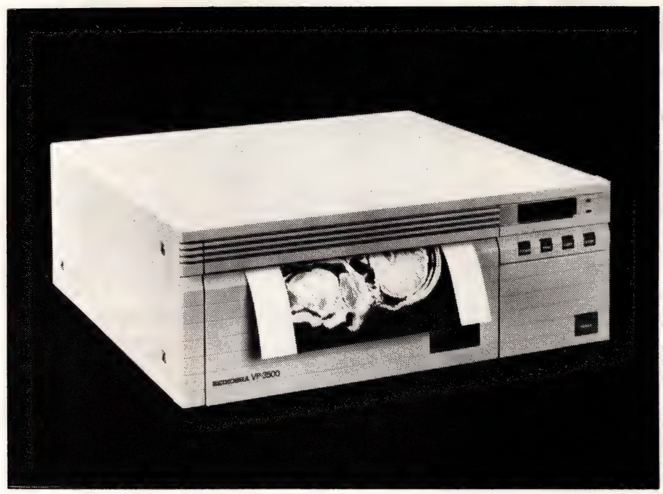


▲ PROGRAMMABLE GATE ARRAYS

The ACT1 Series features two one-time-programmable gate arrays. The ACT1010 has 1200 gates that are equivalent to the gates in standard gate arrays, and the ACT1020 features 2000 of those gates. To use the ACT1 chips, you need the manufacturer's Action Logic System. (pg 58)
Actel Corp.
Circle No 601

PRESSURE TRANSDUCER

Model XT silicon-based pressure transducer is fully compensated over 10 to 85°C and is calibrated to an accuracy of ±0.25%. (pg 142)
Data Instruments Inc.
Circle No 602

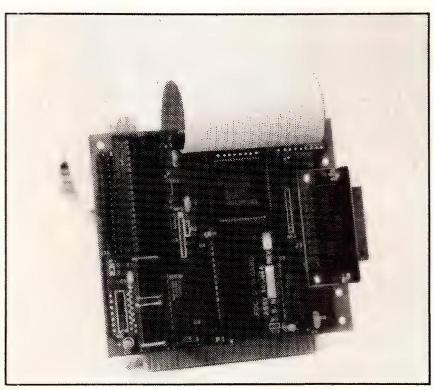


▲ VIDEO PRINTER

The VP-3500 video printer provides 1280×1250 pixels of resolution at 300 dots/in. with a 64-tone gray scale on 8½-in.-wide thermal-print paper. (pg 230)
Seikosha America Inc.
Circle No 603

CAD PACKAGE

The Resicalc CAD program for IBM PCs and compatible systems allows you to design semicustom resistor networks and provides dial-up access to quotations, delivery information, and order-placement facilities. (pg 163)
Ericsson
Circle No 605
Ericsson Components
Circle No 606



◀ SCSI CONTROLLER CARD

The SM911 SCSI controller card for IBM PC and PC/AT buses controls as many as seven serially chained floppy-disk drives or hard drives providing as much as 2.8G bytes of storage. It measures 4×4½ in. (pg 270)
Tega Technologies Inc.
Circle No 604

Plessey - Unsurpassed Process Technology

As system design becomes more and more challenging, and product life cycles become increasingly shorter, design flexibility and getting it right the first time have become critical factors in gaining and maintaining that maximum performance edge you've been looking for.

Plessey's investment in advanced process technology is unequaled in the industry. Successive reductions in feature size and continued improvement in process techniques are at the heart of leading-edge Plessey products.

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Plessey - The Ultimate in ASIC Technology

Our broad range of ASIC products has grown to the point where we are now able to meet all the needs of ASIC users. We offer a full ASIC product range with a variety of options for digital, analog and mixed analog/digital applications, in gate arrays, standard cells, and full-custom. Advanced, state-of-the-art processes in fine geometry, high-density CMOS, bipolar and ECL technologies give you the highest levels of performance and system integration available today.

Plessey - Unparalleled CAD Support

The Plessey Design System (PDS) is a comprehensive suite of software embracing the design, simulation and implementation of gate arrays, standard cell and compiled ASICs in CMOS and bipolar technologies.

Customers who want to use their own CAD workstations or simulators are accommodated by flexible design interfaces at various stages into PDS.

Plessey - Standard Products And Discrete Components

Plessey's standard product family offers the highest performance product range available in the world today. Capabilities range from CMOS DSP devices operating in excess of 20MHz to the world's most advanced 1.3GHz monolithic log amplifier.

High performance solutions are also offered in radio communications, digital

ce that gives you the edge.

PLESSEY KEY PROCESS TECHNOLOGY

BIPOLAR

DESCRIPTION	Ft	EMITTER WIDTH	METAL LAYERS
Industry standard	400MHz	14μm	1
High voltage	200MHz	20μm	1
High speed linear	4.5GHz	4μm	2
High speed digital	6GHz	3μm	2
Ultra-high speed	14GHz	0.6μm	3

MOS

PROCESS FAMILY	fCLOCK	MINIMUM FEATURE	VSUPPLY
KC Industry standard CMOS	20MHz	4μm	3-10V
JG Double SiGate NMOS	10MHz	6μm	9-18V
VB High speed CMOS	40MHz	2μm	3-5V
VJ Very fast CMOS	50MHz	1.5μm	3-5V
VQ Ultra fast CMOS	75MHz	1.2μ	3-5V

BIPOLAR (CDI)

PROCESS	EMITTER WIDTH/ FEATURE SIZE	GRID PITCH	MAX. SPEED	MAX. POWER	MIN. POWER
ORIGINAL CDI	5μm				
CDI FAB I	3.75μm	11.5μm	10ns	2.4pJ	1.5pJ
CDI FAB IIa	2.5μm	8μm	4ns	1.2pJ	0.8pJ
Geometry change (utilizing multi-level differential logic-DML)					
CDI FAB IIb	2.5μm	8μm	800ps	0.8pJ	0.54pJ
CDI FAB III	1.5μm	6μm	400ps	0.4pJ	0.27pJ
CDI FAB IV	1.2μm	4.5μm	200ps	0.2pJ	0.14pJ

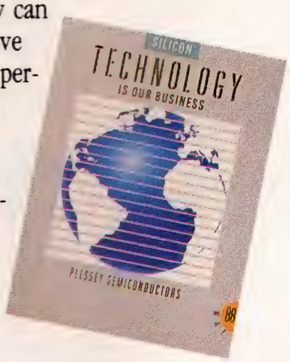
frequency synthesis, data conversion, telecommunications, data communications and consumer products.

Complementing the standard IC family, Plessey manufactures a complete line of discrete components including FETs, transistors and diodes available in SOT-23 and TO-92 packages.

Plessey - Over Two Decades Of Quality Commitment

For more than 20 years, Plessey Semiconductors has been commited to supplying the latest technology, highest quality, and highest performance semiconductor products in the industry. With our unique combination of CAD support, major advances in process technology, and the most advanced research facility in the world, Plessey Semiconductors is, today, a totally commited leader in the industry.

To learn more on how Plessey can help you achieve the maximum performance that gives you the edge, send for our new comprehensive, full color, 72-page short form brochure, or call Plessey Semiconductors today.



In North America call 1-800-441-5665.
Outside North America call 44-793-726666.

For further information you can write to us at one of the following addresses:

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1500 Green Hills Road
Scotts Valley, CA 95066
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Plessey Semiconductors Ltd.
Cheney Manor, Swindon
Wiltshire SN2 2QW
United Kingdom

PLESSEY

Number 1 for **ASICs**

CIRCLE NO 179

"At LTX we evaluated a lot before we chose Vicor."

"As the leading manufacturer of automatic test equipment for linear integrated circuits, we had unique power supply requirements for Hi.T, our new linear test system. Given its advanced resource per pin architecture, we needed new solutions. So we went to the experts. And Vicor delivered.

They delivered a DC power module which lets us achieve low system noise, thus allowing our test equipment to measure signals down to microvolts.

The high power density of Vicor's modules provides us more space for instrumentation. Our systems are smaller, and we can more easily distribute power supplies throughout the system.

They delivered a power system that's modular, flexible and reliable. We can add new features to our testers without having to redesign the power distribution system. And high reliability is especially important to us since we offer a limited lifetime warranty on our test systems.

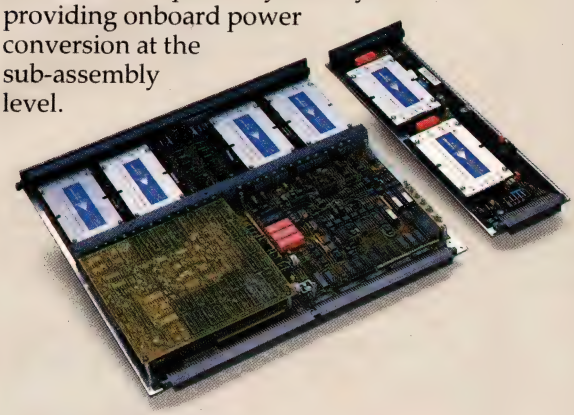
At LTX, our test systems are designed to be flexible. To stay competitive, we're prepared to test semiconductors that are not yet designed. The flexibility of Vicor's power supply is an important ingredient in LTX's role in meeting tomorrow's test challenges."

– Phil Perkins, Staff Scientist,
Co-Founder, LTX Corporation

# of power supply solutions

Distributed Power

Advanced system manufacturers are taking advantage of the inherent benefits associated with distributed power systems. Through the use of component level power converter modules, designers are able to effectively decentralize the traditional power system by providing onboard power conversion at the sub-assembly level.



Rear panel of the Hi.T system

The Component

The building block for distributed power is the Vicor VI-200 series of "zero-current-switching", component level, DC/DC converters.

The Benefits:

- Maximum cost effectiveness
- Minimum time to market
- Minimum inventory
- Reduced size
- Efficient power busing
- Modularity
- Flexibility in system configuration
- Enhanced reliability

To discuss your power system requirements, call Vicor today at (508) 470-2900, 23 Frontage Road, Andover, MA 01810.

VICOR CORPORATION

Component Solutions For Your Power System

CIRCLE NO 180

SIEMENS

Top performance – in a void

Siemens vacuum relays for high frequencies and extra high loads

The contacts of our metal-ceramic relays work effortlessly in a vacuum – in nothing. Dielectric strength is ten times greater than in the atmosphere, because sparking and corrosion are zero in this nothing. Vacuum relays have high currents firmly in their grip, whether switching under very high load or transmitting in an RF system.

Small dimensions but big performance: the benefits you get with the VR100, VR300 and VR400 type families from Siemens. Not forgetting superior features like

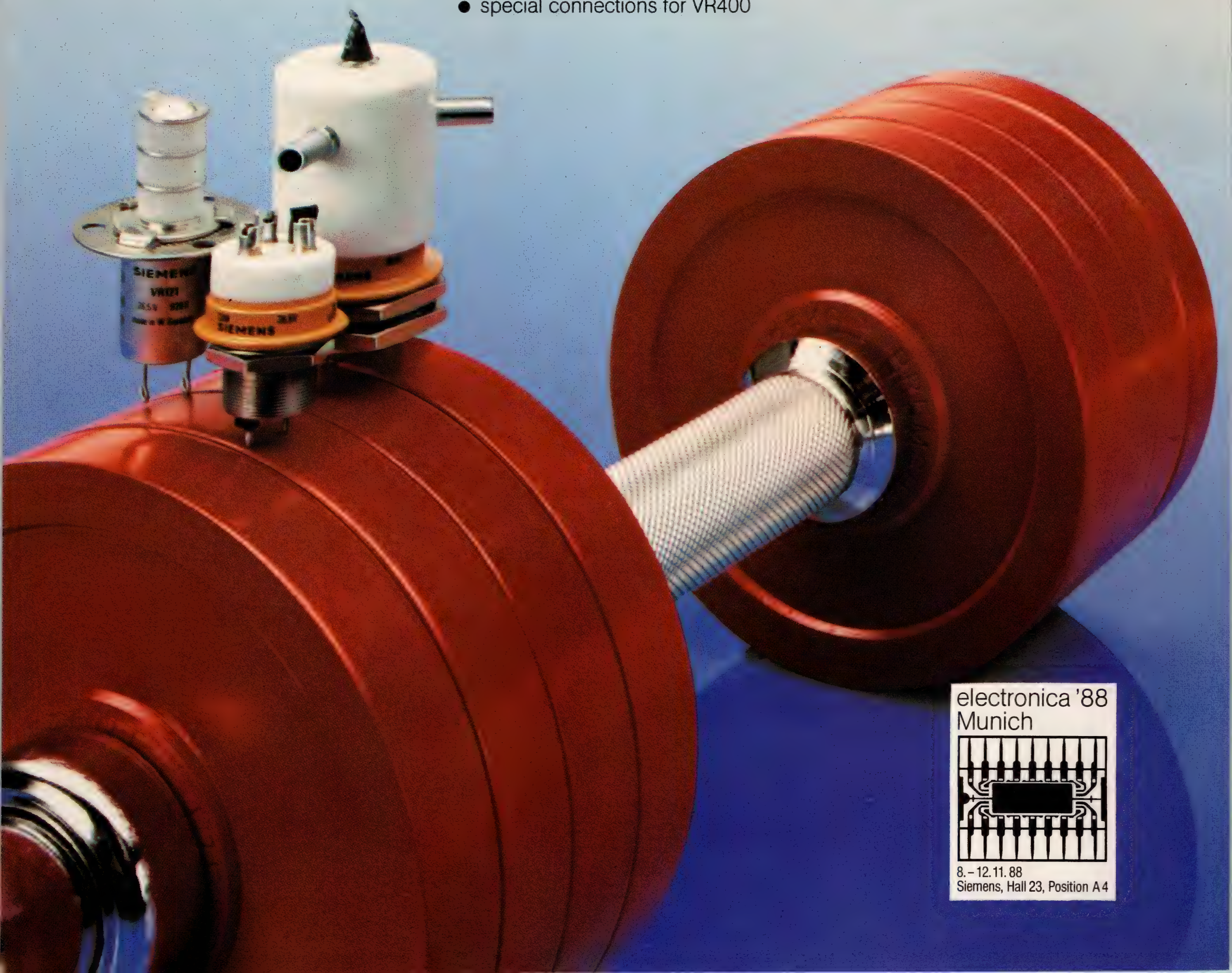
- voltage range up to 15 kV (vacuum relays for 30 kV are upcoming)
- VR100 series with latching actuator (due soon for VR300/VR400)
- 12-V coil for VR300 and VR400
- special connections for VR400

Think there may be one for you? Just write Siemens AG, Infoservice-B-Z076, Postfach 2348, D-8510 Fürth, West Germany quoting "Vacuum relays".

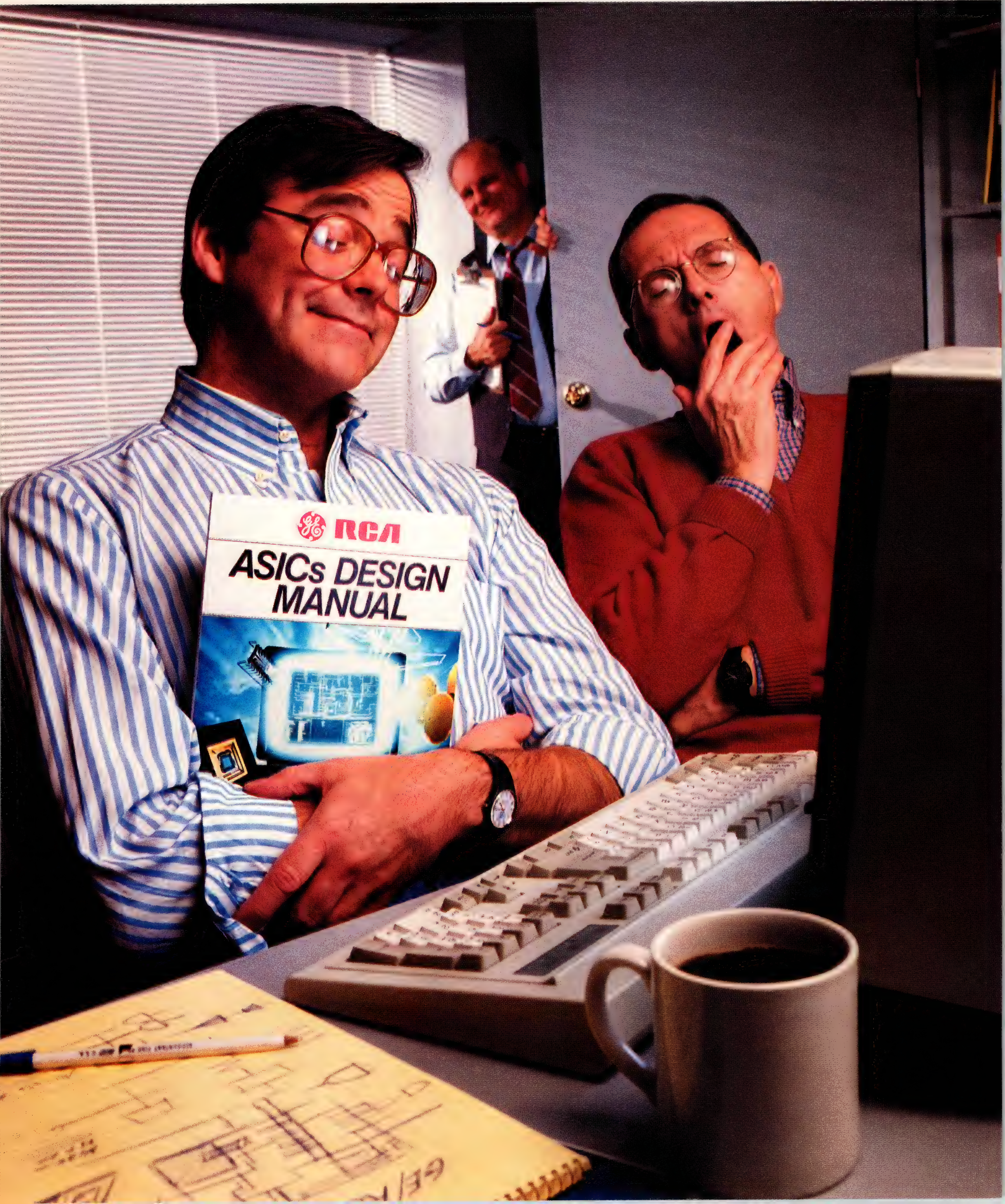
TopTech Components: Siemens

CIRCLE NO 182

A19100-B-Z076-x-7600



Our ASICs



are boring.

They're easy to design. They're ready on time. And first-time success is virtually 100%.

You've heard all about the excitement of ASICs.

They improve performance, lower costs and make many new designs possible.

But, unfortunately, you've probably also heard about one big potential problem: while many ASICs pass the tests specified by the designer, they don't always work in the real world. And that causes excitement you can do without.

How to get first-time success.

It starts with our Design Simulation Software. It's been rated the best in the industry by the people who should know—designers who have used it. Within three days, you can be up to speed, working at any of the major workstations in the industry, creating and revising your ASIC with ease.

The standard cell advantage.

You'll really appreciate the power of our standard cells, which allow you to integrate a whole system, including macros, memories, logic and peripherals, onto a single chip.

We have cells with effective gate length as small as 1.5μ (.9μ coming soon). And double-level metal for higher-density chips that can handle higher clock speeds.

You can choose from a wide range of Supercells, including the leading-edge RS20C51 core micro, RAMs, analog functions, bit-slice processors, HC/HCT logic, Advanced CMOS Logic, and high-voltage cells.

If they aren't enough, we can even generate Supercells to your specs.

And we're also in the forefront of silicon compiler technology. So we can offer you the ability to create designs that are heavily BUS-structured, with your ROMs, RAMs, PLAs and ALUs compiled right into the design.

We also bring you the resources of some very powerful partners, thanks to our alternate-source agreements with VLSI on standard cells; WSI on macrocells and EPROMs; and a joint-development agreement with Siemens and Toshiba on the Advancell® library of small-geometry cells.

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If gate arrays are better for your design, you'll be able to choose from our full line up to 50,000 gates, with effective gate length as small as 1.2μ and sub 1 ns gate delays.

These gate arrays use "continuous gate" technology for up to 75% utilization. They are an alternate source to VLSI Technology arrays.

We also alternate source the LSI Logic 5000 series.

And we have a unique capability in high-rel ASICs, including SOS. Our outstanding production facilities here in the U.S. produce high-quality ASICs in high volume at very low costs.

It almost sounds exciting for something so boring, doesn't it?

For more information, call toll-free today 800-443-7364, ext. 25. Or contact your local GE Solid State sales office or distributor.

In Europe, call: Brussels, (02) 246-21-11; Paris, (1) 39-46-57-99; London, (276) 68-59-11; Milano, (2) 82-291; Munich, (089) 63813-0; Stockholm (08) 793-9500.

GE/RCA/INTERSIL
SEMICONDUCTORS

LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	0	15	54	31	0	0	9.5	8.7
Pot-Core	0	15	54	31	0	0	9.5	10.5
Laminate (power)	6	33	44	17	0	0	7.1	8.4
CONNECTORS								
Military panel	33	34	33	0	0	0	3.6	9.2
Flat/Cable	20	27	46	7	0	0	5.5	5.4
Multi-pin circular	14	43	14	29	0	0	6.9	9.5
PC (2-piece)	20	30	40	10	0	0	5.6	6.4
RF/Coaxial	11	33	33	23	0	0	7.1	7.0
Socket	24	52	18	6	0	0	3.9	6.6
Terminal blocks	13	60	20	7	0	0	4.4	4.9
Edge card	7	36	50	7	0	0	6.1	5.6
D-Subminiature	21	36	36	7	0	0	5.0	4.4
Rack & panel	13	25	49	13	0	0	6.6	7.9
Power	20	40	30	10	0	0	5.1	5.6
PRINTED CIRCUIT BOARDS								
Single sided	8	61	31	0	0	0	4.3	4.9
Double sided	4	35	61	0	0	0	5.9	5.4
Multi-layer	0	21	64	15	0	0	8.0	6.9
Prototype	0	88	12	0	0	0	3.6	3.3
RESISTORS								
Carbon film	39	22	28	11	0	0	4.6	4.8
Carbon composition	50	19	25	6	0	0	3.5	4.9
Metal film	30	25	35	10	0	0	5.0	4.5
Metal oxide	22	33	33	12	0	0	5.4	5.1
Wirewound	13	31	37	19	0	0	6.8	6.3
Potentiometers	11	33	33	23	0	0	7.1	6.6
Networks	0	50	42	8	0	0	6.1	5.5
FUSES	38	37	19	6	0	0	3.5	3.8
SWITCHES								
Pushbutton	29	21	43	7	0	0	5.1	5.3
Rotary	18	45	10	27	0	0	6.3	6.1
Rocker	27	13	40	20	0	0	6.6	5.7
Thumbwheel	27	19	27	27	0	0	6.9	7.1
Snap action	0	30	40	30	0	0	8.7	6.9
Momentary	13	37	37	13	0	0	6.0	5.1
Dual-in-line	30	30	30	10	0	0	4.8	6.0
WIRE AND CABLE								
Coaxial	13	47	40	0	0	0	4.6	5.1
Flat ribbon	28	44	28	0	0	0	3.5	3.6
Multiconductor	29	36	35	0	0	0	3.8	4.8
Hookup	27	50	23	0	0	0	3.3	3.3
Wirewrap	42	33	25	0	0	0	2.9	3.3
Power cords	11	22	56	11	0	0	6.8	6.0
POWER SUPPLIES								
Switcher	17	33	42	8	0	0	5.5	7.4
Linear	9	45	36	10	0	0	5.7	6.6
CIRCUIT BREAKERS	9	36	28	27	0	0	7.5	8.1
HEAT SINKS	7	53	33	7	0	0	5.3	5.3
BATTERIES								
Lithium coin cells	8	50	33	9	0	0	5.5	5.5
9V alkaline	30	40	20	10	0	0	4.3	3.9
Real-time clock back-up	14	43	29	14	0	0	5.7	6.3
RELAYS								
General purpose	13	49	19	19	0	0	5.9	6.1
PC board	7	43	21	29	0	0	7.4	8.1

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
Dry reed	0	50	25	25	0	0	7.3	8.5
Mercury	0	57	14	29	0	0	7.3	10.8
Solid state	0	45	18	27	10	0	9.5	10.1
DISCRETE SEMICONDUCTORS								
Diode	24	24	28	16	8	0	7.4	5.5
Zener	14	28	24	29	0	5	8.8	5.5
Thyristor	8	31	46	15	0	0	6.9	6.6
Small signal transistor	18	34	24	18	6	0	7.2	5.7
MOSFET	0	54	31	15	0	0	6.4	7.6
Power, bipolar	18	36	27	19	0	0	6.1	6.8
INTEGRATED CIRCUITS, DIGITAL								
Advanced CMOS	6	37	38	13	6	0	7.6	8.1
CMOS	10	32	29	19	10	0	8.7	6.3
TTL	18	40	18	18	6	0	6.9	4.7
LS	18	40	24	18	0	0	5.9	4.9
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	0	45	28	27	0	0	7.7	8.2
OP amplifier	0	43	43	14	0	0	6.9	8.9
Voltage regulator	13	43	25	19	0	0	6.2	6.8
MEMORY CIRCUITS								
DRAM 16K	0	43	0	29	14	14	13.6	12.9
DRAM 64K	0	30	20	30	10	10	12.8	13.8
DRAM 256K	0	30	30	20	10	10	12.0	19.1
DRAM 1M-bit	0	22	12	33	33	0	15.1	19.2
SRAM 4K × 4	0	29	14	43	14	0	12.2	15.3
SRAM 8K × 8	0	17	0	42	8	33	19.2	17.8
SRAM 2K × 8	0	25	0	37	25	13	16.8	15.1
ROM/PROM	9	18	18	55	0	0	10.5	13.7
EPROM 64K	6	31	19	38	6	0	9.8	9.8
EPROM 256K	0	21	29	43	7	0	11.3	13.2
EPROM 1M-bit	17	17	17	49	0	0	9.4	12.8
EEPROM 16K	0	33	17	50	0	0	10.0	12.0
EEPROM 64K	0	25	37	38	0	0	9.5	12.5
DISPLAYS								
Panel meters	10	20	40	30	0	0	8.4	10.8
Fluorescent	0	23	33	44	0	0	10.1	11.0
Incandescent	17	33	17	33	0	0	7.4	10.4
LED	7	36	43	14	0	0	6.6	6.3
Liquid crystal	0	17	33	50	0	0	10.8	9.6
MICROPROCESSOR ICs								
8-bit	8	25	25	42	0	0	9.2	7.7
16-bit	0	49	13	38	0	0	8.4	7.8
32-bit	0	33	17	50	0	0	10.0	11.4
FUNCTION PACKAGES								
Amplifier	11	23	44	22	0	0	7.6	9.5
Converter, analog to digital	10	10	50	30	0	0	8.9	9.1
Converter, digital to analog	14	14	43	29	0	0	8.3	9.5
LINE FILTERS	14	43	14	29	0	0	6.9	6.3
CAPACITORS								
Ceramic monolithic	21	37	21	21	0	0	6.0	5.9
Ceramic disc	26	16	32	26	0	0	7.0	6.9
Film	18	35	12	35	0	0	7.4	6.9
Aluminum electrolytic	11	41	16	32	0	0	7.4	8.0
Tantalum	12	35	18	35	0	0	7.9	8.6
INDUCTORS	0	46	16	38	0	0	8.5	8.1

Source: Electronics Purchasing Magazine's survey of buyers.

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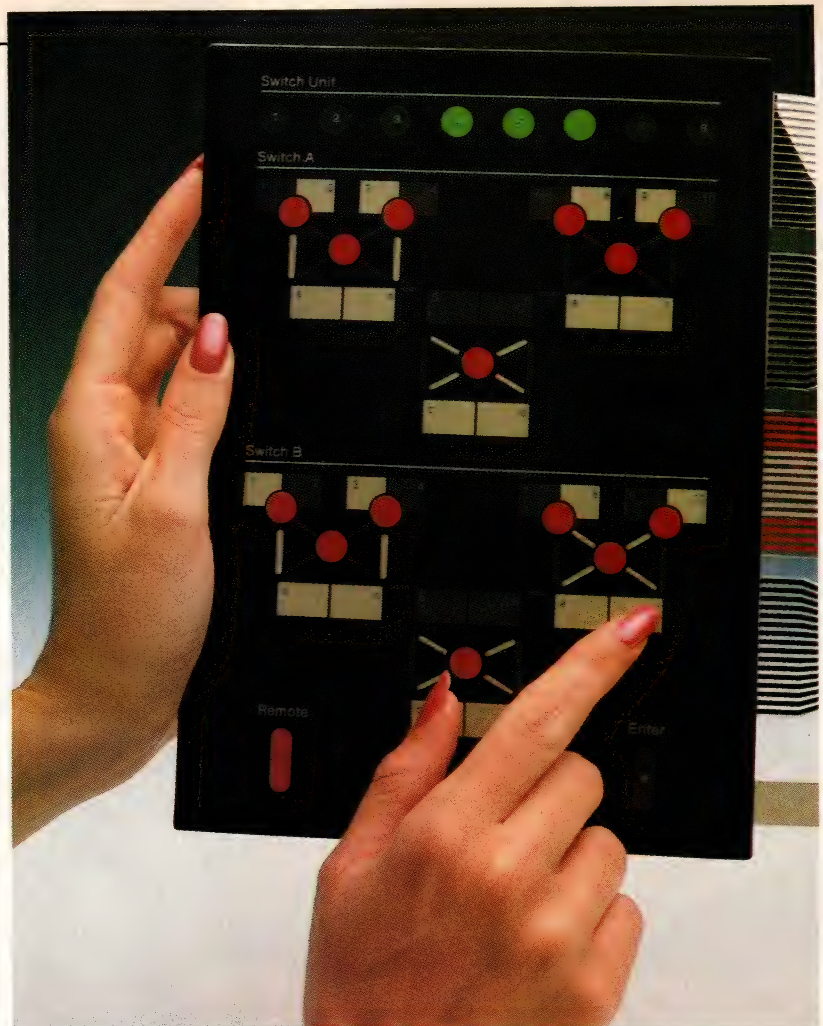
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MT5C2565	64K X 4 $\overline{\text{OE}}$	**25ns**	PDIP, CDIP, SOJ, LCC
MT5C2568	32K X 8	**25ns**	PDIP, CDIP, SOJ, LCC
MT5C6401	64K X 1	**15ns**	PDIP, CDIP, SOJ
MT5C6404	16K X 4	**15ns**	PDIP, CDIP, SOJ
MT5C6405	16K X 4 $\overline{\text{OE}}$	**15ns**	PDIP, CDIP, SOJ
MT5C6406/7	16K X 4 S.I/O	**15ns**	PDIP, CDIP, SOJ
MT5C6408	8K X 8	**15ns**	PDIP, CDIP, SOJ, LCC
MT5C1601	16K X 1	**15ns**	PDIP, CDIP, SOJ
MT5C1604	4K X 4	**15ns**	PDIP, CDIP, SOJ
MT5C1605	4K X 4 $\overline{\text{OE}}$	**15ns**	PDIP, CDIP, SOJ
MT5C1606/7	4K X 4 S.I/O	**15ns**	PDIP, CDIP, SOJ
MT5C1608	2K X 8	**15ns**	PDIP, CDIP, SOJ

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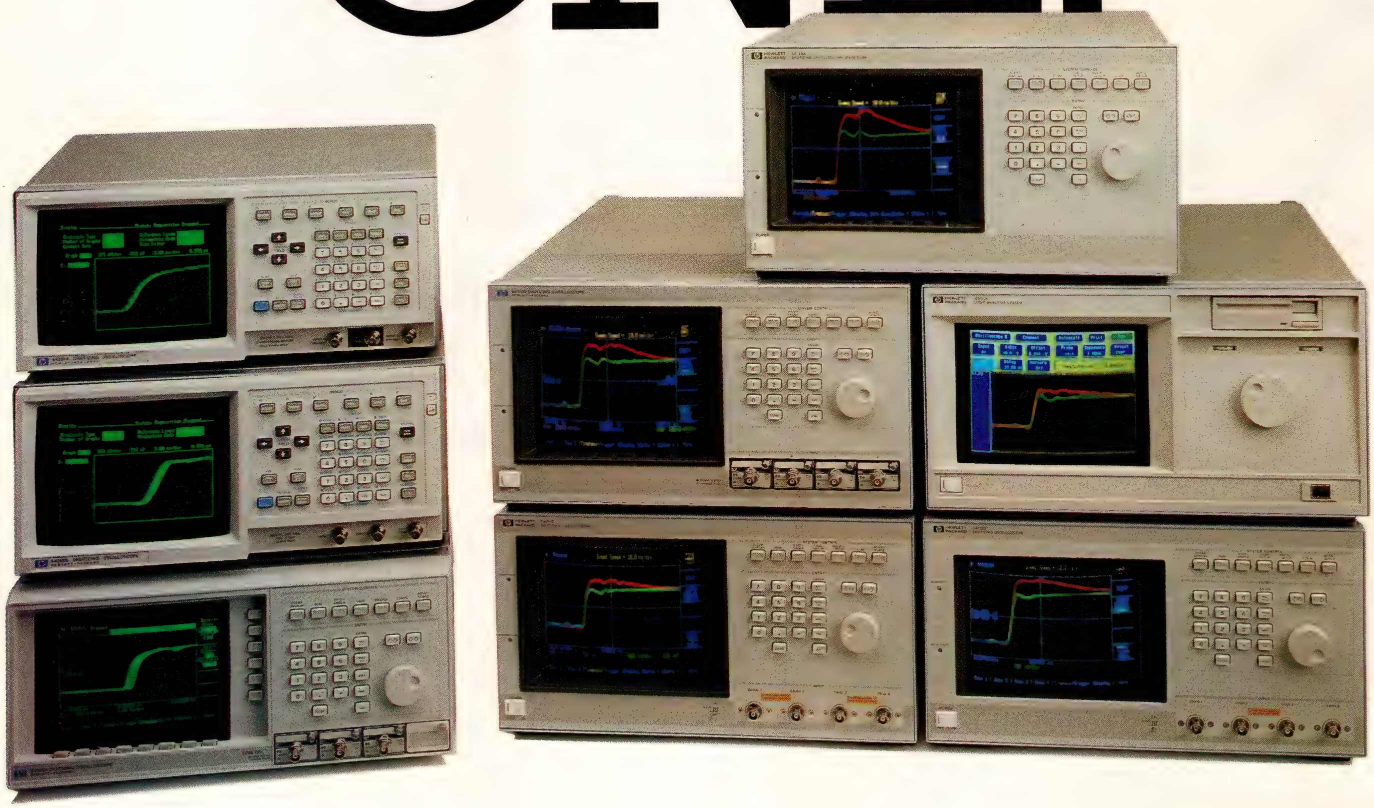

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Programmable Logic Devices

PLD manufacturers have been making waves with large, exotically architectured devices that are lapping at the low end of gate-array applications, but they haven't neglected bread-and-butter 20-, 24-, and 28-pin devices. These more conventional PLDs benefit from a host of detail improvements in speed, semiconductor processing, and architectural enhancements.

Charles H Small, *Associate Editor*

Although programmable logic devices (PLDs) have been around for over a decade, engineers have recently begun to use them at geometrically increasing rates. PLD makers have responded to this surge in demand with a flurry of across-the-board improvements in 20-, 24- and 28-pin PLDs. The improvements include increased speed, advanced processes, architectural enhancements, and lower power.

The biggest news from the PLD front is the dramatic increase in speed that new PLDs offer in comparison with those available just a year ago. Leading the pack in its class of 24-pin devices, with a 7-nsec propagation delay (t_{PD}), is the Gazelle Microcircuits GA22V10-7. Programmed and tested, it sells for $37 (10,000); the 10-nsec version is $35. Fabricated in a MIL-spec and S-qualified GaAs process by Triquint (a Tektronix subsidiary and GaAs foundry), the device has the architecture and programmable output macrocells of the conventional 22V10. Unlike many high-speed devices, the GA22V10 has a preload feature that simplifies device-level testing—especially when you program the PLD as a state machine.

Gazelle also offers the GA22VP10-7, a more flexible version of the GA22V10, for $35 (10,000). This device has a 7.5-nsec t_{PD}. The device is pin and function compatible with the 22V10. In addition, you can set up its output macrocells in configurations that are not possible with the conventional device. For example, the GA22VP10-7's output macrocells can function as bidirectional I/O lines; the 22V10's can be either input or output lines, but not both.

The firm's designers took pains to make the devices usable in conventional circuits. The devices' inputs and outputs are TTL compatible and, unlike those of some other GaAs devices, they operate from a single 5V supply. Their power consumption is 1W—a high figure for a single device, but nevertheless comparable to other high-speed, bipolar, or ECL devices.

Extensive renovations *have led to expanded PLD architectures. (Photo courtesy Exel Microelectronics Inc)*

PLD makers have responded to the surge in demand with a flurry of across-the-board improvements in 20-, 24- and 28-pin PLDs.

The biggest difference between the GA22V10 and a conventional PLD is that the GA22V10's GaAs part is not field programmable. Instead, you must send a JEDEC file for your part to Gazelle, which will program your parts with special laser-trimming equipment. Conventional device programmers can't handle the GA22V10.

Somewhat slower than the exotic GaAs device, and comparable to bipolar 22V10s in speed, is Lattice Semiconductor's CMOS GAL22V10. The device has a 15-nsec t_{PD}. The manufacturer claims that the electrically erasable device typically draws 90 mA.

Now only one speed grade behind bipolar parts, Cypress Semiconductor's CMOS 20-pin 18G8 has a 12-nsec t_{PD} and draws just 80 mA. The UV-erasable device's generic architecture allows you to program it to replace 23 bipolar types. It sports a ninth product term to control each I/O macrocell's output-enable function.

National Semiconductor's new versions of the PAL1016SP4A and PAL10016P4A ECL PALs reduce the t_{PD} to 4 nsec from the 6 nsec of previous versions, and they consume less power than their predecessors do. The two versions are compatible with the 10KH and 100K ECL families, respectively. The PAL1016SP4A costs \$22.75 (100); the PAL10016P4A sells for \$25.94 (100).

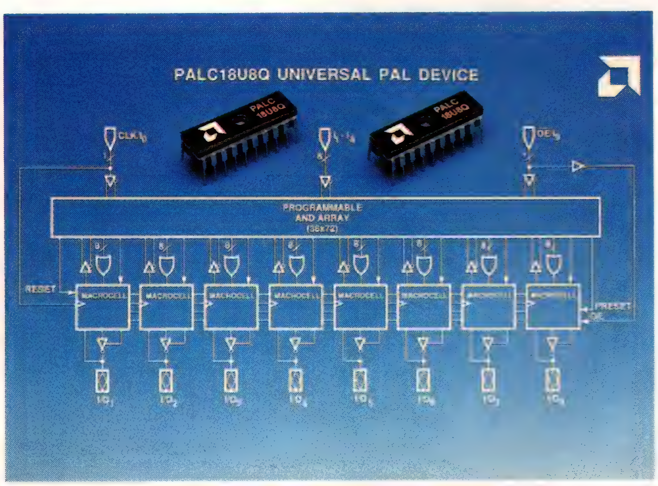
Texas Instruments also offers a fast, ECL version of the 16P8 PLD. The 24-pin TIEPAL10H16P8-6 has a 6-nsec t_{PD} and comes in 10KH and 100K versions. It costs \$19.78 (1000).

Several manufacturers have recently introduced bipolar parts whose blazing speeds rival those of ECL parts. The amazing speed increases in bipolar PLDs amount to a doubling in speed over the past year.

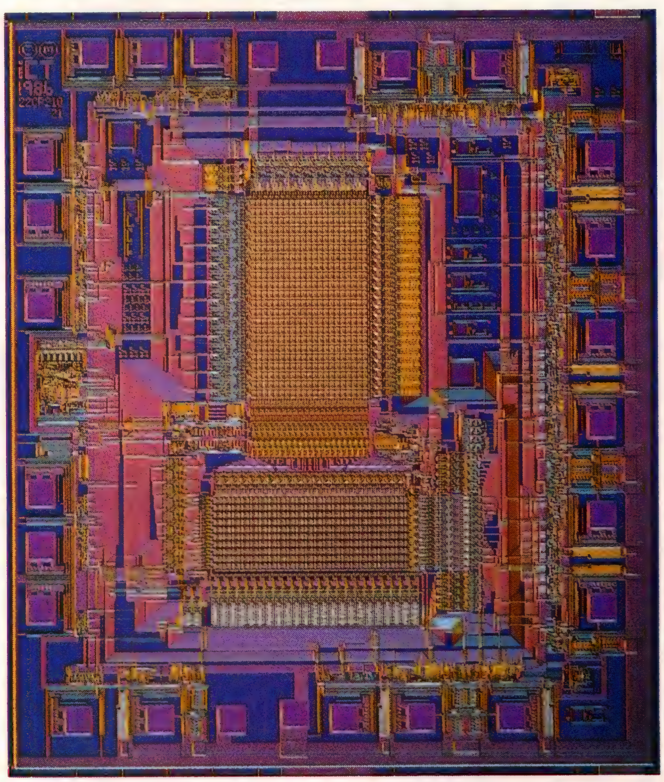
AMD, for example, has enhanced both the speed and the architectural flexibility of PLAs (programmable logic arrays). The PLS105, a 28-pin device, adds buried registers to the conventional PLA architecture; it can therefore realize state machines having 30 to 40 states without requiring off-chip feedback or registers. The device can clock through a sequence of states as fast as 37 MHz, and it costs \$17 (100). The PLS105 is the third member of a new family of fast PLAs that also includes two 24-pin devices, the PLS167 and PLS168.

Signetics, too, has faster versions of its FPLS (field-programmable logic sequencer). The PLUS405 is a superset of the PLS105, which clocks at 33 MHz. It features 16 inputs, eight buried state registers, eight output registers, and 64 state-transition terms. It has two complement-array terms to the PLS105's one. The device dissipates 950 mW and sells for \$9.

AMD's PAL16R8-7 family takes the most common PLDs beyond the speed of conventional TTL. The devices have a 7.5-nsec t_{PD}. The family comprises the



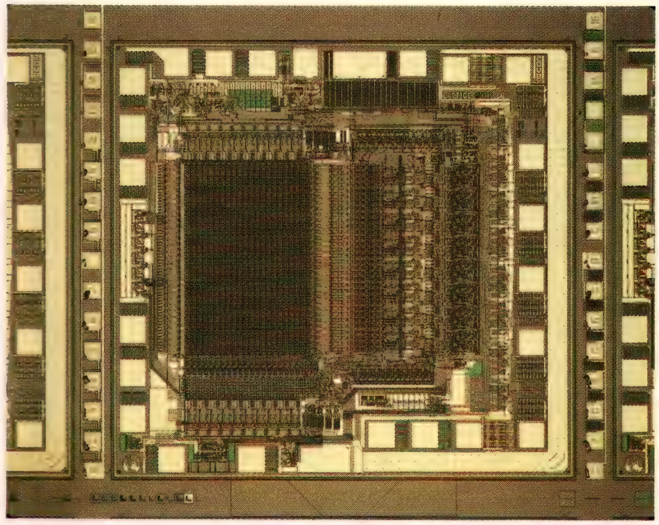
The 20-pin PALC18UQ8 *from AMD is a UV-erasable device whose programmable output macrocells are quite similar to the 22V10's.*



An electrically erasable version *of the classic 173 PLA is the Gould PEEL173.*

garden-variety PAL16L8, PAL16R8, PAL16R6, and PAL16R4, which sell for \$10.45 (100). Using the same bipolar process, AMD also manufactures two classes of 24-pin parts: the PAL20R8 family, which has a 10-nsec t_{PD} and a \$9.95 (100) price tag, and the PAL22V10-15, which has a 15-nsec t_{PD} and costs \$16.45 (100). The PAL20R8 family comprises the PAL20L8, PAL20R8, PAL20R6, and PAL20R4.

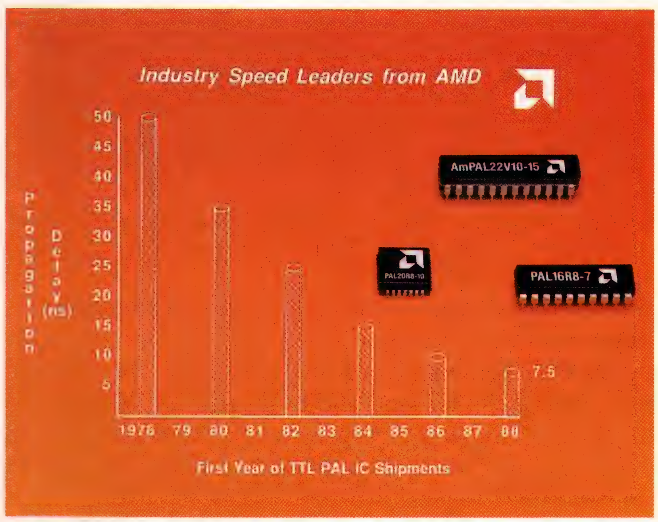
Signetics, too, has faster versions of established devices. First, the firm now has 12-nsec D versions of the 20-pin PLUS153 and 24-pin PLUS173 FPLAs. The parts sell for \$6.50 and \$10.50, respectively (in comparison, a new 15-nsec PLUS173B costs \$7.50). Thus, you can now use these more flexible PLAs in high-speed applications where previously only PAL-type devices could perform. Meanwhile, the firm's 20-pin 16XX and 24-pin 20XX PLDs, which cost \$5 and \$9.50, respectively, now come in 10-nsec t_{PD} versions.



***The GAL20V8A-12** from Lattice Semiconductor is an electrically erasable superset of common 20-pin PAL-type devices.*

CMOS chases bipolar

Lattice Semiconductor has also extended its 20-pin and 24-pin electrically erasable GAL (generic array logic) devices, which are supersets of common PALs, into the speed range of bipolar PLDs by lowering their t_{PD} to 12 nsec. Both the 20-pin GAL16V8A-12 and the 24-pin GAL20V8A-12 draw 115 mA. They sell for \$8.32 and \$9.51 (100), respectively. National Semiconductor acts as an alternate source for these parts.



***The PAL16R8-7 family** from AMD takes bipolar PALs into the speed range previously inhabited only by ECL devices.*

Architectural enhancements

Increases in speed are only part of the story of PLD improvements. In general, PLD makers have striven to make detail improvements to existing PLD architectures. Such improvements make the devices easier to apply, but don't change them so drastically that they require designers to master a completely new design discipline.

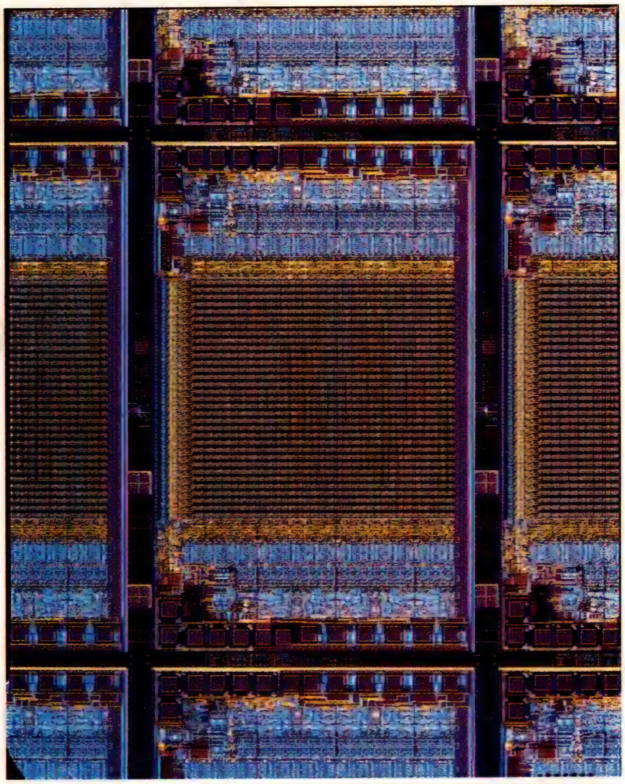
Exel's XL78C800 Erasic, for example, brings an exotic folded-NOR architecture to a 24-pin, electrically erasable device. With the company's software, however, you can compile logic specifications for conventional PLDs and exploit the device's unique properties.

The folded-NOR architecture allows you to program logic functions that can loop through the NOR array several times. Therefore, the device has a 2-part t_{PD} specification: a 10-nsec delay for getting signals on and off the chip plus a 15-nsec delay for each pass through its NOR array. The electrically erasable device can also emulate most common 24-pin PLDs. It draws 45 mA and comes in 45-, 35-, and now 25-nsec versions that cost \$9.25, \$12, and \$17 (100), respectively.

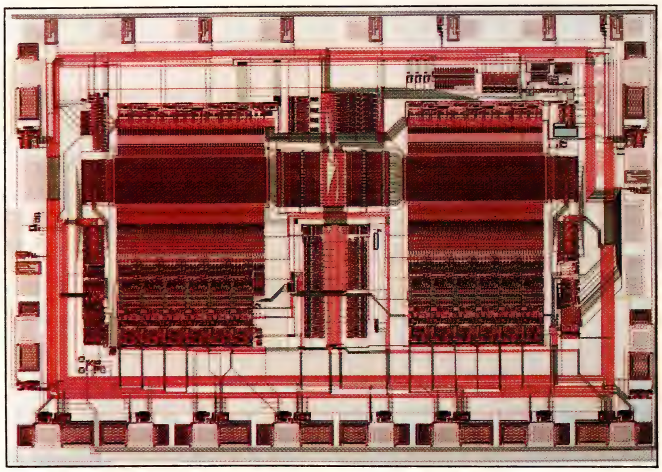
The folded-NOR architecture comprises a plane of uncommitted NOR gates whose outputs can feed the 10 output macrocells or feed back into the input array. Using the NOR plane, you can cascade as many as 42 levels of internal logic without going off chip. This cascading means that you can build up complex logic structures without using up I/O pins and incurring the delays that going off chip for logic feedback would cause.

Altera's EPM5032 takes a different route to architectural enhancement by combining the concept of uncom-

New PLDs are dramatically faster than the PLDs available just a year ago.



***A folded-NOR architecture** lets the XL78C800 Erasic from Exel emulate most common 24-pin PLDs.*



***A number of enhancements** to the conventional PAL-type architecture make the 5AC312 from Intel suitable for multiplexed systems.*

mitted gates—in this case, AND gates—with some elements of conventional PLDs. The device, the first member of a planned family of Max devices, is available in a 20-nsec t_{PD} version and a 30-nsec t_{PD} version for \$31.20 and \$26 (100), respectively. The device has 32 logic macrocells, eight dedicated input pins, and 16 bidirectional I/O pins.

The company claims that the device's more flexible architecture achieves six times the logic-function density of conventional PLDs. Further, it claims that the EPM5032 can directly implement the functions of most 7400 TTL devices and that it doesn't require the design changes that conventional PLDs do when emulating 7400 logic.

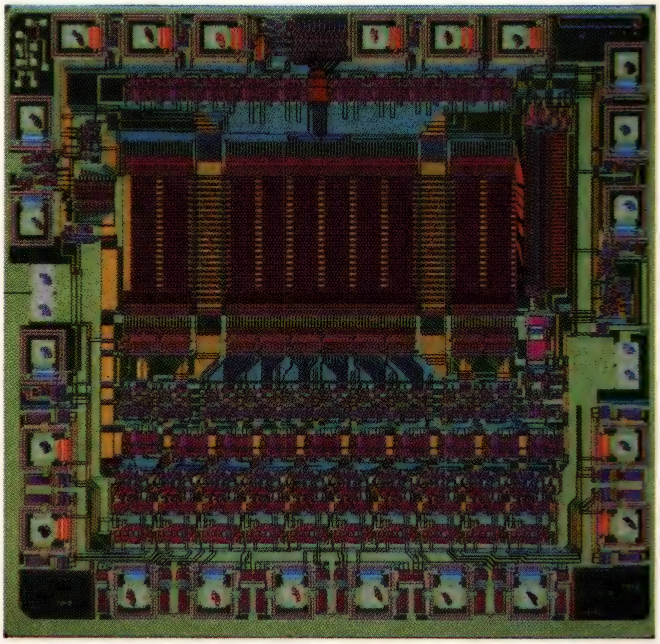
The basic idea underlying the Max architecture derives from the observation that 70% of all logic specifications require three or fewer product terms per output. Most PLDs provide fixed blocks of eight product terms per output; the Max architecture commits only three. To accommodate those designs requiring more than three product terms, the Max devices have an array of uncommitted gates that you can dedicate to any output.

The EPM5032, for example, has 64 expansion gates. If you don't need all the expansion gates for product terms, you can use a pair of cross-coupled expansion gates as a buried register. Further, you can connect the output of any logic element on the chip to the input of any logic element via a crosspoint-like interconnection array. Altera offers the Max devices' uncommitted gates and interconnection array as a solution to the problem of underutilization of PLDs' internal circuit elements.

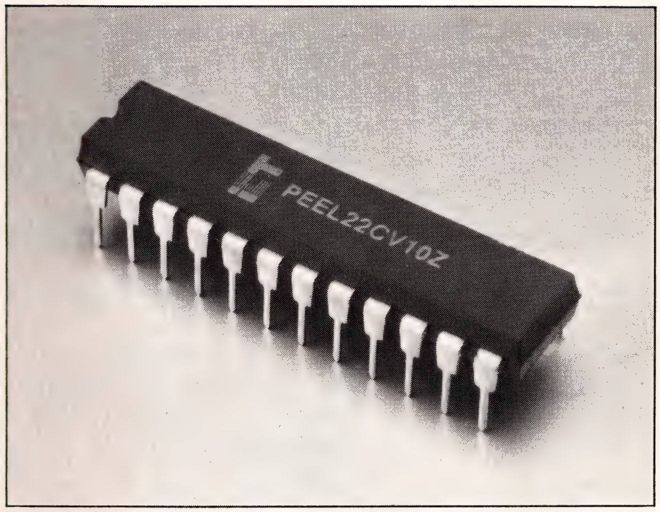
Peculiar numbering scheme misleads

Because of the peculiar part number of the Intel 5AC312, you might expect that this PLD has a very exotic, unusual architecture. In fact, the device is a conventional PAL-type device having a number of subtle, but very useful, enhancements that especially suit computer systems with multiplexed buses. The windowed version of the part costs \$19.50; the one-time-programmable (OTP) version is \$14.30 (100). The peculiar part number arises from a high-level decision at Intel to follow an internal numbering scheme rather than hewing to industry-standard nomenclature.

The 24-pin, 25-nsec t_{PD} device has both input and output macrocells that you can set up as registers, latches, or combinatorial circuits. It has eight dedicated inputs and 12 I/O macrocells. The I/O macrocells can function simultaneously as buried registers and as inputs. The asynchronous-clock, preset, and clear inputs to the I/O macrocells have two product terms each, unlike most PLDs, which have a single product term for these functions. You can reallocate some product



The firm's first entry in the PLD field, *the Seeq PALC20RA10Z, is a zero-power, electrically erasable version of the 20RA10.*



Featuring a user-programmable, automatic zero-power shutdown mode, *the PEEL22CV10Z from International CMOS Technology also offers I/O macrocells that have 12 programmable configurations.*

terms from one output to another.

The eight product terms associated with each I/O macrocell are divided into two groups of four. You can redirect the outputs of one or both of these groups of four from their I/O macrocell to an adjacent macrocell. Thus, a given I/O macrocell can have four, eight, 12, or 16 product terms feeding it (at the expense or profit of its neighbors).

Breaking all the rules

The PAL22IP6, a $13.95 (100) part that AMD dubs IPAC (interface protocol ansynchronous cell), is a unique PLA designed for coordinating communication between two unsynchronized systems. Instead of communicating in lock step with a common clock, two asynchronous processes can use the PAL22IP6 to perform handshakes. Seeq is an alternate source for this part.

The 24-pin PAL violates the secret protocol laid down for PALs by their first designers because it has edge-triggered flip-flops. Early PAL designers were against asynchronous design as a matter of principle. Metastability can always rear its ugly head when you use asynchronous-design techniques. AMD claims, however, that because it characterized the PAL22IP6's flip-flops for metastability, the flip-flops experience 75% less metastability than other flip-flops (a claim from which you can take as much comfort as you wish). The device has 16 inputs, and its six programmable outputs emit a healthy 48 mA for driving buses and backplanes.

Cypress Semiconductor's CY7C330 family, too, has an asynchronous member—the CY7331. The 28-pin, UV-erasable device implements state machines that clock at 50 MHz and costs $16.45 (100) for the 35-nsec version and $21.40 (100) for the 25-nsec version. It has 13 dedicated input pins that feed a conventional, programmable AND-OR array comprising 192 terms. The AND-OR array feeds 12 programmable I/O macrocells. The macrocells have both an input and an output flip-flop. You can program the macrocell's output flip-flops to be edge-triggered devices. Additionally, by virtue of an XOR gate at their inputs, you can program the output flip-flops as either D or T types.

The synchronous member of the family, the CY7330, has the same basic structure as the CY7331 except that its output flip-flops are synchronous and its input flip-flops are edge triggered. The part costs $23.55 (100) for the 33-MHz version and $30.60 (100) for the 50-MHz version.

Ranking second only to implementing state machines, address decoding comprises 20% of all PLD applications. Texas Instruments calls its TIBPAD16N8-7C a "PAD" for "programmable address decoder." Despite its familiar-looking part number, the device is not a conventional 16XX part. It has only one product term per output. Thus, it suits only high-speed address-decoding applications, and not general-

The amazing speed increases in bipolar PLDs amount to a virtual doubling in speed in just the past year.

purpose logic applications. But, because it has fewer logic elements than do conventional PLDs, it sports a 7-nsec t_{PD}. It costs $9.93 (1000).

The most popular architectural enhancement for PLDs has proven to be programmable output macrocells for CMOS PLDs. By virtue of the macrocells, one such CMOS device can replace a host of less-flexible bipolar devices.

AMD has joined the ranks of manufacturers that offer a nearly universal CMOS replacement for a gaggle of bipolar devices. The 20-pin PALC18UQ8 is a UV-erasable device having programmable output macro-

PLD testing: The issue that won't go away

If you use PLDs instead of fixed-function devices, you may have to assume some of the device-testing responsibilities that once were borne entirely by device manufacturers. PLD-testing strategies vary widely in their complexity, cost, and effect on device yields and field failures.

Logically, PLD-testing strategies should vary only to accommodate different device types and to achieve an appropriate AQL (acceptable quality level). Sadly, PLD-testing strategies also vary from company to company because of lack of understanding of PLD-testing issues or simply lack of care.

Rigorous testing

For example, although some PLD users follow the programming of their bipolar PLDs with a rigorous 3-day burn-in and full ac and dc parametric testing, others do no more than verify the PLD's fuse map after programming. These latter PLD users do not even bother to append a set of design-verification vectors to their JEDEC file to exercise the PLD with their PLD programmer's low-speed functional-test capability. (Some programmers apply test vectors to devices only one pin at a time. Such programmers may not be able to do proper testing of PLDs that have multiple qualifiers.)

Such slapdash methods will no longer suffice, however, because PLDs are becoming more complex and because the number of PLDs used in a given design is increasing. The likelihood of device failures is also increasing, therefore, and so is the probability of nonfunctional pc boards. Design engineers must realize that no matter which PLD they specify, the part brings certain testing costs with it into the factory.

An effective PLD-test strategy devolves from several factors:

- Device process technology,
- PLD architecture,
- On-chip test circuitry,
- Each particular PLD's program,
- Desired quality level.

These factors influence just how much testing you'll perform on a PLD (or whether you'll test it at all) at each manufacturing stage as it passes through your factory. The various tests include incoming inspection, device testing, and accelerated-life testing. Accelerated-life testing can have two goals—to reveal infant mortality and to predict field failures.

Duplicate production-line testing

The most rigorous in-house testing strategy for bipolar parts is simply to duplicate the final-test methods that any device manufacturer would employ for fixed-function parts. First, you must ensure that you have a testable design. Before releasing your PLD design for production, you should evaluate it for fault coverage and develop a comprehensive set of test vectors to supplement your design-verification vectors.

Secret test modes

In general, bipolar parts can't be tested before you program them. In some cases, however (especially if you're a big enough customer), the PLD manufacturer will release secret device-testing details that could allow you to perform some tests at incoming inspection. Bipolar-PLD makers use various fuse technologies; you should look for extended burn-in test results from each manufacturer to see if its fuse technology affects the programming yield.

After you program the device, you can check its fuse map and perform a simple, low-speed functional test on the device programmer. After programming and verification, you burn the device in for 72 hours and then retest it on high-speed (and high-cost) automatic test equipment (ATE) by using a complete suite of design-verification and fault-isola-

cells that are quite similar to the 22V10's. You can program the device's outputs in eight different registered or combinatorial, active-high or active-low, and locally or globally enabled combinations.

The devices exhibit t_{PD}s comparable to those of other low-power (55-mA) CMOS devices: 25 and 35 nsec. One-time-programmable versions of the devices cost $4 and $2.75 for the 25- and 35-nsec versions, respectively.

International CMOS Technology's PEEL18CV8 is a superset of both conventional 20-pin PAL-type PLDs and some architecturally enhanced devices, such as the

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tion test vectors. Such a test procedure will yield AQLs in the same range as those of TTL parts: failures of 100 to 200 ppm.

Such testing is expensive. Today's bipolar PLDs are approaching ECL speeds, and testing such fast parts requires high-speed, expensive ATE. Expensive test-vector-generating programs can lessen the number of man hours required to develop test vectors.

If you can't afford this expensive procedure, you can take advantage of services such as Texas Instruments' Impact program. TI has placed its Impact PLD testers with various distributors around the US. These distributors can program and test PLDs for you and can deliver PLDs whose AQLs are the same as those of TTL parts.

The PLD-testing picture changes dramatically when you use erasable PLDs. Manufacturers of either electrically erasable or UV-erasable PLDs can program several patterns into their devices for test purposes during manufacturing, and then erase them before shipping. They claim, therefore, that because they ship devices that are 100% tested, you don't need to do any testing beyond simple fuse-map verification to achieve a 100-to 200-ppm AQL.

Indeed, Intel suspects that further testing on your part may only decrease yields and damage devices without increasing device reliability. The only field failures Intel has seen to date in its UV-erasable devices were caused by improperly calibrated device programmers. Typically, an out-of-spec programmer blows the device's V_{PP} line open.

Altruism versus experience

Be aware that the reason that erasable-PLD makers are doing extensive tests on their devices is not simply because the devices' process technology permits them to do so. Erasable-device makers generally do a high-temperature burn-in on each device to check for program-data retention. Elevated temperature puts the greatest stress on the insulation layer that protects the erasable devices' floating gates. The manufacturers must do this burn-in to achieve an acceptable quality level.

You can take advantage of their test procedures, therefore. However, before you do, you should examine their test procedures thoroughly. The thoroughness of a given manufacturer's test may reflect the company's devotion to quality or may reflect a less-than-mature manufacturing process. Typically, IC makers do less and less testing as they gain more experience with a given process.

Erasable-device manufacturers can often supply extended-burn-in test results, which link the burn-in data to expected field failures. You should pay particular attention to 1000-hour burn-ins at elevated temperature *and* elevated humidity for plastic-packaged devices. Today's smaller IC packages have less plastic between the outside world and the chip, so they can be more susceptible to environmental contamination.

The devices' process technology can determine the number of tests a manufacturer performs. Electrically erasable devices have a shorter program-erase cycle than do UV-erasable devices. Therefore, manufacturers of electrically erasable devices can program and test 20 to 30 patterns for each device. To make up for their devices' slower program-erase cycle, UV-erasable-device manufacturers typically include more onboard test circuitry than do makers of electrically erasable devices.

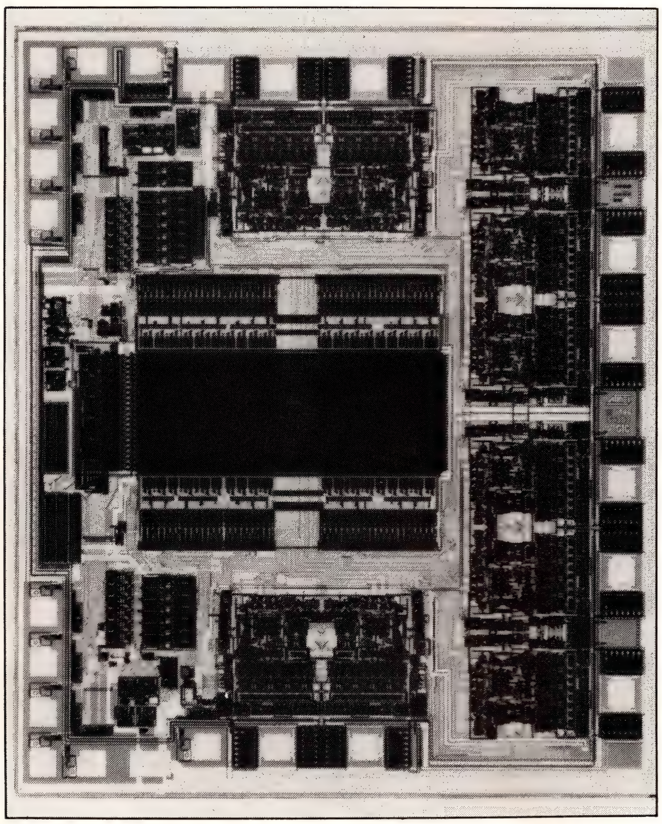
Finally, in many cases, you won't be able to duplicate the manufacturers' test patterns, because erasable-device makers won't release their internal test procedures for fear of giving away design secrets.

PLD makers' improvements to existing PLD architectures make the devices easier to apply without requiring designers to master a new design discipline.

COMPARISON OF VARIOUS DEVICE TECHNOLOGIES

	PARAMETER	FAST	AS	16R8-7	GA22V10-7
COUNTERS 74161 4-BIT COUNTER	t_S	5.5	8.0	7.0	3.0
	t_{CO}	11.0	13.5	6.5	6.0
	f_{MAX}	60.0	46.5	74.0	110.0
74269/869 8-BIT COUNTER	t_S	2.5	5.0	7.0	3.0
	t_{CO}	10.0	11.0	6.5	6.0
	f_{MAX}	80.0	62.5	74.0	110.0
COMBINATORIAL FUNCTIONS 74138 DECODER	t_{PD}	8.0	10.0	7.5	7.5
74151 MULTIPLEXER	t_{PD}	11.0	15.0	7.5	7.5
REGISTER, LATCH 74374 OCTAL REGISTER	t_{CO}	10.0	9.0	6.5	6.0
74373 OCTAL LATCH	t_{PD}	8.0	6.0	7.5	7.5
	t_{LEO}	13.0	11.5	7.5	7.5

NOTE:
ALL TIMES ARE IN NANOSECONDS, EXCEPT FOR f_{MAX}, WHICH IS IN MHz



***The equivalent of two 22V10s** reside on the 1-chip Atmel V750.*

Lattice GAL16V8 and the Altera EP320—which are themselves supersets of conventional PAL-type devices. The electrically erasable PEEL18CV8 achieves this flexibility by virtue of its output macrocell. Other 20-pin PLDs' macrocells allow only four or eight configurations; the PEEL18CV8 permits 12.

The 18CV8 has an architectural enhancement that typifies the detail improvements PLD designers have been incorporating in newer devices. The device has a ninth product term for each output macrocell for the output-enable function; older devices have only eight product terms per macrocell. In μP systems, you often need all eight product terms for the logic function, which would leave you one product term short for the output-enable function if you used older devices. The 18CV8 comes in 35- and 25-nsec t_{PD} versions; they sell for $2.10 and $3 (1000), respectively. The 18CV8's power consumption—the lowest among 25-nsec devices—specs 20 mA plus 0.7 mA/MHz max.

Atmel's V750, which costs $14.63 (100), is a more flexible superset of the industry-standard 22V10. The V750 is virtually a Siamese-twin pair of 22V10s shoehorned into the same package that the company uses for a single 22V10. Each of the V750's output macrocells has a pair of flip-flops; a 22V10's macrocells have a single flip-flop each. Each of the V750's flip-flops, in turn, has a full complement of conventional AND/OR

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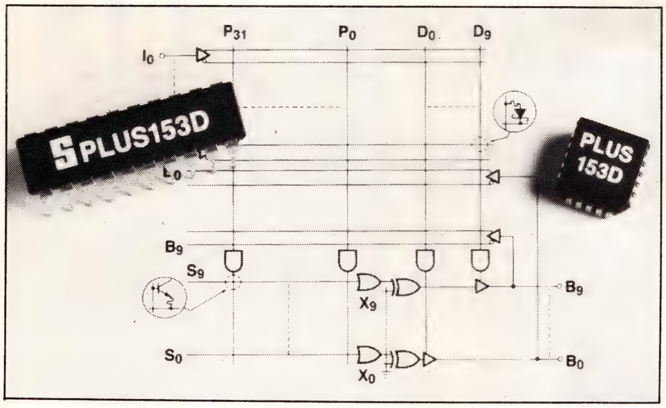
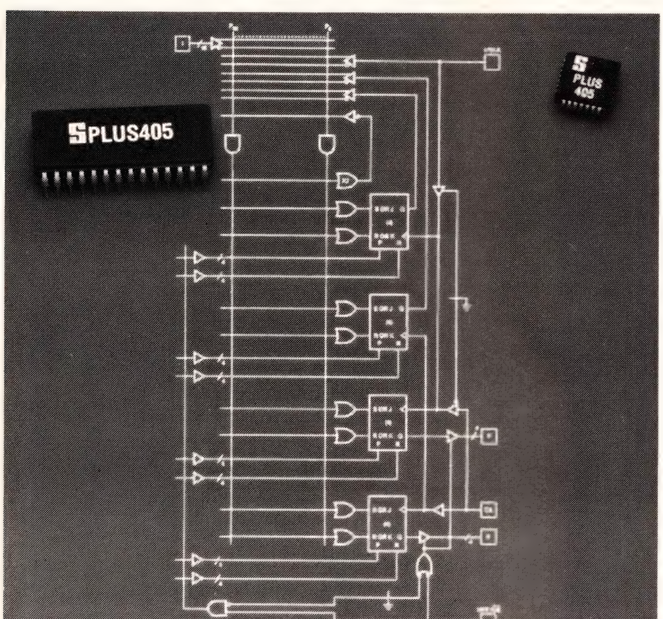
Ranking second only to implementing state machines, address decoding comprises 20% of all PLD applications.

terms driving it. One of the two flip-flops feeds the output, and the other is a feedback term to the chip's AND/OR array. You can optionally route the feedback flip-flop's product terms into the output flip-flop's OR gate.

These architectural enhancements yield a device that's much more flexible than a 22V10. For example, you can have both a buried register and an output register for each output. Or you can program each output macrocell as an input while still retaining the buried register. Or you can double the number of product terms fed to the output register by routing the feedback register's product terms to it.



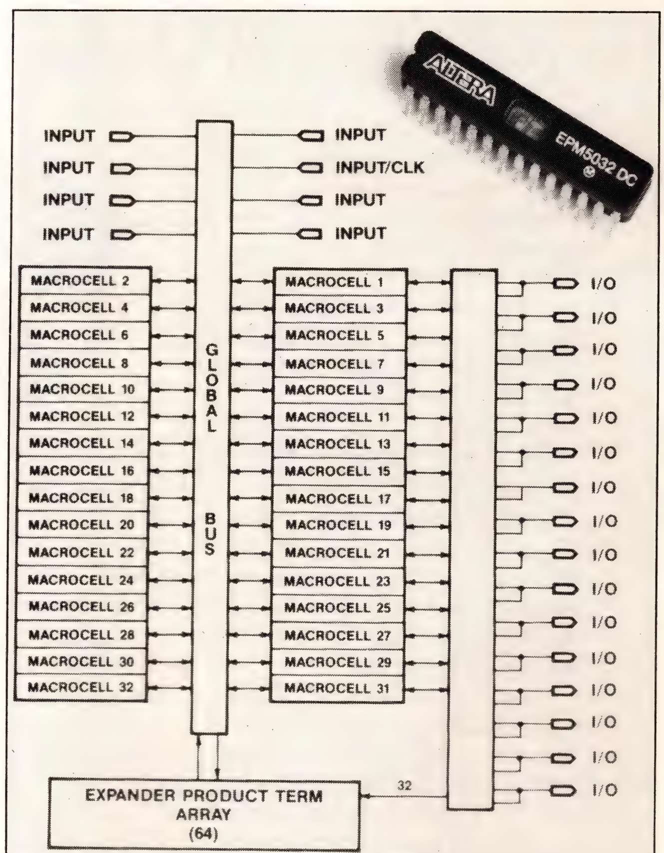
With a t_{PD} of only 12 nsec, *the PLUS153D PLA from Signetics now allows you to use the more-flexible PLA in applications for which formerly only PAL-type devices were fast enough.*



The PLUS405 is a field-programmable logic sequencer *from Signetics that clocks at 33 MHz.*

Lattice Semiconductor has brought its GAL concept to the FPLA. The firm's GAL6001 is a superset of existing 24-pin PAL and IFL PLDs. It is an electrically erasable device that has 10 programmable output macrocells, eight buried registers, and 10 input macrocells. It also features a 30-nsec t_{PD}. Its AND array has 78 inputs × 75 outputs; its OR array has 64 inputs × 36 outputs.

As engineers pack ever-increasing numbers of PLDs onto their pc boards, power consumption is becoming a critical issue. Half- and quarter-power versions of conventional bipolar PAL-type devices have been available for some time. The tradeoff associated with these devices is that lower speed accompanies lower power consumption. Now, however, the speed of low-power bipolar devices is improving. For example, the Signetics PLHS16L8B ($3.75) and PLHS18P8B ($4.33)



The first UV-erasable device *to use the Max architecture is Altera's EPM5032. The Max architecture features 64 uncommitted product terms that you can allocate to any macrocell, and it has a crosspoint array for interconnecting logic elements.*

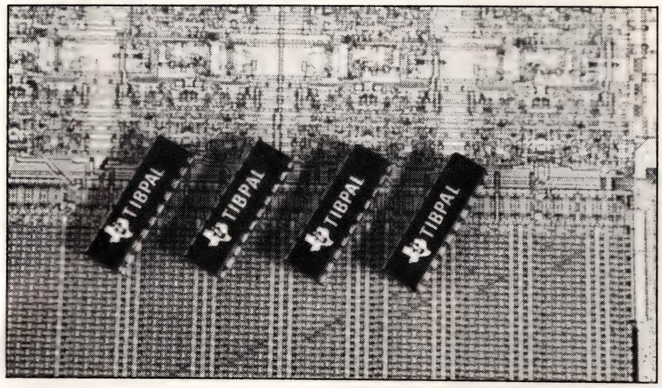
The most popular architectural enhancement for PLDs has proven to be programmable output macrocells for CMOS PLDs.

have 15-nsec t_{PD}s but draw only 155 mA; similar PLDs draw 180 mA. The PLHS16L8B costs \$3.75; the PLHS18P8B is \$4.33.

A series of four 24-pin, half-power PALs from Texas Instruments—the TIBPAL20L8, R4, R6, and R8-25—have the 25-nsec t_{PD} of second-generation devices but draw only 90 mA versus 180 mA for the earlier parts. Note that first-generation, 24-pin PALs had 35-nsec t_{PD}s and drew 180 mA. The parts in the series each sell for \$3.61 (1000).

Even among different vendors' versions of the venerable 22V10, you can find a low-power variant. Atmel's 22V10L draws 12 mA on standby plus an additional 15 mA when clocked at 1 MHz. In contrast, the company's standard 22V10 specs 100 mA standby and 100 mA when clocked at 1 MHz. It costs \$14 (100).

In addition to the larger 22V10, low-power CMOS versions of the original PLD, FPLAs, are available from International CMOS Technology; an alternate source is Gould Semiconductor. They consume about one-fifth the power of their bipolar cousins despite their shorter (35-nsec) t_{PD}s. International CMOS Technology makes two flavors of electrically erasable



***The TIBPALs** from Texas Instruments feature a 10-nsec t_{PD}.*

FPLA: the PEEL153P and the PEEL173P, which are comparable to the Signetics PLS153 and PLS173 respectively; they sell for \$4.57 and \$5.15 (100). The company also makes the PEEL253P and the PEEL273P. These last two devices are supersets of the PLS153 and PLS173 and cost \$5.81 and \$6.64 (100). Their enhancements include 10 additional product terms, independent output enables for the OR arrays, and a device-signature word. Gould is an alternate

Manufacturers of PLDs

For more information on PLDs such as those discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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Exel Microelectronics Inc
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Gazelle Microcircuits Inc
2300 Owen St
Santa Clara, CA 95054
(408) 982-0900
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Gould Semiconductor
2300 Buckskin Rd
Pocatello, ID 83201
(208) 234-6668
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International CMOS Technology Inc
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FAX (408) 434-0688
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Intel Corp
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Seeq Technology Inc
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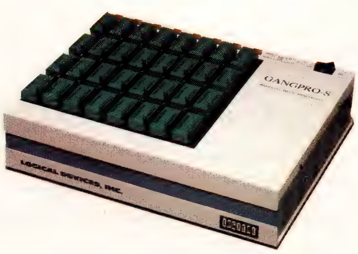

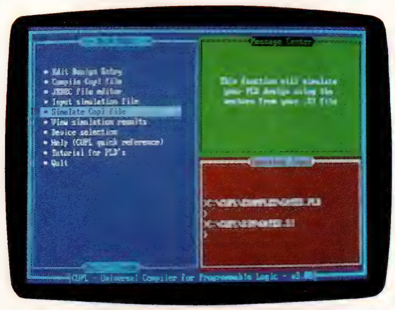

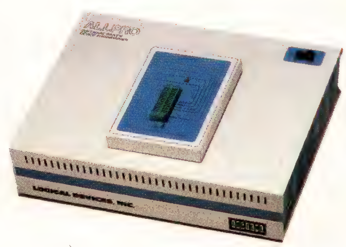

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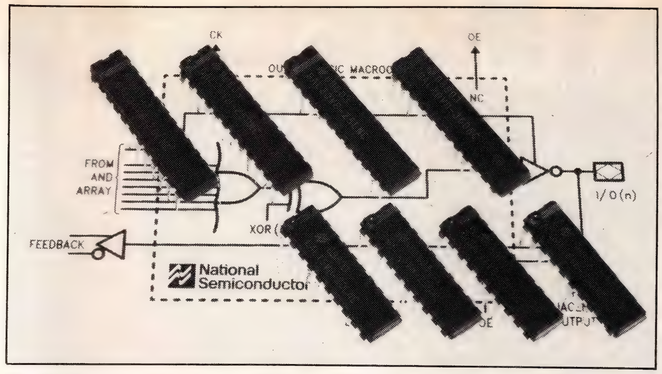

Two electrically erasable devices, *National Semiconductor's GAL16V8 and GAL20V8, permit complete ac, dc, cell, and functional testing.*

source for these devices.

Making their debut in the medium-power, medium-speed range are 16XX and 20XX UV-erasable PLDs from Samsung. The 16XX parts range in price from \$2.60 to \$4.50, and the 20XX devices range from \$3.50 to \$7. The devices feature t_{PD}s of 25 and 35 nsec, and they draw 45 and 75 mA, respectively.

For the most power-critical applications, a narrow selection of so-called zero-power devices is available. The devices, like all electronic parts, actually consume zero power only when they are off and unpowered; in their standby state, however, they draw only microamps and hence almost justify their name.

Almost no power at all

The low-power version of International CMOS Technology's UV-erasable 22CV10, for example, is the 22CV10Z, which draws 45 mA plus 0.5 mA/MHz when operating. However, if you've selected the low-power mode when programming the device, the device will power itself down when it detects no input activity. It will stay powered down until input activity resumes. In the power-down state, the device draws only 100 μA. The 22CV10 costs \$10.45 (1000); the low-power 22CV10Z costs \$14.14 (1000).

Seeq's first entry in the PLD field, the PALC20RA10Z, is a zero-power, electrically erasable version of the 20RA10. The PALC20RA10Z draws only 150 μA on standby and 5 mA/MHz when operating. AMD is an alternate source for the device, which comes in 40- and 45-nsec t_{PD} versions.

Finally, Texas Instruments has extended zero-power characteristics to 20-pin devices with a series of four UV-erasable PALs: the TICPAL16R4, R6, R8, and L8-55, all of which are priced at \$5 (1000). The devices draw 100 μA in standby mode and 2 mA/MHz when operating. Like other very-low-power devices, they are not as fast as higher-power devices; their t_{PD} is 55 nsec. EDN

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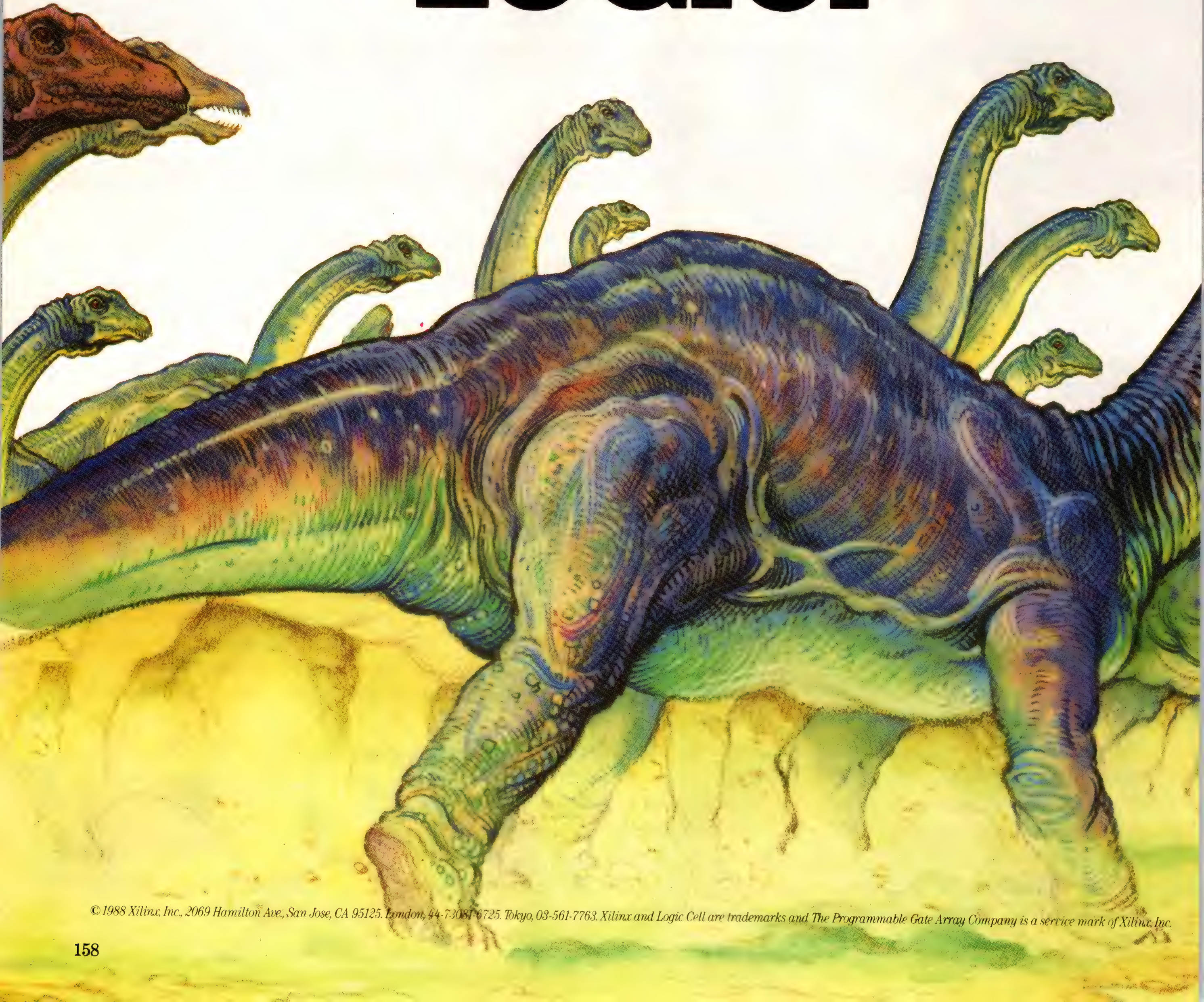

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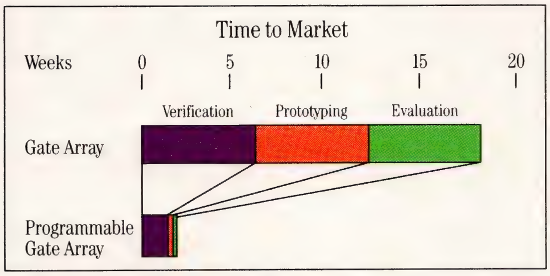

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Wescon/88

Tom Ormond, *Senior Editor*

When the 1988 edition of Wescon opens for a 3-day run at the Anaheim, CA, Convention Center on November 15 through 17, it will spotlight the latest in electronics technology. The 36-session professional program will address such topics as advanced logic, gallium arsenide (GaAs) technology, application-specific integrated circuits (ASICs), programmable logic devices, and testability considerations. The program will also touch on neural networks.

This year, the Wescon program is organized into tracks—topically related sessions—so that attendees can devote a specific block of time to subjects that particularly interest them. Heading the list of tracks is a group of sessions on designing with today's high-performance devices.

A logical place to start

ECL has long been the primary driving force in high-speed, high-performance systems, and device manufacturers have had to make significant improvements in packaging and process technology to keep pace with the demands for higher system throughput. The four papers in **Session 11** will highlight some of the new ECL product introductions and illustrate how these products address today's system needs. The presentations will discuss the crossing of the TTL-ECL boundary, how BiCMOS fits into an ECL design, and how to apply ECL in automatic test equipment systems. Papers will illustrate how designers can couple the new technologies with innovative circuitry to build economical systems with highly improved performance levels.

ECL is no longer the only technology to consider when it comes to high speed. Advanced CMOS logic (ACL) also offers high speed performance and provides one additional and very significant benefit—low power consumption. For designers striving to learn how to fully realize the benefits of ACL, **Session 2** will prove most helpful. Papers in this session will address topics such as compatibility and system-level, analog, and thermal considerations.

For years, GaAs IC manufacturers have trumpeted the advantages of using their technology. Today, designers are finally thinking about GaAs as a viable way to solve the needs of high-performance systems. The papers in **Session 28** will go over the problems designers have experienced in trying to use off-the-shelf GaAs devices in their system designs.

The papers in **Session 32** will look at the GaAs ASIC situation. Discussions will cover a communication-system crosspoint switch design, the application of GaAs logic in frequency-measurement applications, and the use of ASIC design techniques to verify a multiplexer/demultiplexer system.

But wait—there's more on ASICs

ASICs will garner center-stage attention in two other sessions. **Session 4,** for example, will highlight techniques for successful system design using the devices. The papers will present some specific design methodologies that reduce the risk of using ASICs to implement systems. Presentations will stress the point

WESCON/88 TECHNICAL-SESSION PROGRAM AT THE ANAHEIM HILTON HOTEL

Day	Time	California Ballroom A	California Ballroom B	Pacific Ballroom A	Pacific Ballroom B	Pacific Ballroom C
TUESDAY, NOVEMBER 15	9:00 AM TO 11:00 AM	(1) ADVANCED FLOATING POINT SOLUTIONS FOR 32-BIT MICROPROCESSORS	(2) SYSTEM LEVEL DESIGN SUCCESS WITH ADVANCED CMOS LOGIC	(3) VLSI SOLUTIONS FOR MICROCHANNEL INTERFACING	(4) SUCCESSFUL SYSTEM DESIGN TECHNIQUES USING ASICs	
TUESDAY, NOVEMBER 15	12:00 PM TO 2:00 PM	(5) MEMORY MANAGEMENT SCHEMES FOR TODAY'S COMPLEX COMPUTER ARCHITECTURES	(6) ADVANCED ECL—GENESIS OF A NEW ERA IN PERFORMANCE	(7) HIGH PERFORMANCE SCSI INTERFACE CHIPS	(8) ASIC MODULE COMPILATION/ CUSTOMER SPECIFIC CELLS	(9)* UPDATE ON THE SPACE STATION
TUESDAY, NOVEMBER 15	3:00 PM TO 5:00 PM	(10) SYSTEM DESIGN FLEXIBILITY OFFERED BY FLASH EPROM/EEPROM	(11) EMITTER COUPLED LOGIC (ECL)—SYSTEM SOLUTIONS FOR HIGH PERFORMANCE SYSTEMS	(12) MODEMS IN THE 1990's	(13) DESIGN FOR TESTABILITY; SYSTEM TESTABILITY IN LIGHT OF EMERGING TEST BUS STANDARDS	
WEDNESDAY, NOVEMBER 16	9:00 AM TO 11:00 AM	(14) DESIGN TECHNIQUES FOR INNOVATIVE PLD ARCHITECTURES	(15) MODERN PROGRAMMABLE STATE MACHINES	(16) INTEGRATED CIRCUITS' ELECTROMAGNETIC COMPATIBILITY		
WEDNESDAY, NOVEMBER 16	12:00 PM TO 2:00 PM	(17) PROGRAMMABLE LOGIC TESTABILITY—THE DESIGN IS DONE...NOW WILL IT WORK IN PRODUCTION?	(18) HIGH SPEED/HIGHLY INTEGRATED MICROCONTROLLERS AND THEIR APPLICATIONS	(19) SILICON CIRCUITS OFFER CIRCUIT DENSITY IMPROVEMENT	(20) THE USE OF PERSONAL COMPUTERS IN TEST AND MEASUREMENT APPLICATIONS	(21) NEURAL APPLICATIONS
WEDNESDAY, NOVEMBER 16	3:00 PM TO 5:00 PM	(22) SPECIAL-PURPOSE PROGRAMMABLE LOGIC DEVICES AND THEIR APPLICATIONS	(23) RISC SYSTEMS ENTER THE MAINSTREAM	(24) NEW TECHNOLOGY; PROTECTING IT AND PROTECTING YOURSELF	(25) SIGNIFICANT ADVANCES IN DATALOGGING	
THURSDAY, NOVEMBER 17	9:00 AM TO 11:00 AM	(26) MEETING THE NEEDS OF THE EE PROFESSION	(27) AUTOMATION OF SURFACE MOUNT MANUFACTURING	(28) GALLIUM ARSENIDE ICs FROM A USER'S PERSPECTIVE: PART I—STANDARD PRODUCTS	(29) PARALLEL COMPUTING AND MULTIPROCESSORS	
THURSDAY, NOVEMBER 17	12:00 PM TO 2:00 PM	(30) BUSINESS ISSUES FOR THE YOUNG HIGH-TECHNOLOGY COMPANY	(31) SOLVING THE INDUSTRIAL COMMUNICATION PROBLEMS BY IMPLEMENTING MANUFACTURING AUTOMATION PROTOCOL (MAP)	(32) GALLIUM ARSENIDE ICs FROM A USER'S PERSPECTIVE: PART II—ASICs	(33) C DEVELOPMENT ENVIRONMENT FOR SUPPORTING ELECTRONIC APPLICATIONS	
THURSDAY, NOVEMBER 17	3:00 PM TO 5:00 PM	(34) SYNERGISTIC MARKETING	(35) CAE/CAD: LINKING DESIGN TO SUPPORT MANUFACTURING		(36) DEVELOPMENT TOOLS FOR HIGH PERFORMANCE RISC MICROPROCESORS	

*SESSION 9 RUNS FROM 2:00 PM TO 5:00 PM, RATHER THAN 12:00 TO 2:00.

that first-pass ASIC success requires development tools that coordinate the ASIC-design and the system-design specifications.

The ASIC industry is moving to expand the capabilities available to customers. The commercialization of compilation techniques that enable customers to augment (directly or indirectly) ASIC libraries epitomizes this movement. More comprehensive customer/vendor interaction is the key ingredient.

Participants in the panel discussion of **Session** 8 will debate key issues associated with the value of module compilation for ASIC designers and whether module compilation's time has come. Panelists will also address the question of whether module compilation/customer specific cells are the responsibility of the vendor or the customer. Discussions will also center on the level of sophistication necessary to effectively use module compilation. The key here is responsibility—should cell development be in the hands of the customer, the vendor, or a combination of both?

A look at the PLD picture

Today's programmable logic device (PLD) architectures offer designers more flexibility and integration capability than ever before. To take advantage of these architectures, however, users must fully understand correct design techniques. The papers in **Session 14** will focus on such techniques by walking through the implementation of applications examples for several architecturally innovative PLDs.

As the technology matures, so too does the level of PLD specialization. Papers in **Session 22** will illustrate some of these specialized devices (for example, a programmable BUS interface) along with some target applications—a solution for asynchronous designs and a programmable PS/2 interface.

But will it work in production?

Any discussion of PLDs would be incomplete without considering the testing question. PLDs are finding their way into more design starts today. This popularity raises testability issues that were not even considered when PLDs were sparingly used as glue-logic chips. The papers in **Session 17** will illustrate that reliable PLD implementation is possible only if testability questions are addressed throughout the design and production cycles.

Design for testability (DFT) is quickly becoming a critical component in the product design cycle. The increase in test costs and the use of new packaging techniques have increased the importance of including self-testing capabilities in today's system designs. Designers can now use emerging test-bus standards to ensure interoperability at board or system levels.

Papers in **Session 13** will illustrate several approaches to DFT and discuss the new JTAG/IEE P1149.1 serial test bus. Coverage will include boundary scan technologies from the standards and user's point of view, along with the viability of merging BIST (built-in self test) and boundary scan at the IC level.

Closing with a final thought

On Wednesday afternoon, November 16, **Session 21** will describe potential applications of neural networks via five short talks and a panel discussion, where questions from attendees will be answered. After a short review of the neural network concept and the kinds of problems such networks are best equipped to solve, presentators will cover four application aspects—electronic neural networks, optical neural networks, neural networks in signal processing, and neural networks in defense programs. The neural field is progressing rapidly, and most of the presentations will highlight very recent advances. EDN

Transportation and show details

The Wescon/88 conference and exhibition will take place on Tuesday, November 15 through Thursday, November 17 at the Anaheim Convention Center in Anaheim, CA. General admission is $10 at the door; the fee covers exhibits, technical sessions, and admission to the film theater for the three days.

Registrants coming from the San Diego and Santa Barbara areas are encouraged to ride Amtrak to the show; free shuttle buses will transport train passengers to the Convention Center. Free shuttles will also run between the Anaheim Convention Center and many of the major local hotels. For more information, contact Electronic Convention Management, 8110 Airport Blvd, Los Angeles, CA 90045. Phone (213) 772-2965.

Article Interest Quotient (Circle One)
High 470 Medium 471 Low 472

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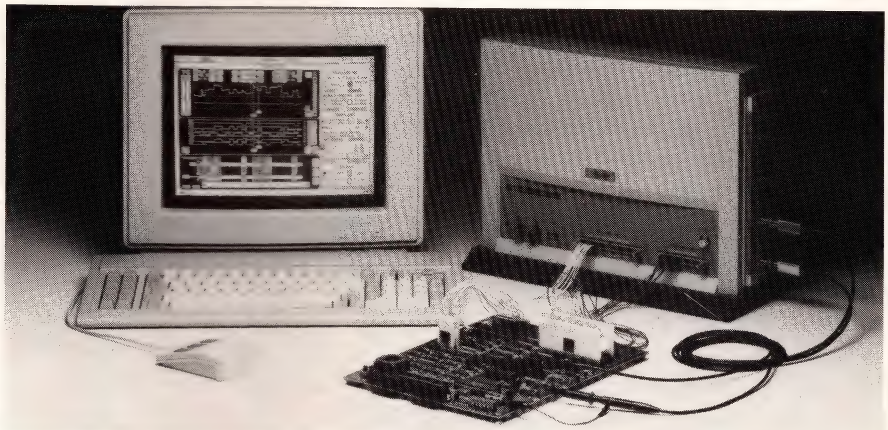
CIRCLE NO 193

Instrument combines 48-channel LA, 100-MHz DSO, and stimulus generator



The Omnilab 9240 is a combination digital-storage oscilloscope (DSO), logic analyzer (LA), and digital stimulus generator that comes in an attaché-case-sized enclosure. Unlike separate instruments, the DSO and LA are designed to work in tandem. An IBM PC, PC/XT, or compatible computer hosts the unit.

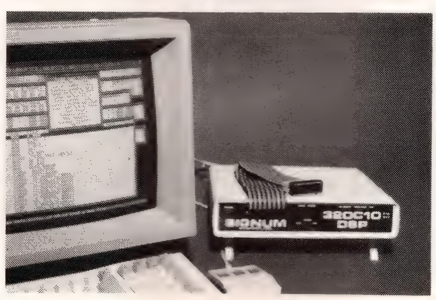
In combination with a feature named Multiview, the Select trigger system allows you to observe time-correlated analog and digital displays. Select combines the features of scope and logic-analyzer triggering. You can qualify the trigger conditions by using the truth tables stored in RAM or by programming minimum and maximum time delays. In addition to letting you see time-correlated displays, Multiview lets you watch digital data alone, analog data alone, or both analog and digital displays representing separate time intervals.

Continuous sampling in conjuntion with flexible triggering permits the unit to capture and display every occurrence of infrequent events, such as missing pulses, metastable states, noise glitches, and bus contentions. From $8900.

Orion Instruments, 702 Marshall St, Redwood City, CA 94063. Phone (415) 361-8883. TLX 530942. FAX 415-361-8970. Booth Nos 3372, 3374.

Circle No 635

DSP development tool is nonintrusive to target system



Designed specifically for digital signal processing (DSP) systems, the Model E-232-DSP-10 emulator is nonintrusive to the target system. It features an easy-to-use user interface and completely emulates the target system without missing anything.

Under interactive control, the E-232-DSP-10 emulates all functions of TI's TMS320C10 family of DSP microcontrollers without restrictions of any sort. It offers sophisticated event definitions, which can be used as breakpoints or trace controls. Three simultaneous sets of events are defined in terms of any or all of the following parmeters in any combination—addresses, data patterns, CPU operations, and external inputs. In addition, two 16-bit pass counters allow you to count and/or delay events. An 8-level hardware sequencer can sequentially trigger to, from, or between any breakpoint event sets or pass-counter values. Still other breakpoints can be triggered in the event of a trace-full condition, a watchdog timer out, or an illegal op code fetch.

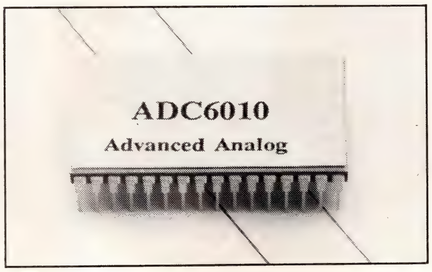
Other features include in-line symbolic assemblers and disassemblers, two banks of 4k overlay program memory for virtual memory operation, an 8-channel user-logic state analyzer, and performance-analysis hardware and software that allows the target-system designer to evaluate the target code's efficiency with both tabular and graphic displays. $5995.

Signum Systems Inc, 1820 14th St, Santa Monica, CA 90404. Phone (213) 450-6096. Booth No 3142.

Circle No 639

12-bit A/D converter features on-board sample/hold circuitry

The AD6010 12-bit successive-approximation A/D converter comes complete with internal sample/hold circuitry, a clock, and a reference. The conversion time is 4 μsec and can be short-cycled to 2.8 μsec. The converter features five user-selectable input ranges—0 to 5V, 0 to 10V, ±2.5V, ±5V, and ±10V.



Data is available in parallel or serial format complete with corresponding clock and status signals. The gain and offset can be externally trimmed to zero to provide a full-scale accuracy of ±0.012%±½ LSB. Digital input and output signals are DTL/TTL compatible. The power consumption is 1.2W typ.

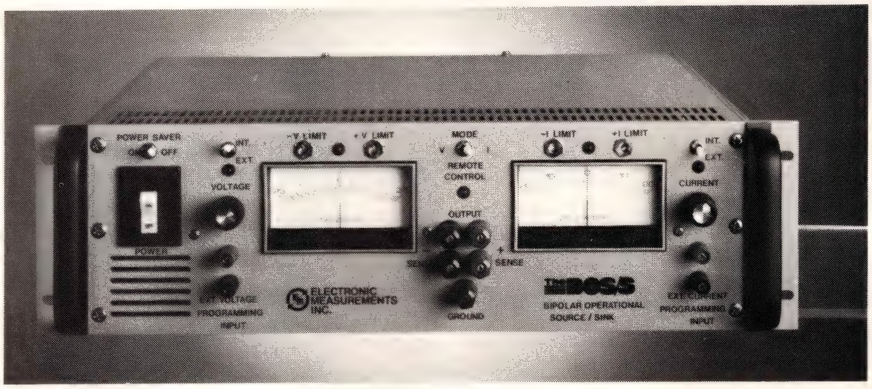
The 6010 is housed in a hermetically sealed 32-pin DIP and is available in three operating range grades: 0 to 70°C, −25 to +85°C, and −55 to +125°C. The 6010C, which is specified over the −55 to +125°C operating range, has a linearity drift spec of ±2 ppm/°C max. A military version is also available, which is fully screened and tested to MIL-STD-883 Rev C Level B requirements. $136 (100) for the −25 to +85°C version. Delivery, stock to nine weeks ARO.

Advanced Analog, 2270 Martin Ave, Santa Clara, CA 95050. Phone (408) 988-4930. TWX 910-338-2213. FAX 408-988-2702. Booth No 1708.

Circle No 637

Bipolar operational power supply provides over a dozen functions

The BOS/S can function as a dc power supply, an electronic load, a voltage source, a power pulse generator, a current source, a power function generator, a direct-coupled amplifier, a variable gain amplifier, a fast-slewing power supply, a dc amplifier, an ac power supply, a differential amplifier, and a signal-invertering amplifier. The current or voltage output is controlled via a front-panel mode switch.



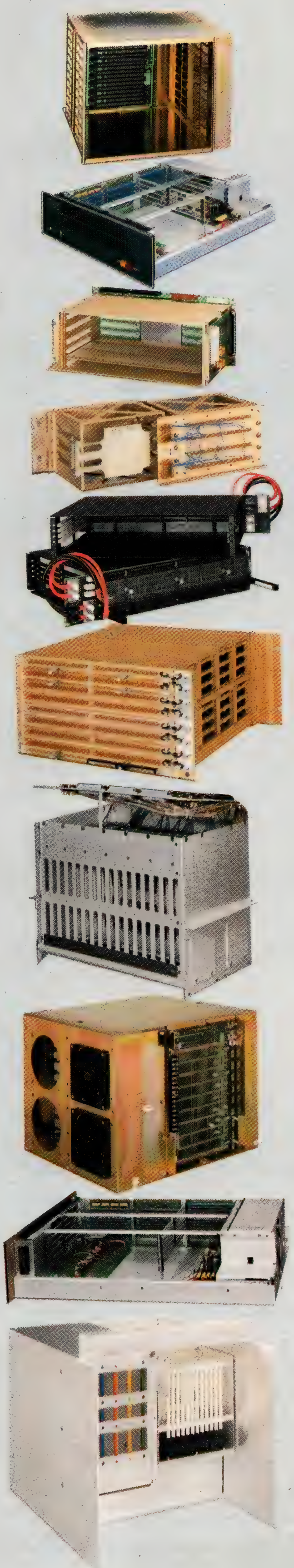
Control can be internal or external. A 10-turn potentiometer controls the output over the maximum −V to +V range. An external ±10V source provides identical external control. An optional digital control board allows you to program most of the unit's functions via the IEEE-488 bus or a parallel data-transfer bus.

The talk and listen functions have 12-bit resolution. The voltage and current regulation are 0.005%, and the TC is 0.01%/°C in the voltage mode and 0.03%/°C in the current mode. The rms ripple equals 3 mV in the voltage mode and 0.05% in the current mode. Voltage and current output changes over eight hours are 0.02 and 0.03%, respectively. Standard features include adjustable output limiting, indications of mode and remote operation, and analog or digital voltage and current meters. $1095 to $1995. Delivery, stock to eight weeks ARO.

Electronic Measurements Inc, 405 Essex Rd, Neptune, NJ 07753. Phone (201) 922-9300. Booth Nos 3369, 3371.

Circle No 636

Think SAE Stanford Applied Engineering



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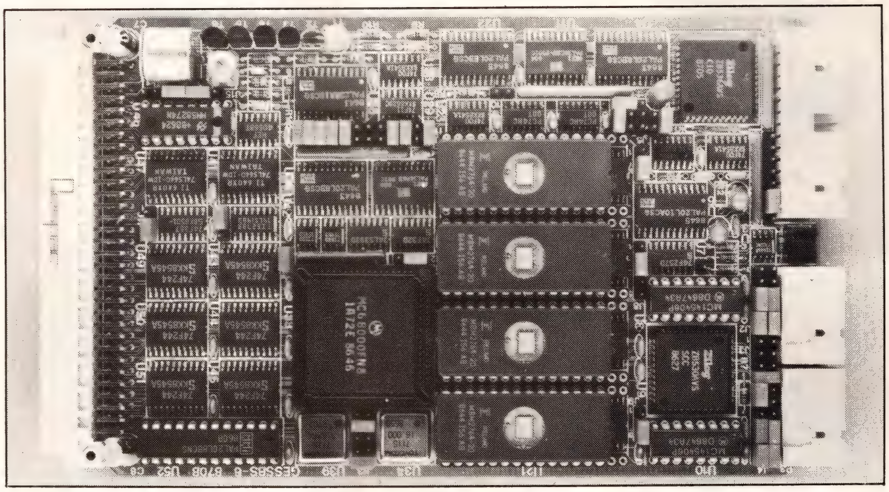
Wescon/88 Products

Single-board computer designed for G-64 bus applications



Designed to interface with the G-64 bus, the MPL-4079 single-board computer features an all-CMOS design built around the 68HC000 µP. The 4×6-in. Euroboard incorporates two serial ports, a 4-channel A/D converter, parallel I/O, a clock, EPROM, and battery-backed RAM.

The CPU and memory available on board are sufficient to handle most applications running under the OS-9 operating system. Drivers are available for all the peripherals, as are full facilities for symbolic debugging and program down-loading through the serial port. Users can also develop programs under the MTX multitasking kernel, and a debugger is available for programs written in Pascal.

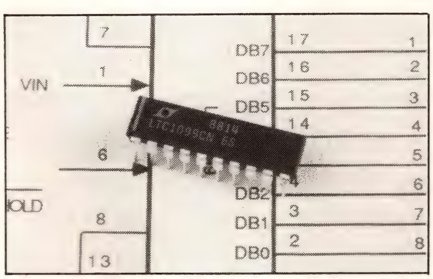
A 4-channel, 8-bit A/D converter with a 40-µsec conversion time allows the MPL-4079 to fully support industrial real-time applications. There are 20 parallel I/O lines available for logic level inputs and two RS-232C serial ports for communications. The baud rates are programmable.

The MPL-4079 is also equipped with useful local peripherals, such a power-failure detector, a watchdog timer, two 16-bit timers, and a battery-backed real-time clock complete with calendar. The board requires 5V and draws 70 mA. $795.

Gespac Inc, 50 W Hoover Ave, Mesa, AZ 85202. Phone (602) 962-5559. FAX 602-962-5750. Booth No 1129.

Circle No 638

Half-flash A/D converter handles 20V/µsec slew rates



Featuring on-chip sample-and-hold circuitry, the 8-bit LTC1099 half-flash A/D converter has a 2.5-µsec conversion time and can handle slew rates of 20V/µsec. The total unadjusted error is ±1 LSB.

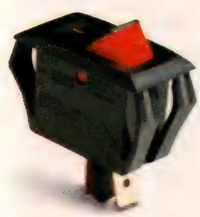
The converter requires few external components for operation: All timing circuitry for the 1099 is internal and edge-sensitive, eliminating the need for external pulse-shaping and -timing circuitry. The data outputs are latched with 3-state control to permit easy interface to a µP data bus or an I/O port. Two modes of operation—Read and Write-Read—also simplify µP interfacing.

The LTC1099 features an overflow output, allowing it to be cascaded for higher resolution systems. There is also a stand-alone mode for applications that do not involve a µP. The converter requires no user trimming and operates from a 5V supply. The analog and reference inputs have a −0.3 to V_{CC}+0.3V range; the digital input range is −0.3 to +12V. Power dissipation equals 75 mW max. The converter is available in plastic or ceramic DIPs, as well as a surface mount package. $8.25 for a unit in a plastic DIP.

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 432-7487. FAX 408-434-0507. Booth No 3800.

Circle No 642

60 years of innovation and we're still not sitting on our rockers.



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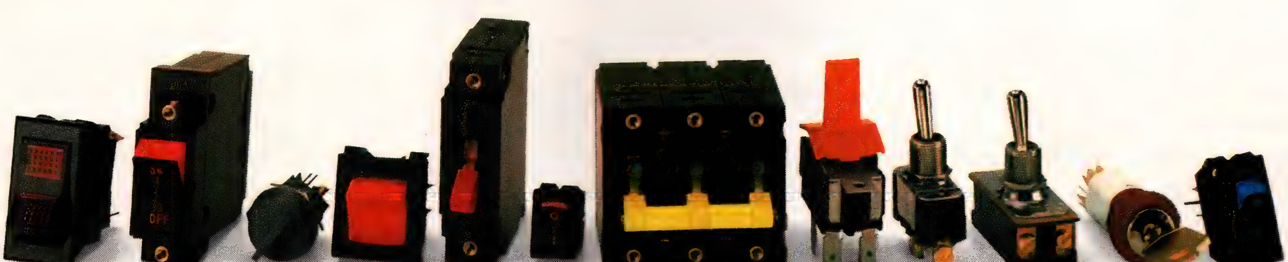


CARLINGSWITCH

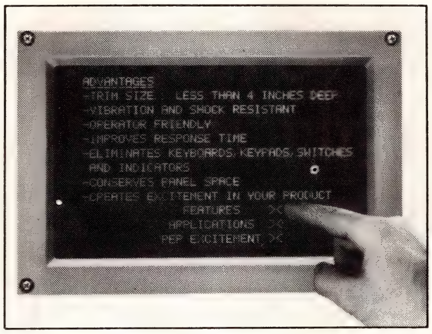
INNOVATION BY DESIGN

CIRCLE NO 195

Touch-entry display modules offer canned-message capability

The model 4284-XX display module combines a 12-line by 40-character dc gas plasma display with an infrared touchscreen. The 16k lithium-battery-backed memory provides as many as 127 canned messages.

The touch-input infrared switch matrix provides 240 active switch locations. The switch matrix uses optical technology, which enhances display appearance. Proprietary techniques help to prevent ambient light from affecting the optical switches.



The 4284-XX's display provides both upper and lower case letters and an expanded ASCII character set that includes scientific and European characters in a 5×7 dot-matrix format. The characters are available in neon-orange or green and are software-dimmable to three levels of brightness.

The module accepts and outputs RS-232C or RS-422 serial data at 1200 or 9600 baud. It supports clear-to-send and data-terminal-ready signals and can detect parity and rate errors in transmission. The module also features a set of jumper-initiated self-diagnostic tests to check the operation of all infrared light beams and to display brightness levels, signify the selected baud and parity rates, check the number of stored messages, and provide battery status. From \$1198 and \$1329 for the neon-orange and green display modules, respectively.

IEE Inc, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311. TLX 4720556. FAX 818-902-3723. Booth Nos 2254 to 2257.

Circle No 641

12-bit, 4-quadrant CMOS D/A converter features on-chip output amplifier

The monolithic AD7845 is a full 4-quadrant multiplying D/A converter that includes an on-chip amplifier. Simple external connections let you configure the unit for either unipolar or bipolar operation as a programmable-gain amplifier (PGA) or as a programmable current souce.

Three matched internal application resistors provide gain ranging and offsetting. TTL- or CMOS-compatible inputs drive the 12-bit latch controlled by standard $\overline{CS}$ and $\overline{WR}$ signals, thus making bus interfacing simple through the use of direct unbuffered operation.

Guaranteed to be monotonic over the full operating range, the AD7845 has a ±1 LSB max differential nonlinearity and a ±2 mV zero code offset error. The on-chip amplifier and feedback resistor perform current-to-voltage conversion with an accuracy to within ±1 LSB. Delivering a ±10V swing into a 2-kΩ load, the internally compensated amplifier settles to 0.01% of the full-scale range in under 5 µsec. The full power bandwidth is 250 kHz, and the unity-gain small-signal bandwidth is 600 kHz with a 7-µsec slew rate.

The AD7845 operates from ±15V supplies and is available in three operating-range grades: 0 to 70°C (J and K grades), −25 to +85°C (A and B grades), and −55 to +125°C (S and T grades). \$7.40 (100) for J-grade versions.

Analog Devices Inc, 804 Woburn St, Wilmington, MA 01887. Phone (617) 935-5565. TLX 924491. Booth Nos 3278 to 3283.

Circle No 640

Stand-alone EPROM, EEPROM programmer requires no personality modules

The EZ-Writer stand-alone multiprogrammer supports all MOS and CMOS EPROMs and EEPROMs ranging to 1M bps and 40 pins without the need for personality modules or adapters. Programming is done internally, and all required voltages and waveforms are generated under software control.

The EZ-Writer features nine function keys for direct command execution. Device operations include Load, Program, Blank Check, Verify Device, Edit RAM Data, Fill RAM, Display Device Data, and Sumcheck RAM/Master. The unit also features two ZIF sockets—one to support 24- to 32-pin memory types and one for 40-pin EPROMs.

Four operating modes are available: stand-alone programming, including Data Editing using an integral 25-position keyboard and a 40-character alphanumeric LCD; terminal remote-control mode, using the standard serial RS-232C; computer remote-control mode via the RS-232C and the five translation formats; and menu-driven operation, using an optional PC-compatible software driver.

The EZ-Writer offers three choices for selecting a device for programming: You can scroll through a menu of manufacturers and device numbers, directly enter the device code, or use an (E)EPROM electronic identifier. The device also features a nonvolatile memory to save default parameters as well as power protection for chips in the ZIF sockets. From $975.

Bytek Corp, 508 NW 77th St, Boca Raton, FL 33487. Phone (407) 994-3520. FAX 407-994-3615. Booth No 4003.

Circle No 643

Personal-computer clock battery offers long life, low cost

The Model 844 battery utilizes a 4.5V, 1-Ahr alkaline system and can replace the lithium battery that comes with IBM PC/AT computers.

These clock batteries maintain power to the clock chip when the computer is turned off. They also maintain the memory of the chip to prevent the loss of the computer's system-configuration information.

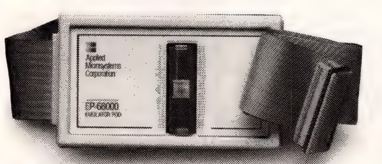
The 844 features a 4-pin termination that lets it directly replace the original lithium battery in most 80286 and 80386 μP-based systems. Unlike the 6V OEM lithium batteries, the 844 employs no internal voltage-dropping resistors. Because of this difference, the 844 has an expected lifetime of two to four years. $18.

Rayovac Corp, 601 Rayovac Dr, Madison, WI 53711. Phone (608) 275-4912. Booth No 1496.

Circle No 644

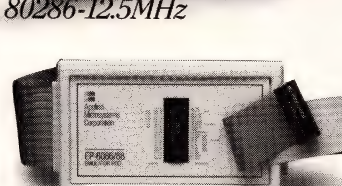
68020 EMULATION NOW AT 25MHz.

68020-25MHz



68000-16.7MHz

80286-12.5MHz



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In Europe contact Applied Microsystems Corporation Ltd., Chiltern Court, High Street, Wendover, Aylesbury, Bucks, HP22 6EP, United Kingdom. Telephone 44-(0)-296-625462. FAX 44-(0)-296-623460.
In Japan, contact Applied Microsystems Japan Ltd., Nihon Seimei, Nishi-Gotanda Building, 7-24-5 Nishi-Gotanda, Shinagawa-KU, Tokyo T141, Japan. Telephone 03-493-0770. FAX 03-493-7270.

AMC 247

CIRCLE NO 197

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Cubit Model 8020 CPU Board—
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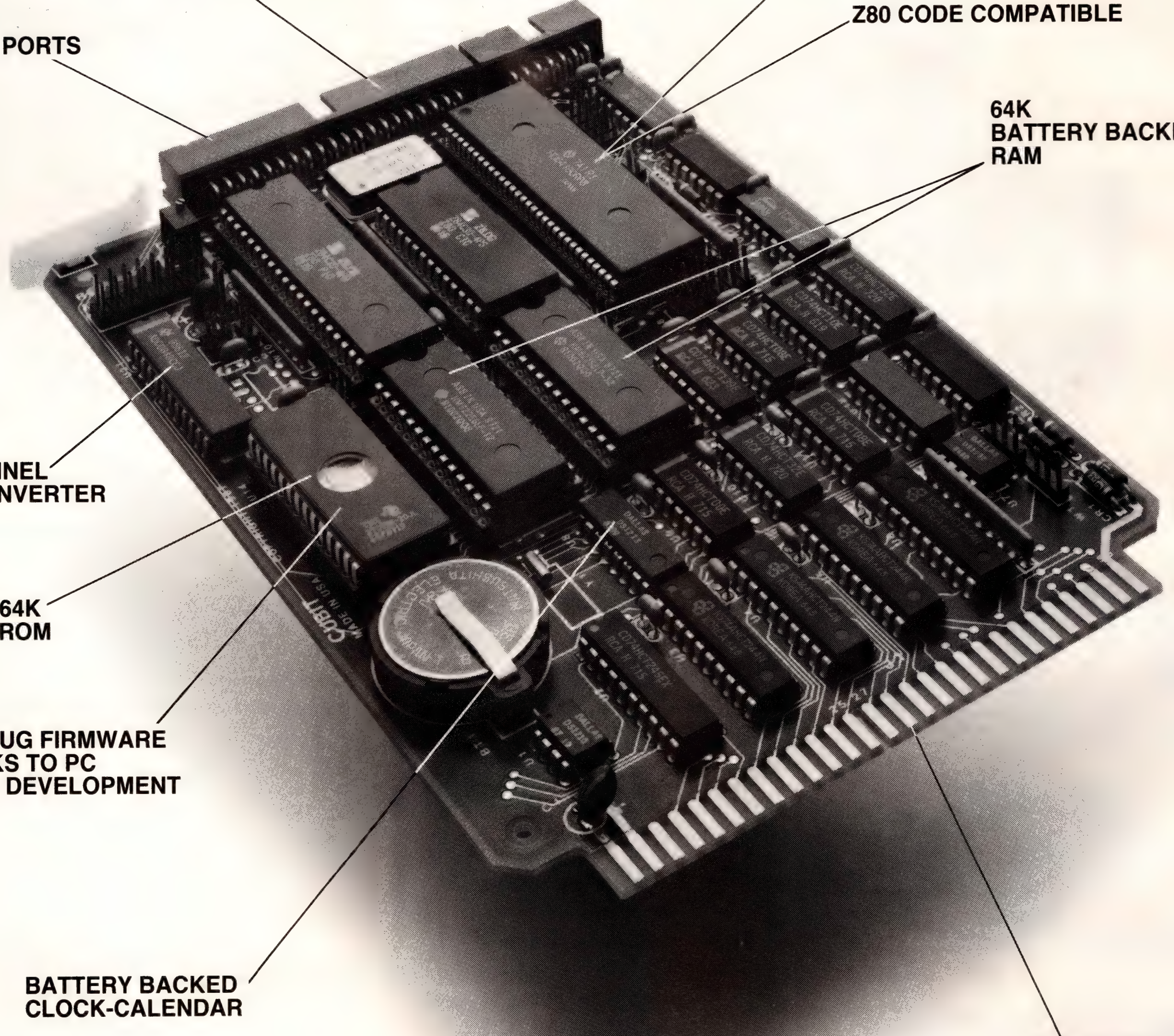
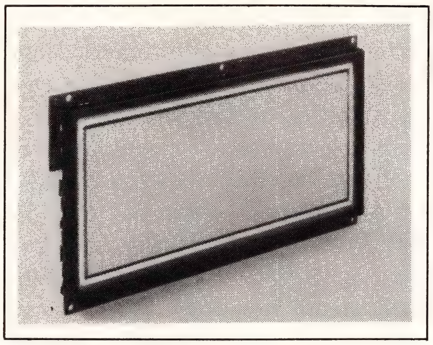


CµBIT DIVISION OF PROTEUS INDUSTRIES

190 South Whisman
Mountain View, CA 94041-1577
(415) 962-8237

CIRCLE NO 198

Wescon/88 Products



EL DISPLAY

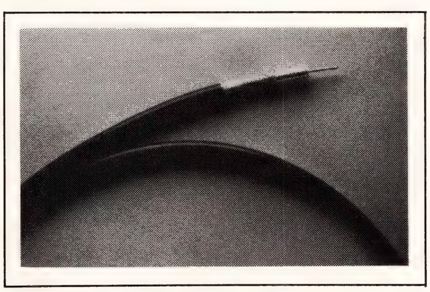
These display panels use dc electroluminescent technology to achieve high reliablility and long life. The use of dc technology and proprietary drive circuitry eliminates the chance of catastrophic failures.

Two basic units are available, both with a 640×200-pixel matrix: the EL 1C-B000, which has a 2:1 aspect ratio, and the 1C-A000, which has a 1.4:1 aspect ratio. The width of the total package, including the display and the drivers, is less than 0.6 in.

Both display modules offer flicker-free imaging, high resolution, wide viewing angles, and a uniform brightness. $800 for either configuration.

Cherry Electrical Products, 3600 Sunset Ave, Waukegan, IL 60087. Phone (312) 360-3500. Booth Nos 1440 to 1448.

Circle No 610



NETWORK CABLES

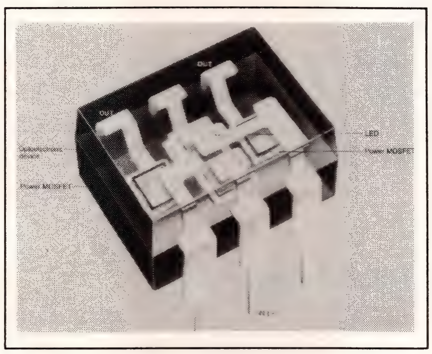
The 1223A and 1224A 75Ω coaxial cables are designed for manufacturing automated protocol (MAP) networks. Both meet IEEE MAP requirements and are CL2X rated.

Designed for drop applications from the cable trunk to individual work stations, the 1223A cable features an 18 AWG solid copper-covered steel conductor and a black PVC jacket. The 1224A accommodates both trunk-cable and drop-cable applications and features a 14 AWG conductor.

Both cables employ a shield that consists of a double-layer of foil bonded to the dielectric core, followed by an aluminum-braid shield and then an overall copolymer mylar foil. The outer foil has a shorting fold, which provides metal-to-metal contact for maximum shield effectiveness. Both cables are available in 1000-ft put-ups. $220.65 and $377.25 for the 1223A and 1224A, respectively.

Belden Wire and Cable, Box 1980, Richmond, IN 47375. Phone (800) 235-3364. Booth Nos 2455 to 2463.

Circle No 611



RELAYS

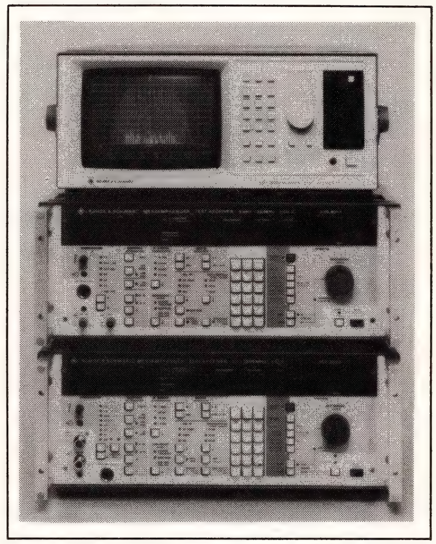
Photo-MOS relays employ state-of-the-art technology that incorporates the advantages of both electromechanical and solid-state relays. They feature an optoelectronic element that directly drives a power MOSFET, thus eliminating the need for a power supply. The optoelectronic element converts received light to voltage to drive the power FET, allowing the FET to switch the load on and off.

The relays can control loads of 150 mA at a peak load voltage of 400V. And, despite their small size (a 6-pin DIP measuring 0.369×0.252 in.), the Photo-MOS relays feature a 1500V ac min input-to-output isolation rating.

You can mount the relays in any position; and, since they are unaffected by magnetic fields, they are compatible with applications involving high packing densities. Photo-MOS relays are available in tube packaging to accommodate automatic insertion equipment needs. From $4.50 (500). Delivery, eight to 12 weeks ARO.

Aromat Corp, 629 Central Ave, New Providence, NJ 07974. Phone (201) 464-3550. Booth Nos 1544 to 1548.

Circle No 612



TEST SYSTEM

Covering a 20-Hz to 1300-MHz frequency range, the EP-6 EMI test system conforms to the latest requirements of MIL-STD 461/462, FCC, and VDE. It uses crystal-based synthesized receivers rather than spectrum analyzers to meet the exacting VDE receiver specifications.

The EP-6 features menu-driven soft keys for ease of operation, audio and visual interference identification, color-monitor capability for display clarity, a printer, and a plotter for historical records.

Measurements are presented in direct physical units—there's no need for antenna-factor or bandwidth conversions. Full IEEE-488 capability is standard. The EP-6 is

backed by a full line of active and passive probes, antennas, and line-impedance stabilization networks. \$82,000. Delivery, 12 weeks ARO.

Rohde & Schwarz Inc, 4425 Nicole Dr, Lanham, MD 20706. Phone (301) 459-8800. TWX 510-223-0414. FAX 301-459-2810. Booth Nos 3138, 3140.

Circle No 613

RELAYS

The CT2100 solid-state relay module is designed to interface a computer system to the outside world where hostile signal environments present an operational hazard to the electronic system.

Designed for direct μP access and control, the CT2100 features four independent solid-state relays. The isolation between the switches and between the control inputs is 1500V, and an isolated status line indicates overcurrent trip or current flow.

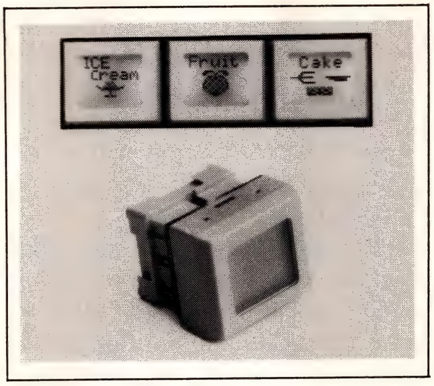
The relay switches are designed to withstand electromagnetic pulses and are self-protected for overcurrent conditions. The module operates from a 5V supply, and the switches can operate as high- or low-line drivers. The continuous current rating is 200 mA, the trip level is 2 to 3A, and the sense-current flow is 25 mA min. \$1300. Delivery, 12 weeks ARO.

Circuit Technology Inc, 160 Smith St, Farmingdale, NY 11735. Phone (516) 293-8686. Booth Nos 2292, 2294.

Circle No 614

SWITCH MODULE

These switch modules integrate a custom IC driver and a low power LCD that utilizes super-twist technology in the keycap of an spst, momentary-contact switch. The high-contrast super-twist LCD consists of 864 pixels in a 24×36-pixel matrix and is enhanced by LED backlighting for low ambient lighting conditions.



The LCD provides full-screen graphic displays. If used as a 5×7 dot-matrix alphanumeric display, it provides three lines of as many as six characters per line. The ⅞×¾-in. switch module is designed for through-the-panel pc-board mounting and requires only ¾ in. behind the panel-mounting area.

Designed to operate over a 0 to 40°C range, these low contact-resistance (less than 1Ω) switch modules have an average life of greater than 10^6 operations. \$40.72 (100).

IEE Inc, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311. TLX 4720556. FAX 818-902-3723. Booth Nos 2254 to 2257.

Circle No 615

OSCILLOSCOPE

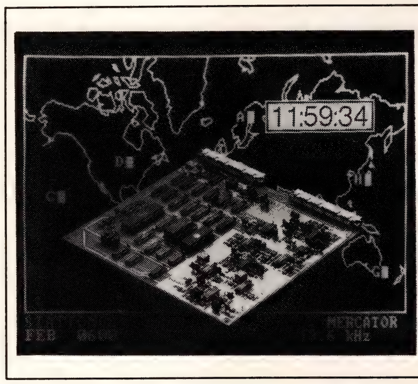
The VP-5516A oscilloscope offers analog power with digital intelligence. The 100-MHz, 4-channel unit features a novel 3-dimensional video display that is well-suited for the analysis of complicated waveforms.

Other major features include 23 types of digital readout functions that display measured values and measurement conditions, 1-step rise- and fall-time calculations, a yes/no decision function for screening input signals, and a one-touch repeat-measurement capability.

A labeling function (full alphanumeric plus symbols) allows you to mark the waveforms with data, location, and comments. Six cursor lines and two cursor symbols provide as many as 10 types of waveform measurements. The simple menu operation saves time and enhances accuracy, and an auto-ranging function optimizes the waveform size for best viewing. \$2195. Delivery, stock to six weeks ARO.

Panasonic Industrial Co, 50 Meadowlands Parkway, Secaucus, NJ 07094. Phone (201) 348-7000. Booth Nos 3548, 3550.

Circle No 616



RECEIVER

The OM-PCB timing receiver is accurate to within 0.001 sec. You can configure the single-board unit for most any application requiring either UTC traceable time or time synchronization between widely separated sites.

Unlike some OEM-type receivers, the OM-PCB integrates directly into your equipment and provides a precise reference at any location in the world. Designed to receive and process the very low frequency signals broadcast from the global network of navigational transmitters, the unit can provide time outputs in a wide range of formats.

By incorporating a μP controller and receiver/decoder design, both the size (less than 81 in.^{2}) and the power consumption (less than 200 mW) of the OM-PCB are kept to a minimum. \$1300.

Kinemetrics/Truetime, 3243 Santa Rosa Ave, Santa Rosa, CA 95407. Phone (707) 528-1230. TLX 176687. FAX 707-527-6640. Booth No 3360.

Circle No 617

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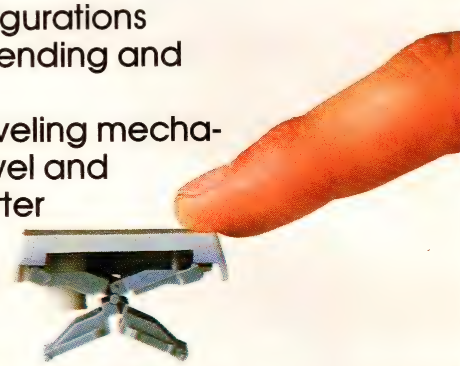

Preh E.R.O.S. Keypads are also completely dustproof and waterproof* for use in environmentally difficult applications such as public access, retail systems and manufacturing. A custom grid and overlay turns the E.R.O.S. Keypad into a sealed, flat unit with full-travel keys…available only from Preh.

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*Per IP-65 (DIN Standard 40050)

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Preh Electronic Industries, Inc.
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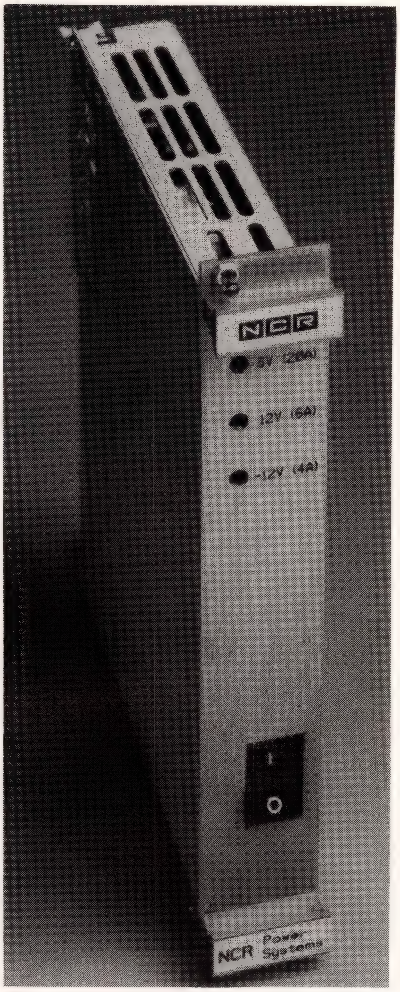
CIRCLE NO 199



POWER SUPPLY

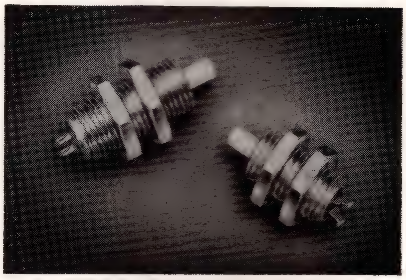
These dedicated 200W power supplies are designed for systems utilizing VME bus architectures. The devices feature a TTL-compatible open-collector signal that verifies in-spec performance within 500 msec after turn-on.

Remote control is accomplished by using a 2.4V dc TTL signal as the Enable and an open-collector signal as the Disable. Three outputs (5V, ±12V) are standard, and the calculated MTBF is 50,000 hrs. The supplies comply with DIN-41494 for Eurocard packaging as well as the stringent safety and EMI requirements imposed by UL, CSA, and TUV (VDE).

The supplies interface with the VME bus via a direct plug-in connection. Standard supplies accommodate most applications, but the units can be easily factory customized to comply with special system conditions. $277 (1000).

NCR Corp, 3200 Lake Emma Rd, Lake Mary, FL 32746. Phone (407) 323-9250. Booth Nos 2815, 2816.

Circle No 618



LIMIT SWITCHES

Series 39 miniature limit switches include a plunger seal, which prevents contact contamination when operating in harsh environments. The switches are available in spst NO (39-701) and spst NC (39-702) contact configurations.

The overall length of Series 39 switches is less than 1 in., and the diameter, including the mounting nuts, is less than 0.5 in. The fully threaded switch body allows users to accurately adjust the operating point. The 39-701 switches 150 mA at 5V dc; the 39-702 switches 250 mA at 115V ac.

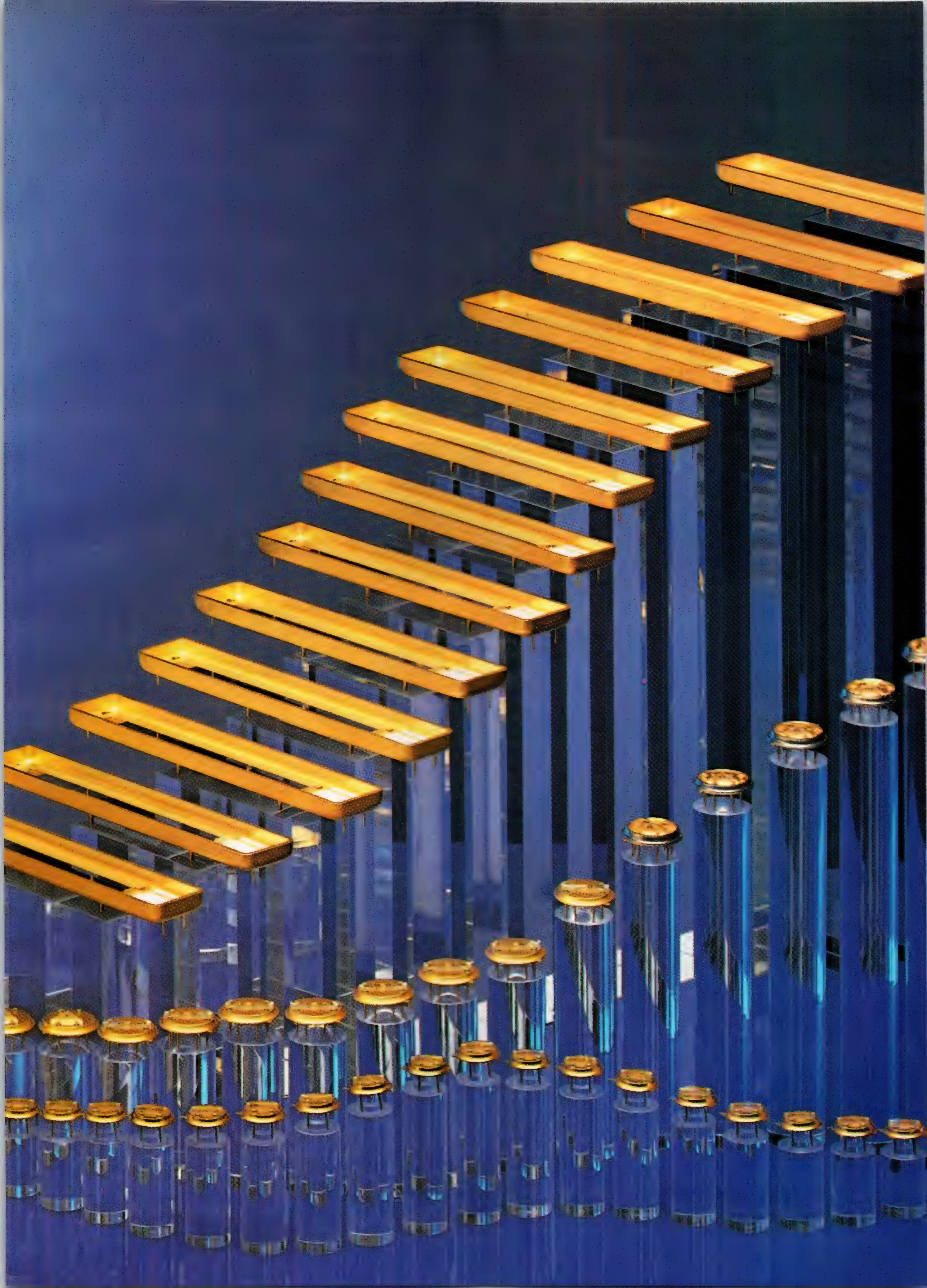
For resistive loads, both versions have a 100,000-operation lifetime. The contact resistance measures 25 mΩ max on a new switch, and the actuating force is 12±4 oz for NO models and 8±4 oz for NC models. $4.43 (100) for the 39-701; $5.10 for the 39-702.

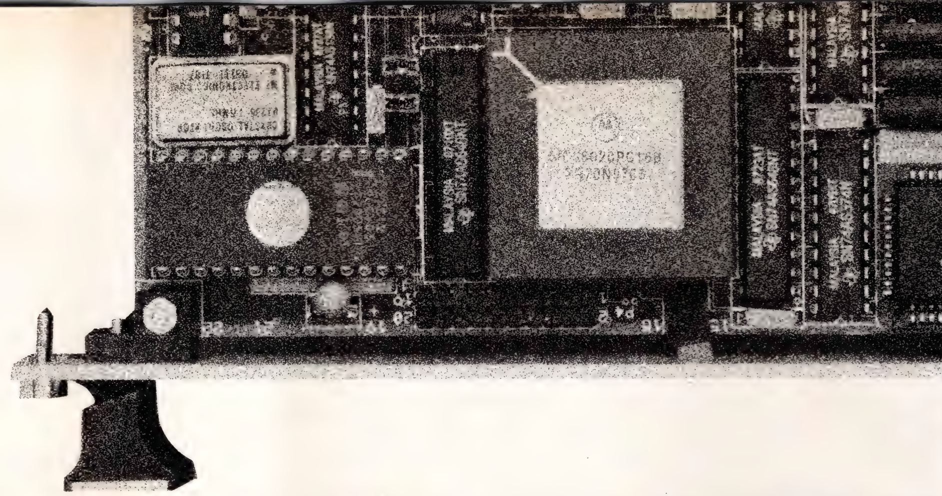
Grayhill Inc, Box 10373, LaGrange, IL 60525. Phone (312) 354-1040. TLX 6871375. FAX 312-354-2820. Booth Nos 2032, 2034.

Circle No 619

BACKPLANES

J1/J2 VME Bus backplanes combine the J1 and J2 sections into a 1-piece construction to provide a more stable ground reference for 32-bit ap-





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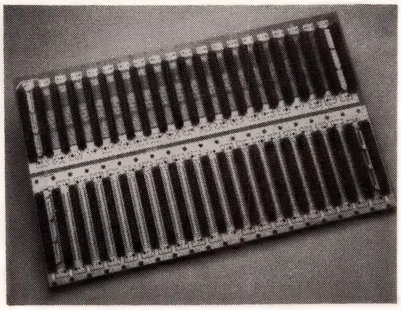
CIRCLE NO 201



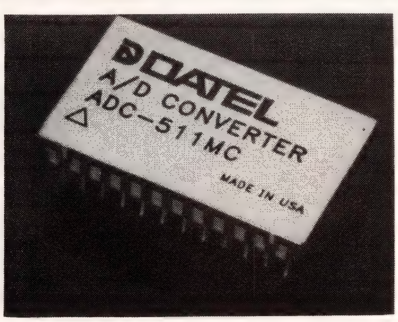
plications. This construction also eliminates the potential for ground loops.

Designed to meet revision C.1 of the VME Bus spec, the J1/J2 backplane utilizes on-board termination. The line includes 21-, 15-, 10-, and 5-slot designs; and power terminals are available in three styles: power cubes, press-fit posts, and snap-on lugs. Press-fit DIN connectors come standard.

J2 connector shrouds with latching arms to firmly secure I/O cabling are available as an option. Four auxiliary power buses are included in the J2 area to handle multiple power requirements in special VME Bus applications. $907.75 and $1200 for the 15- and 21-slot versions, respectively.

Augat Inc, Box 779, Attleboro, MA 02703. Phone (508) 222-2202. TWX 710-391-0644. Booth Nos 2354 to 2363.

Circle No 620



A/D CONVERTER

The ADC-511 A/D converter provides high-speed, 12-bit conversion with reduced power. The unit dissipates just 925 mW and needs only 1 μsec for the 12-bit-accurate conversion process.

Functionally complete, the ADC-511 contains an internal clock and an internal reference that can supply 10V at 1.5 mA externally. All digital inputs and 3-state outputs are CMOS/TTL compatible. The output coding can be in straight binary, offset binary, complementary binary, or complementary offset binary.

A pin-programmable feature allows you to select inputs of 0 to 10V or ±5V. Packaged in a 24-pin DIP, the ADC-511 requires ±15V and 5V supplies and is available in both commercial and military versions. $99 (1000).

Datel Inc, 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. TWX 710-346-1953. Booth Nos 3030 to 3034.

Circle No 621

DISPLAY

The SealTouch is a VT-220 compatible, NEMA 4 and 12 rated touch-screen terminal designed to withstand harsh industrial environments. The design encases a 9-in. electroluminescent flat-panel display with infrared touch interaction in a completely sealed cast-aluminum housing.

To prevent contamination, the terminal employs no fans or filters. The solid-state display is inherently resistant to magnetic interference, shock, and vibration. VT-220, VT-100, and VT-52 emulations are all

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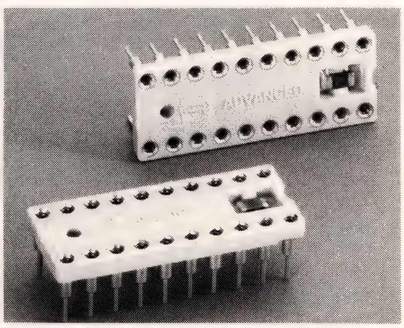
standard; and the unit features easy, 1-finger programming set-up using menu screens.

SealTouch's display capabilities include 80-line × 25-character format, line graphics, down-loadable fonts, pop-up touch menus, and full on-screen touch keyboards. The terminal can connect with RS-232C, RS-422, or RS-485 interfaces using multidrop protocols. A 20-mA current interface is optional. $3950.

Digital Electronics Corp, 31047 Genstar Rd, Hayward, CA 94544. Phone (415) 471-4700. TLX 172073. FAX 415-489-3500. Booth Nos 2175, 2177.

Circle No 622



IC SOCKETS

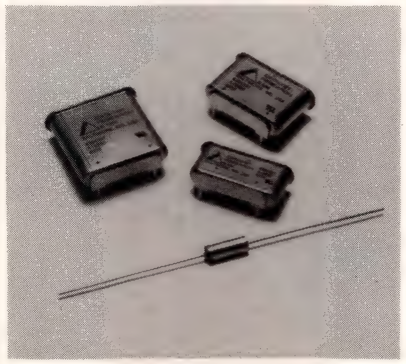
MDS Series decoupling capacitor IC sockets feature molded-in copper circuits with committed voltage and ground terminals. These terminals are designed to provide highly reliable electrical performance and thermal conductivity.

Available in 14- through 20-pin standard DIP configurations, the MDS sockets feature a thermoplastic body material that carries a 94V-0 UL rating. The socket design also features a flush top to accommodate robotic pick-up (vacuum or mechanical) equipment. The chip capacitor, which is surface mounted within the socket body, is available in values of 0.1, 0.01, and 0.33 μF.

The sockets are supplied with screw-machine terminals, which are 100% antisolderwicking and available in several plating versions. The sockets employ a 4-fingered contact design for high reliability and are available in versions that have 0.095-, 0.120-, and 0.165-in. above-the-board mounting heights. $2.09 (100) for a 20-pin model. Delivery, stock to six weeks ARO.

Advanced Interconnections, 5 Energy Way, West Warwick, RI 02893. Phone (401) 823-5200. FAX 401-823-8723. Booth Nos 3189, 3191.

Circle No 623



BATTERIES

The B-35 μPowercell 2.8V lithium iodide cell resembles a standard ½W resistor in size, shape, and packaging. Designed as a backup for CMOS RAM, its tape-and-reel packaging is compatible with automatic insertion equipment.

Each B-35 cell has a 35 mAHr capacity rating and can deliver a full power output of 10 μA at 2V min at room temperature. As the RAM leakage current varies with the temperature, the cell tracks the variation and makes appropriate corrections. The total cell energy is available over the cell's operational life.

The cell features a true hermetic glass-to-metal insulator/seal and metal-to-metal case construction. The current limiting qualities of lithium iodide minimize outgassing, overheating, and venting problems in the event of electrical abuse, such as shorts, forced discharge, and overcharge.

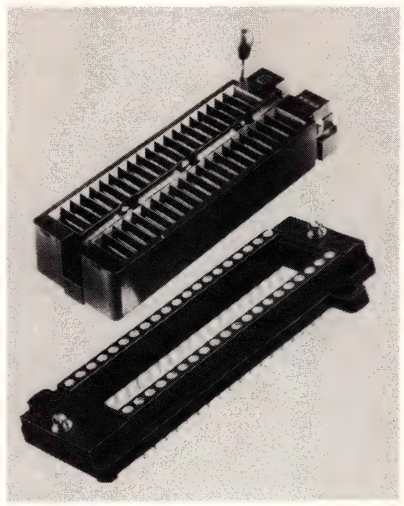
The operating range for the B-35 cells extends from −55 to +125°C. The units meet all MIL spec 883

Wescon/88

requirements. From $3.

Catalyst Research, 1421 Clarkview Rd, Baltimore, MD 21209. Phone (301) 296-7000. Booth No 3286.

Circle No 624



TEST SOCKETS

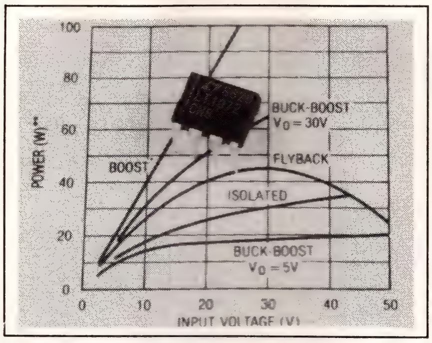
Available for both test and burn-in applications, these ZIF sockets are available in 24- to 48-pin sizes. Depending on the plating/material specified, the contacts can withstand temperatures as high as 105 (tin over beryllium copper), 150 (gold over beryllium copper), or 200°C (NiB over CuNiSn spinodal alloy).

The broad entry area allows you to test ICs with 0.3-, 0.4-, or 0.6-in. pin-to-pin centers in one socket. The contacts are designed to be normally closed for consistent force. The plastic socket bodies carry a 94V-0 UL rating.

Additional specs include a $10^9\Omega$ insulation resistance, a 1000V ac min dielectric withstanding voltage, a 1A current rating, and a minimum life of 50,000 cycles. The sockets mount on pc boards with 0.3- or 0.6-in. center hole patterns. $3.87 (100) for a 24-pin, tin-plated version.

Aries Electronics Inc, Box 130, Frenchtown, NJ 08825. Phone (201) 996-6841. FAX 201-996-3891. Booth Nos 2189, 2191.

Circle No 625



VOLTAGE REGULATOR

Housed in an 8-pin plastic mini-DIP, the LT1072 synchronizable switching voltage regulator operates over a 3 to 10V range and features an on-chip 1.25A switch. The internal design allows you to synchronize multiple regulators with a system clock in the 48- to 70-kHz range.

The LT1072 uses an adaptive antisaturation switch drive to accommodate a wide range of load currents. The regulator operates in a variety of standard switching configurations, including buck, boost, flyback, forward, and inverting. To minimize application problems, the 8-pin device includes all oscillator, control, and protection circuitry on chip.

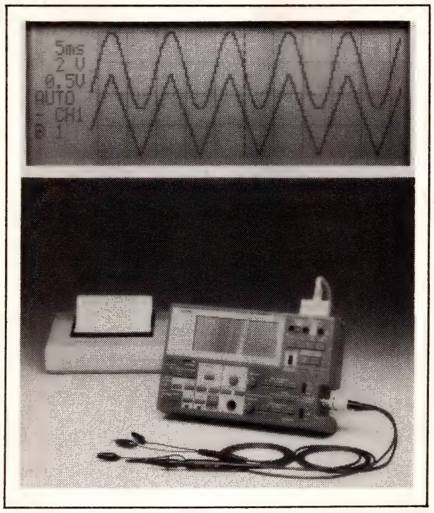
The chip also contains the circuitry for developing a fully isolated flyback regulator—no optocouplers or extra transformer windings are needed. An externally activated shut-down circuit on the LT1072 chip reduces the total supply current to 50 μA for standby operation. $2.35 (100).

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 432-1900. FAX 408-434-0507. Booth No 3800.

Circle No 626

DSO/DMM

The Model 200 portable digital storage oscilloscope (DSO)/digital multimeter (DMM) provides two channel operation. This capability allows two-channel comparisons and the addition or subtraction of two signals, as well as X-Y operation.

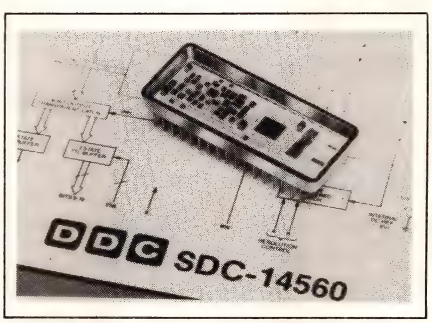


The scope section has a 3M-sample/sec capability and offers autoranging. The unit lets you store three waveforms per channel in a battery-backed memory. You can also use ac to run the unit. The scope features an on-screen display of setting conditions, which include sensitivity, time base, trigger source and slope, and display mode.

The autoranging DMM has a manual override as well as audible continuity and overload indicators. This section of the unit offers ac and dc current and voltage measurement functions as well as resistance. There's also a low-ohm mode that provides a lower test voltage for resistance measurements. $1645.

Leader Instruments Corp, 380 Oser Ave, Hauppauge, NY 11788. Phone (516) 231-6900. TWX 510-227-9669. Booth Nos 3343 to 3349.

Circle No 627



S/D CONVERTERS

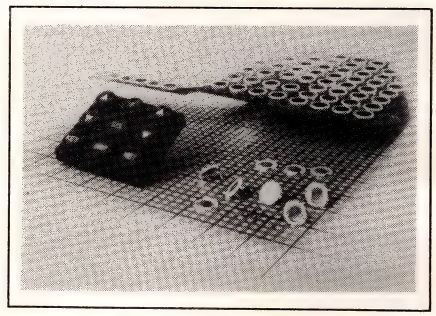
SDC-14560 synchro-to-digital converters feature user-programmable resolution. They provide the precise positioning attainable at 16-bit resolution and the fast tracking of a 10-bit device in a 36-pin DIP.

The converter's active-selection design allows you to change resolution during converter operation. An analog velocity output of 0 to ±10V and a linearity of 0.25% are provided, negating the need to use a tachometer. The SDC-14560 converters accept broadband inputs—360 to 1000 or 47 to 1000 Hz.

The converters are available in versions that have operating ranges of 0 to 70 and −55 to +125°C. Units are also available that offer full compliance to MIL-STD-883. $345. Delivery, 120 days ARO.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 563-5678. TWX 3106852203. FAX 516-567-7358. Booth Nos 1528, 1530.

Circle No 628

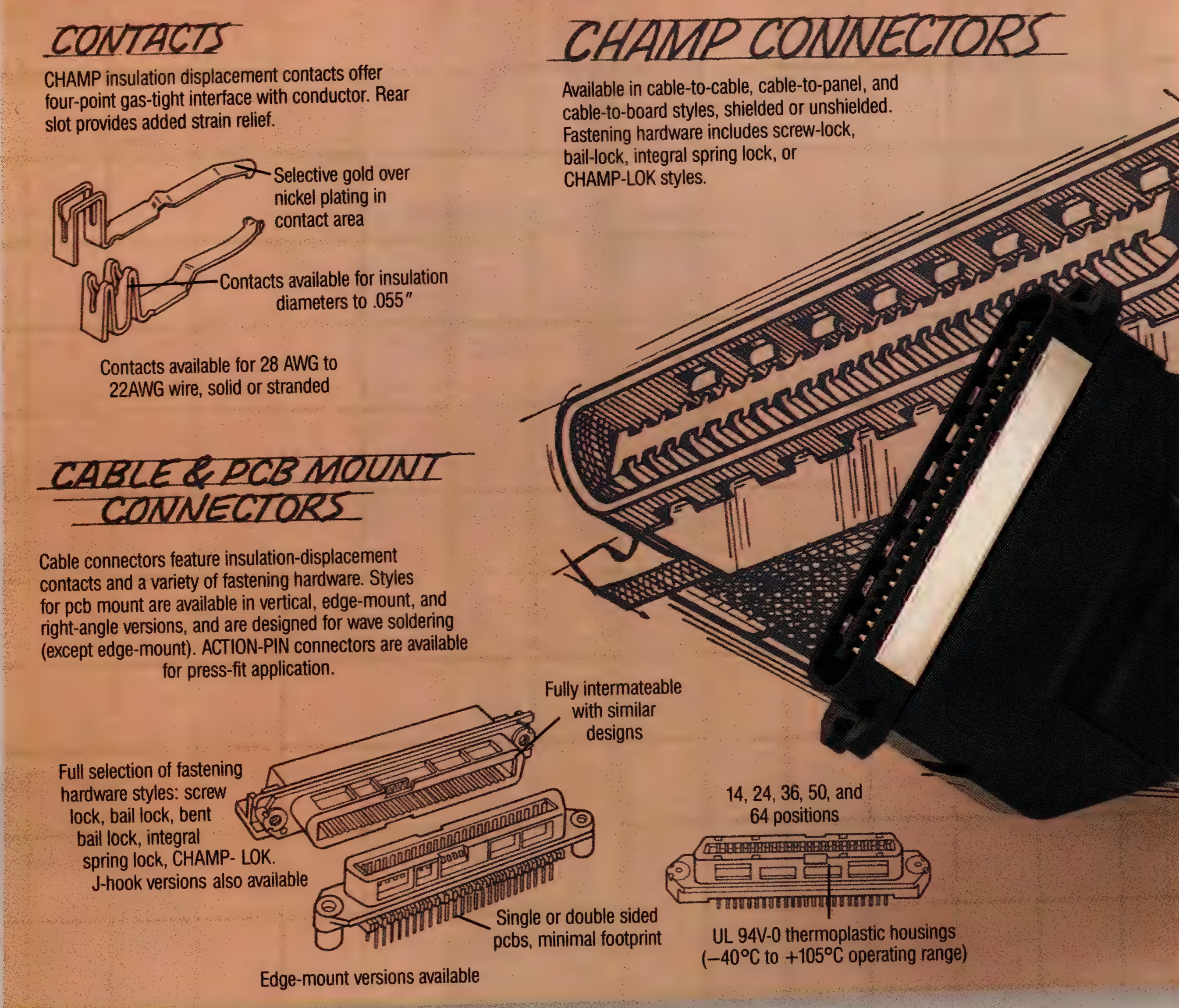


SWITCH

Designed for flat-panel keyboard applications, the ED multidome switch combines a stainless-steel snap dome with a low-profile gold-contact keyswitch. The added dome increases the normal actuation force to 600 grams.

The gold-contact ED disk switch features a wiping-action contact closure to improve reliability. The switch is sealed against particulate contamination to withstand harsh environments.

Electrically, the ED multidome switch has a 50-mA switching-current rating, a 100V dc voltage rating and a 3W power capability. The minimum operating life at full



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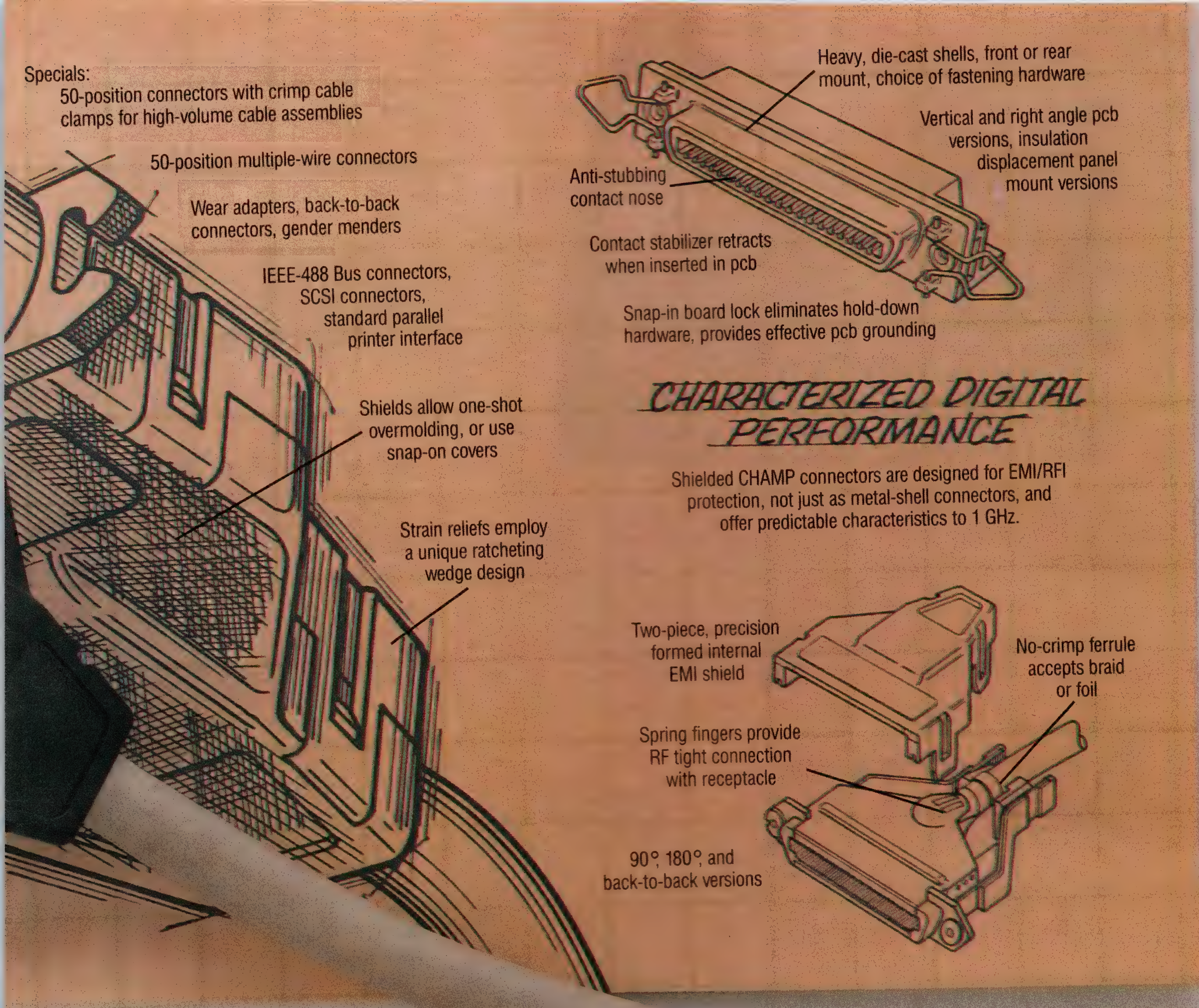

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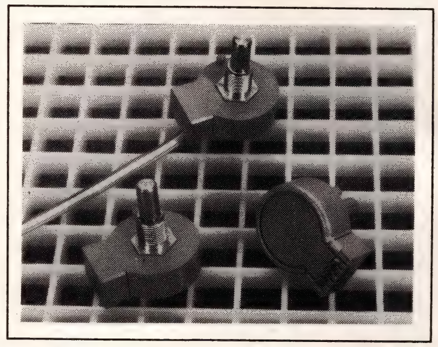

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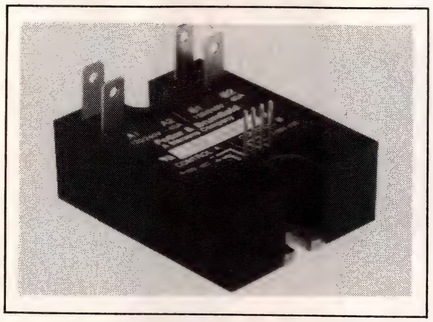

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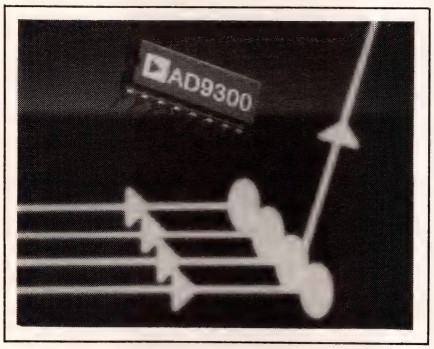

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The AD9300 operates from ±10 to ±15V supplies. Its power consumption is 300 mW typ at ±12V. Three package/temperature versions are available: ceramic-DIP packages (16 pin) for operation over 0 to 70 and −55 to +125°C and a 20-pin LCCC for operation over −55 to +125°C. $8 (100) for commercial-grade units.

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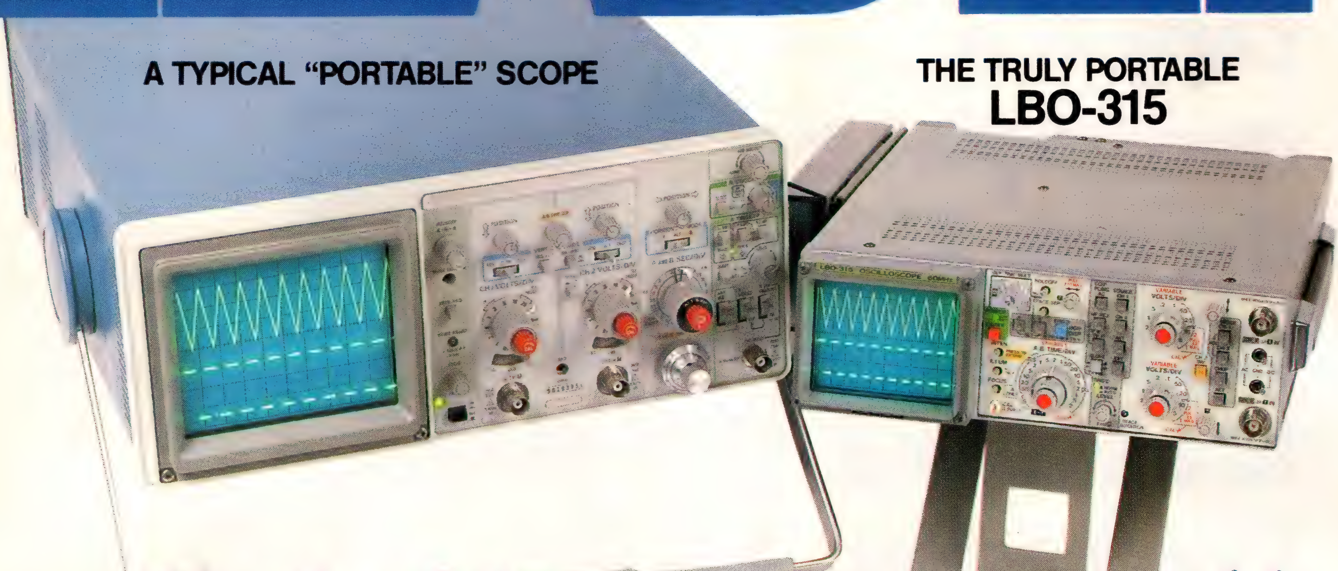

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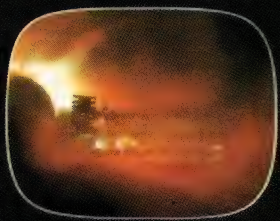

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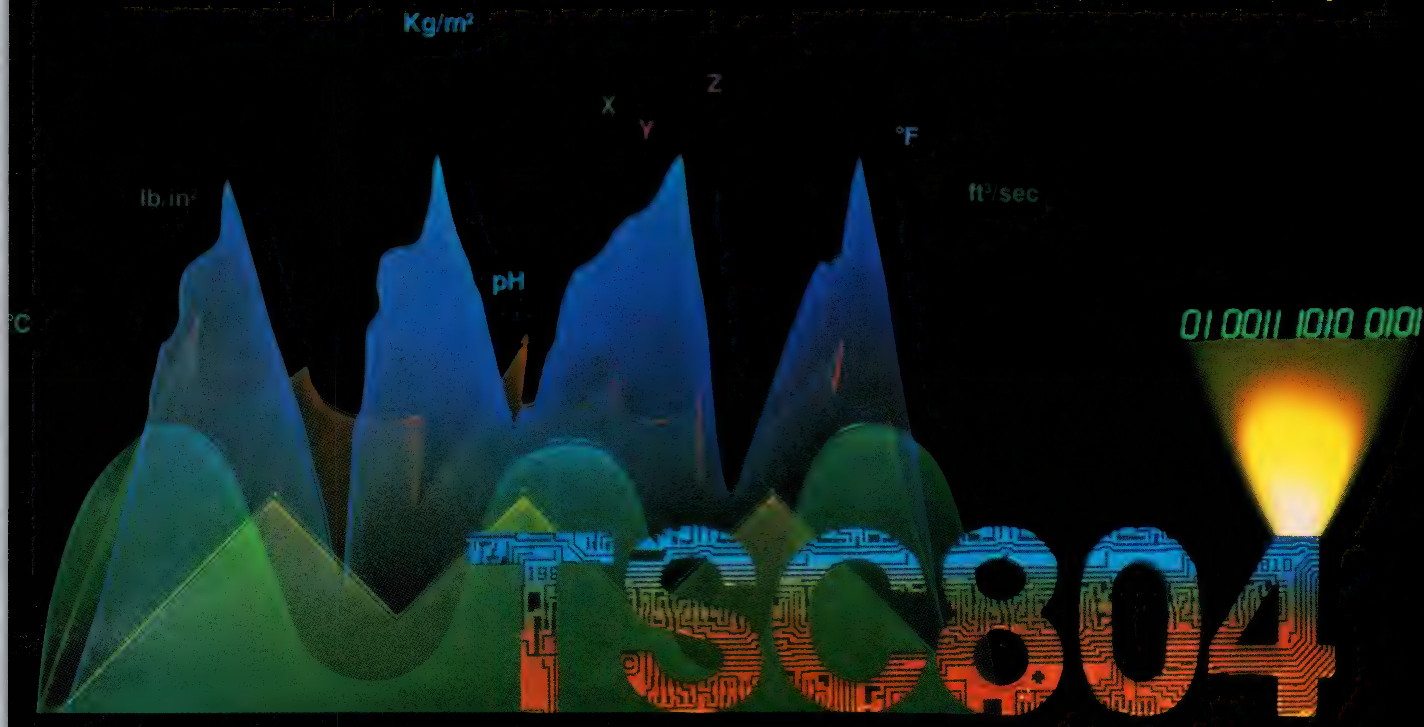

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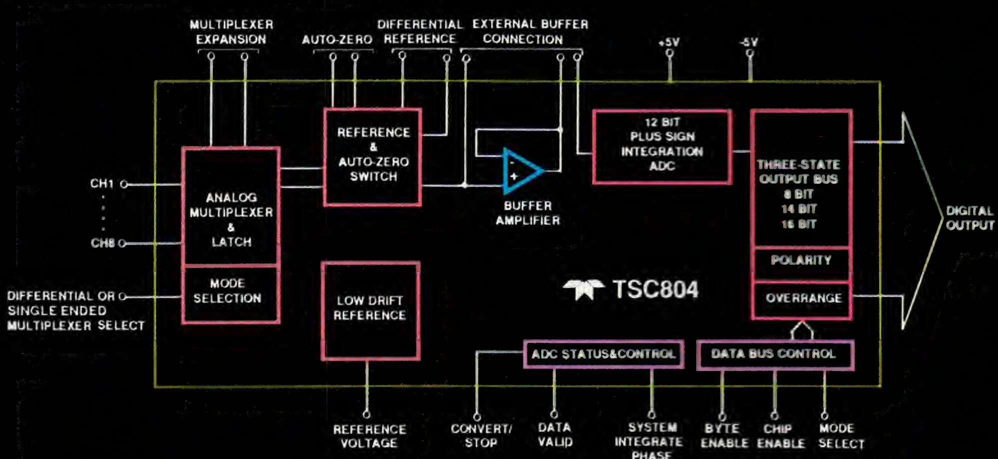

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CIRCLE NO 209

Design dc/dc converters for power conservation and efficiency

This article, part 3 of a 4-part series, will demonstrate design techniques for optimizing power conservation, efficiency, and wide input range in dc/dc converters. Parts 1 and 2 of this series covered the design of 5- to ±15V converters and the proper use of instrumentation in converter design. Part 4 will show how to replace inductors with switched-capacitor techniques in dc/dc-converter designs.

Jim Williams and Brian Huffman,
Linear Technology Corp

At first glance, converter power drain, efficiency, and input range might seem an odd threesome. In portable applications, however, power drain and efficiency go hand in hand. And wide-input-range capability is often closely related to both these parameters. In applications where space or reliability are major considerations, it's sometimes best to operate circuitry from a single 1.5V cell. This objective eliminates almost all ICs as design candidates. Although it's possible to design circuitry that runs directly from a single cell, a dc/dc converter with a wide input-range capability allows you to use standard higher-voltage ICs.

Fig 1's design converts the output of a 1.5V cell to a 5V output and features quiescent current of only 125 μA. Oscillator IC_{1a}'s output—trace D in **Fig 1b**—is a 2-kHz square wave. This circuit has a conventional configuration, with one exception: The biasing scheme accommodates the narrow common-mode range available with the 1.5V supply. To maintain low power, IC_{1a}'s integrating capacitor has a small value, which limits the swing to only 50 mV. IC_{2a} and IC_{2b} operate in parallel to drive T_1. This parallel connection minimizes saturation losses.

When the 5V output (trace A) slopes down far enough, IC_{1b}'s output goes low (trace B) and pulls the noninverting inputs of both IC_{2a} and IC_{2b} close to ground. IC_{1a}'s clock signal now forces energy into T_1. T_1's flyback pulses, rectified and stored in the 47-μF capacitor, form the converter's dc output. IC_{1b} on-off modulates C_2 at whatever duty cycle is necessary to maintain the converter's 5V output. The LT1004 serves as a reference, and the resistor divider at IC_{1b}'s positive input sets the output-voltage level. The Schottky clamp at IC_2's outputs prevents any parasitic behavior of T_1 from developing negative-going overdrives.

The LT1004's output is bootstrapped to the 5V output so that the converter can operate with inputs as low as 1.1V. The 10-MΩ bleed resistor ensures circuit start-up, and the 1-MΩ resistors divide the 1.2V reference to keep IC_{1b} within common-mode limits. IC_{1b}'s positive feedback establishes hysteresis of about 100 mV, and the 22-pF capacitor suppresses high-frequency oscillations.

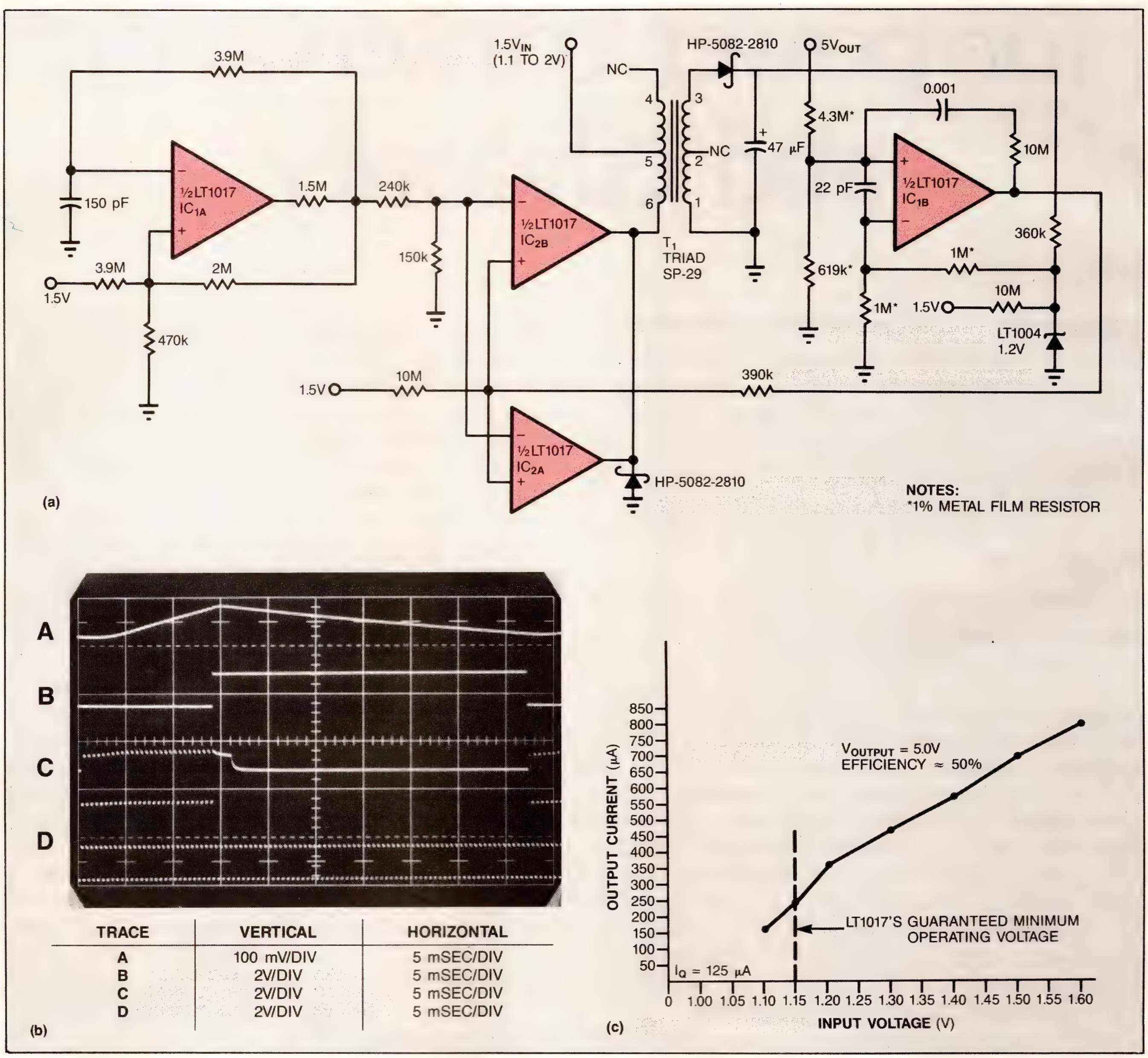
This circuit's low duty cycle at light loads minimizes quiescent current. The 125-μA figure noted is quite close to the LT1017's steady-state currents. As the

In small portable computers, converters must operate from a battery input with very high efficiency.

load increases, the duty cycle increases to meet the demand, drawing more power from the battery. A decrease in the battery's output voltage produces similar behavior.

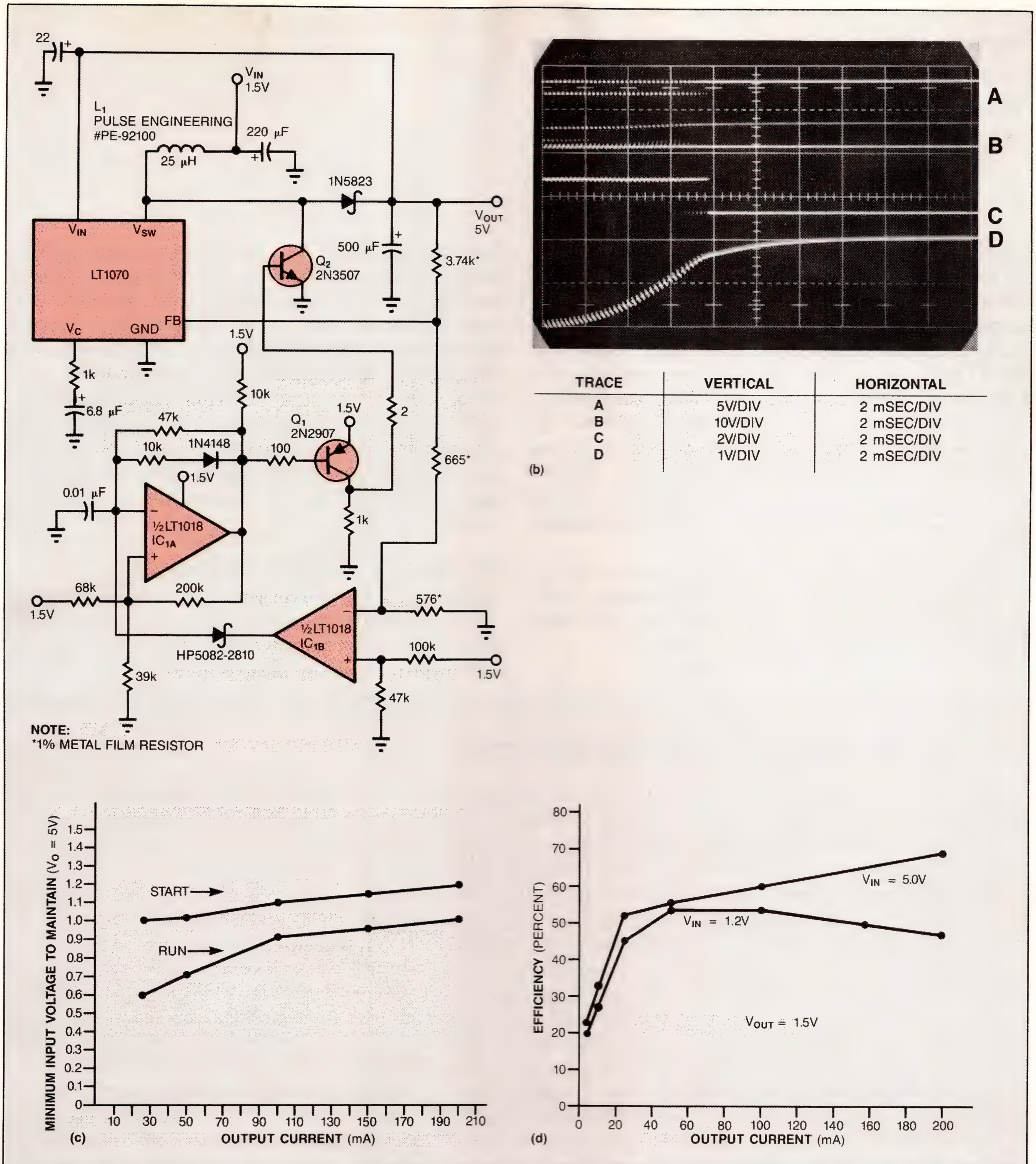
Fig 1c plots the available output current versus the battery voltage for **Fig 1a**. Predictably, the highest power is available from a fresh cell, although the circuit maintains regulation to 1.15V for 250-μA loading. Because of the low supply voltage, it's difficult to control the saturation and other losses in **Fig 1**'s circuit. As a result, the circuit's efficiency is only about 50%.

Fig 1's circuit is useful in low-power applications, but some 1.5V systems require much more power. **Fig 2**'s circuit provides a 5V/200-mA output. Assuming that **Fig 2**'s circuit operates continuously at high power, its quiescent-current level is allowed to be higher than



TRACE	VERTICAL	HORIZONTAL
A	100 mV/DIV	5 mSEC/DIV
B	2V/DIV	5 mSEC/DIV
C	2V/DIV	5 mSEC/DIV
D	2V/DIV	5 mSEC/DIV

Fig 1—Featuring a quiescent current of only 125 μA, *this dc/dc converter* ***(a)*** *generates 5V from a 1.5V cell input. Oscillator IC_{1a}'s output is a 2-kHz square wave (**b,** trace D). A plot of output current versus battery voltage* ***(c)*** *shows that the highest power is available from a fresh cell.*



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	2 mSEC/DIV
B	10V/DIV	2 mSEC/DIV
C	2V/DIV	2 mSEC/DIV
D	1V/DIV	2 mSEC/DIV

Fig 2—Essentially a flyback-type regulator, *this dc/dc converter* ***(a)*** *generates 5V at 200 mA. When power is applied, IC_{1a} oscillates at 5 kHz* ***(b).*** *The circuit's input-output characteristics* ***(c)*** *illustrate that the circuit will start into a full load as long as the battery voltage equals 1.2V. Although the circuit's performance is impressive, its quiescent power requirements at lower currents degrade its efficiency figures* ***(d).***

that of **Fig 1**.

The circuit in **Fig 2** is essentially a flyback-type regulator. Because the LT1070 exhibits low saturation losses and is easy to apply, it's simple to design the flyback regulator to supply the 1W output. Unfortunately, the LT1070 has a 3V min supply-voltage requirement. Bootstrapping from the 5V converter output to the LT1070's supply pin satisfies that requirement. The dual comparator (IC_{1a} and IC_{1b}) and the transistors form a start-up loop.

When power is applied, IC_{1a} oscillates at 5 kHz (see trace A in **Fig 2b**), biasing Q_1 and allowing it to drive the base of Q_2. Q_2's collector (trace B) pumps energy into L_1 and generates step-up voltage-flyback signals. These signals are rectified and stored in the 500-µF capacitor to produce the converter's 5V output.

In many applications, dc/dc converters must accommodate a wide range of input voltages.

IC_{1b} is configured so that its output (trace C) goes low when the converter's output crosses the 4.5V level. When IC_{1b}'s output goes low, IC_{1a}'s integration capacitor pulls low and terminates the circuit's oscillations. Under these conditions, Q_2 can no longer drive L_1. The LT1070 can, however. You can see this behavior (trace D) at the LT1070's V_{SW} pin. When the start-up circuit activates, the V_{IN} pin of the LT1070 has an adequate supply voltage and starts to operate—at the fourth vertical division in **Fig 2b**'s scope photo. There's some overlap between the turn-off of the start-up loop and the LT1070's turn-on, but it has no detrimental effect.

Careful design allows the start-up loop to function over a wide range of loads and battery voltages. Start-up currents exceed 1A, so Q_2's saturation and drive characteristics are particularly important.

Fig 2c plots the circuit's I/O characteristics. Note that the circuit will start for all loads as long as the battery voltage is 1.2V or better. With reduced loads, the circuit will start for battery levels as low as 1V. Once the circuit starts, it can drive full 200-mA loads with battery voltages as low as 1V. **Fig 2d** plots the efficiency of **Fig 2a**'s circuit at two supply-voltage levels for a range of output currents. Although the circuit's performance is impressive, its quiescent power requirements at lower currents degrade its efficiency figures. Fixed junction-saturation losses at the lower supply-voltage levels are responsible for the lower overall efficiency.

Addressing the efficiency question

Efficiency is a prime concern in some converter applications (see **box,** "Design converters for optimum efficiency"). In small portable computers, for example, the converter typically must generate 5V from a 12V

Design converters for optimum efficiency

Squeezing the utmost efficiency out of a converter is a complex, demanding design task. To obtain efficiencies in excess of 80 to 85%, you'll have to use some finesse, some witchcraft, and some plain luck. The interaction of electrical and magnetic terms produces subtle effects that influence a converter's efficiency. It's not possible to establish a detailed, generalized method for obtaining maximum converter efficiency, but it's easy to list some guidelines.

Losses fall into several loose categories: junction, ohmic, drive, switching, and magnetic. Semiconductor junctions produce losses. Diode drops increase with operating current, a fact that can be quite costly in low-output-voltage converters. A 700-mV drop in a 5V-output converter introduces a loss of more than 10%. Schottky devices will cut this loss by almost 50%, but it's still appreciable. Germanium devices, which are rarely used today, cut losses even more, but their switching losses negate their low-drop performance at high speeds. Germanium devices' reverse leakage may be equally oppressive in very-low-power converters.

Synchronously switched rectification **(Fig 3a)** is more complex, but it can sometimes simulate a more efficient diode. When evaluating such a scheme, however, remember to include both ac and dc drive losses in efficiency calculations. DC losses include base or gate current in addition to dc consumption in any driver stage. AC losses might include the effects of gate (or base) capacitance, transition region dissipation, and power lost because of the delay between the application of the drive and the actual switch action.

Transistor saturation losses are also a significant term. Channel and collector-emitter saturation losses become increasingly significant as the operating voltage decreases. The most obvious way to minimize these losses is to select low-saturation components. This scheme will work, in some cases, but remember to include drive losses (which are usually higher for low-saturation devices) in overall loss estimates.

Sometimes, it's difficult to ascertain the actual losses caused by saturation effects and diode drops. Changing duty cycles and time-variant currents complicate matters. However, there's one simple way to make relative-loss judgments: You can measure the rise in device temperature. Unfortunately, this technique is not very effective at low power levels. In some cases, you can determine losses by deliberately adding a known loss to the component in question and then noting any change in efficiency.

Ohmic losses in conductors are

battery input, and it must do so very efficiently. With a 90% efficiency rating, the positive buck converter in **Fig 3a** fills the bill easily.

Transistor Q_1 serves as the pass element. Replacing the catch diode typically used in buck-type converters with a a synchronous rectifier (Q_2) improves the efficiency of **Fig 3a**'s circuit. The input supply is nominally 12V, but it can vary from 9.5 to 14.5V. The NMOS transistors used for Q_1 and Q_2 have a low (0.028Ω) source-to-drain resistance, which minimizes power losses. The inductor's low-loss core material helps squeeze a little more efficiency out of the design. In addition, keeping the current sense-threshold low minimizes the power loss in the current-limiting circuit.

Fig 3b illustrates the operating waveforms. When the V_{SW} pin turns off (trace A), Q_5 drives Q_2. Q_2 turns off (through D_1 and D_2) when V_{SW} is on. To turn on Q_1, you must drive its gate (trace B) above the input-voltage level. C_1, bootstrapped from the drain of Q_2 (trace C), provides this drive. C_1 charges up through D_1 when Q_2 turns on. When Q_2 turns off, Q_3 conducts to provide a path for C_1 to turn Q_1 on. During this period, current flows through Q_1 (trace D), through the inductor (trace E), and into the load.

Q_1 turns off when the V_{SW} pin is off, allowing Q_5 to turn on Q_4 and pull Q_1's gate low through D_3 and the 50Ω resistor. This resistor reduces the noise voltage generated by Q_1's fast switching transitions. Q_1 must be off when Q_2 is conducting (trace F). The efficiency of **Fig 3a**'s circuit will suffer if both transistors are conducting simultaneously. The 220Ω resistors combine with D_2 to minimize any switch-cycle overlap.

Transistors Q_6 through Q_9 provide short-circuit protection. The LT1004, Q_6, and the 9-kΩ resistor generate a 200-μA current that flows through R_1 and develops a 124-mV threshold for the Q_7-Q_8 comparator.

usually significant only at higher current levels. Hidden ohmic losses include socket and connector contact resistance and equivalent series resistance (ESR) in capacitors. ESR generally decreases as the capacitance value increases, and increases as the operating frequency increases.

Don't forget the copper resistance of inductive components. Quite often, you have to evaluate the tradeoffs between an inductor's copper resistance and its magnetic characteristics.

Components make a difference

Drive losses are also important when it comes to efficiency. A MOSFET's gate capacitance draws substantial ac drive current per cycle, which implies that average currents will increase as frequency increases. Bipolar devices have lower capacitance, but dc base-current requirements make them very power hungry.

Large-area devices may appear attractive because of their low saturation, but you must evaluate drive losses carefully. Usually, large-area devices are viable only when the converter will operate consistently at a significant percentage of its rated current.

Efficiency should be a major consideration in any drive-circuit design. Class A drives (resistive pull-up or pull-down drives) are simple and fast, but they're inefficient. For efficient operation, you'll typically need to use active source-sink combinations that have minimal cross-conductance and biasing losses.

Switching losses occur when devices spend significant amounts of time (relative to operating frequency) in their linear region. At higher repetition rates, transition times can become a substantial source of loss. Proper device selection and drive-circuit design can minimize these losses.

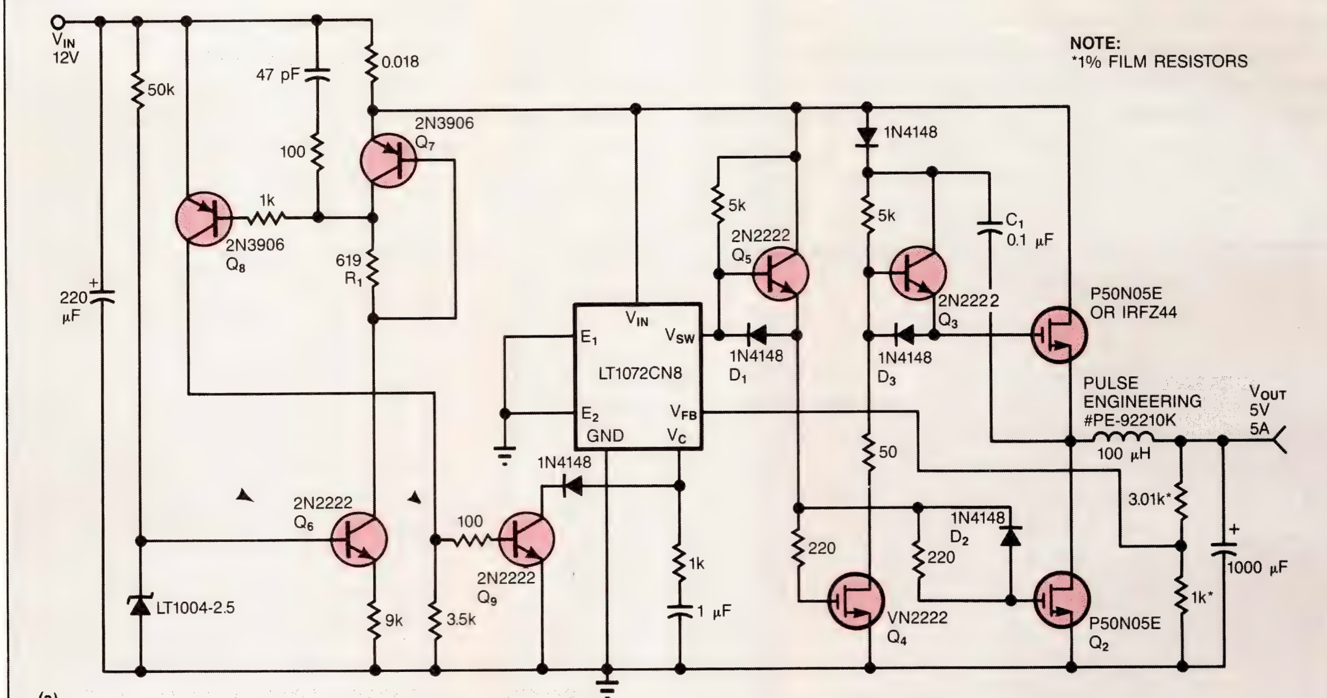
Magnetics design can also influence a converter's efficiency. It's important for you to consider such issues as core-material selection, wire type, winding techniques, size, operating frequency, current levels, and temperature. Practically speaking, access to a skilled magnetics specialist is the only way to ensure a successful design. Fortunately, electrical losses typically outweigh magnetic losses, so you can usually realize fairly high efficiency by using standard magnetic components. If the converter's efficiency is still too low after you've reduced losses to the lowest practical level, you'll need to use custom magnetics.

The buck-boost converter topology is very useful in circuits where the input voltage can be either lower or higher than the output voltage.

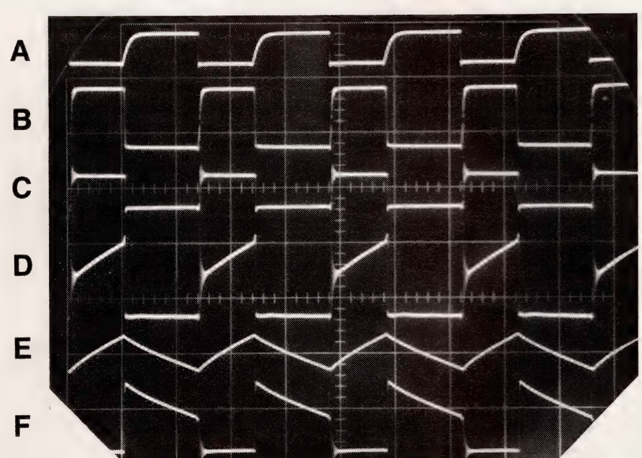
When the voltage drop across the 0.018Ω sense resistor exceeds 124 mV, Q_8 turns on. The LT1072's V_{SW} pin goes off when the V_C pin drops below approximately 0.9V. This drop occurs when Q_8 forces Q_9 to saturate. The RC damper across Q_8 suppresses line transients that might turn on Q_8 prematurely.

Designing for wide input-range capability

Converters must often accommodate a wide range of inputs. Telephone-line voltages, for example, can vary over a considerable range. **Fig 4's** circuit uses an LT1072 to supply a 5V output from a telecomm-type input. The raw telecomm supply is nominally −48V, but it can vary from −40 to −60V. The V_{SW} pin can accommodate this voltage range, but the V_{IN} pin requires some protection, because it has a 60V max rating. Q_1 and the 30V zener diode provide this protection, decreasing the V_{IN} pin's voltage to acceptable levels



(a)



(b)

TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	10 µSEC/DIV
B	20V/DIV	10 µSEC/DIV
C	20V/DIV	10 µSEC/DIV
D	2A/DIV	10 µSEC/DIV
E	2A/DIV	10 µSEC/DIV
F	2A/DIV	10 µSEC/DIV

Fig 3—With a 90% efficiency specification, *this positive-buck-converter design readily satisfies the needs of small portable computers.*

under all line conditions.

In **Fig 4,** the top of the inductor is at ground and the LT1072's ground pin is at the negative supply-voltage rail. The LT1072's feedback pin senses signals with respect to the ground pin, so the 5V output must provide a level shift. Q_2 provides this shift by introducing a low (−2-mV/°C) drift. Such a drift normally presents no problems in a logic supply. In problem cases, the optional network shown will provide appropriate compensation.

The RC damper at the V_C pin provides frequency compensation. The 68V zener diode is designed to clamp and absorb excessive line transients that might otherwise damage the LT1072; the V_{SW} pin has a 75V max rating.

The approach in **Fig 5** has an even wider input range. In this case, the converter produces a −5V output (+5V optional). The coupled inductor will accommodate buck, boost, or buck-boost converter configurations. As the figure shows, this converter will handle an input range of 3.5 to 35V dc.

Fig 5b shows the operating waveforms for the circuit. When the V_{SW} pin is on (trace A), current flows through the transformer's primary winding (trace B). The reverse bias on catch diode D_1 prevents any current transfer to the secondary winding during this period: The energy is stored in the transformer's magnetic field. When V_{SW} turns off, D_1 forward-biases and transfers the energy to the secondary winding. Traces C and D show the voltage on the secondary winding and the current flow through the secondary winding, respectively. Because the transformer is not an ideal device, not all of the primary winding's energy is coupled into the secondary winding. The energy left in the primary winding generates overvoltage spikes on the V_{SW} pin (trace E).

A leakage-inductance term in series with the transformer's primary winding models this phenomenon. When V_{SW} turns off, the transformer current continues to flow, causing the snubber diode to conduct. As the

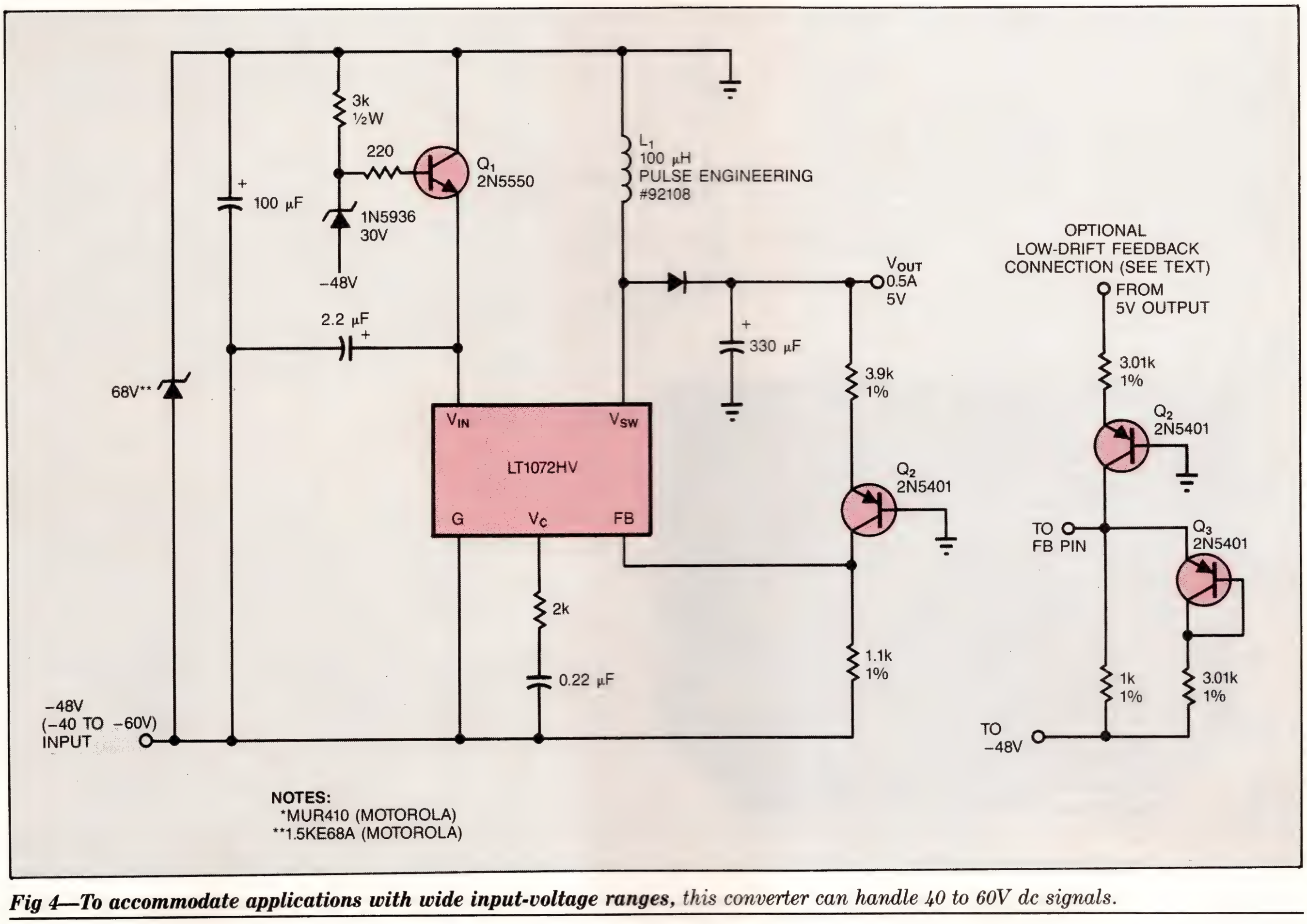


Fig 4—To accommodate applications with wide input-voltage ranges, *this converter can handle 40 to 60V dc signals.*

Linear converters don't encounter the dynamic problems that switching regulators face under varying input and output ranges.

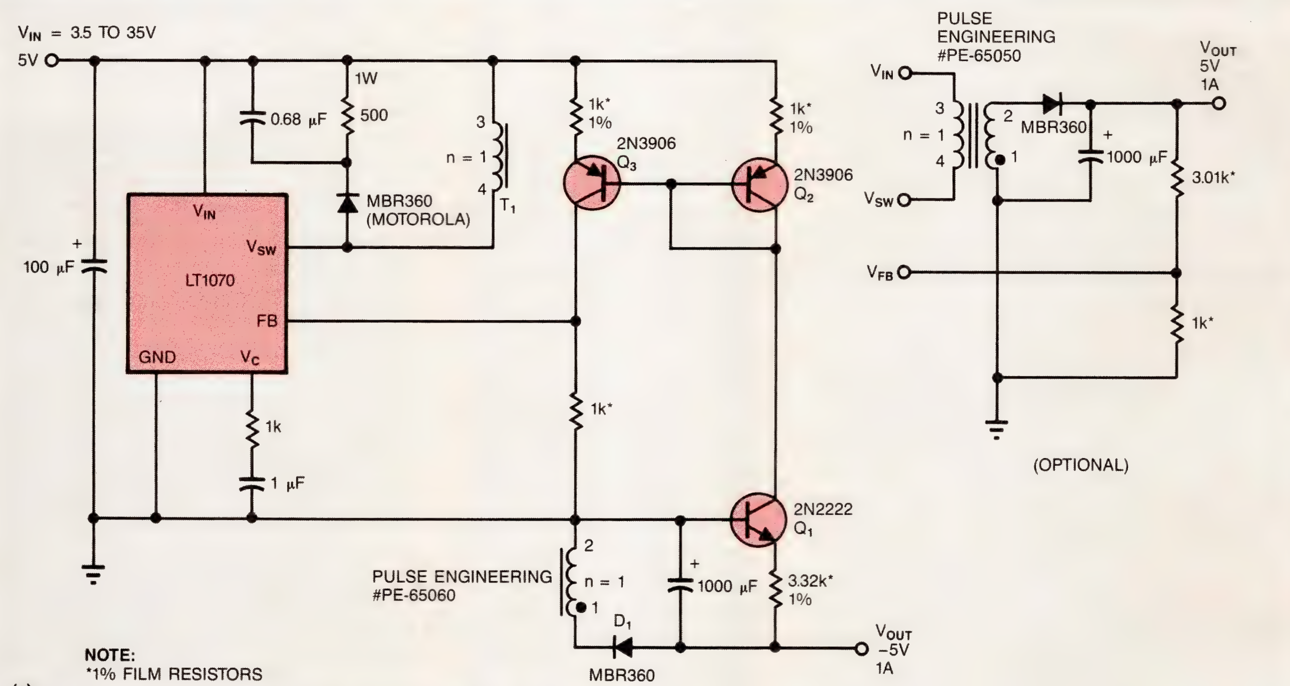
transformer loses its energy, the snubber-diode current falls to zero, clamping the voltage spike. The feedback pin senses with respect to ground, so Q_1 through Q_3 use the $-5V$ output to provide a level shift.

The buck-boost solution for wide input range

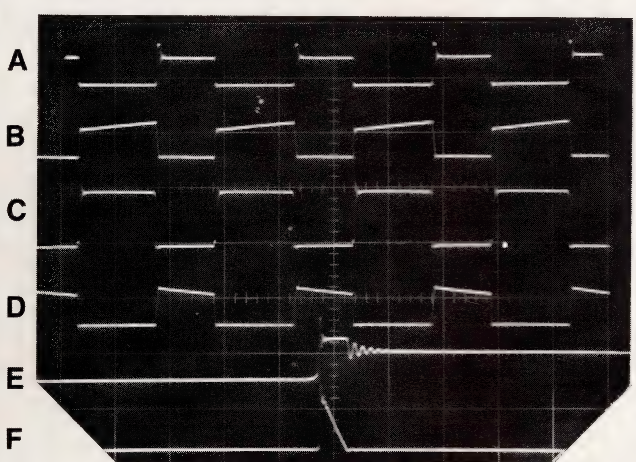
The buck-boost topology is useful in circuits whose input voltage can be either lower or higher than the output voltage. The design in **Fig 6** uses a single inductor in place of the transformer that you'd typically use in such designs. The circuit's operation somewhat mirrors that of **Fig 5**'s converter.

The pass-transistor gate-drive scheme is identical in both cases, except that in **Fig 6** the gate-source voltage is clamped so that it won't exceed the device's $\pm 20V$ rating. **Fig 6b** shows the operating waveforms.

When V_{SW} is on (trace A), pass transistor Q_1 saturates. The gate voltage (trace B) is clamped by the



(a)



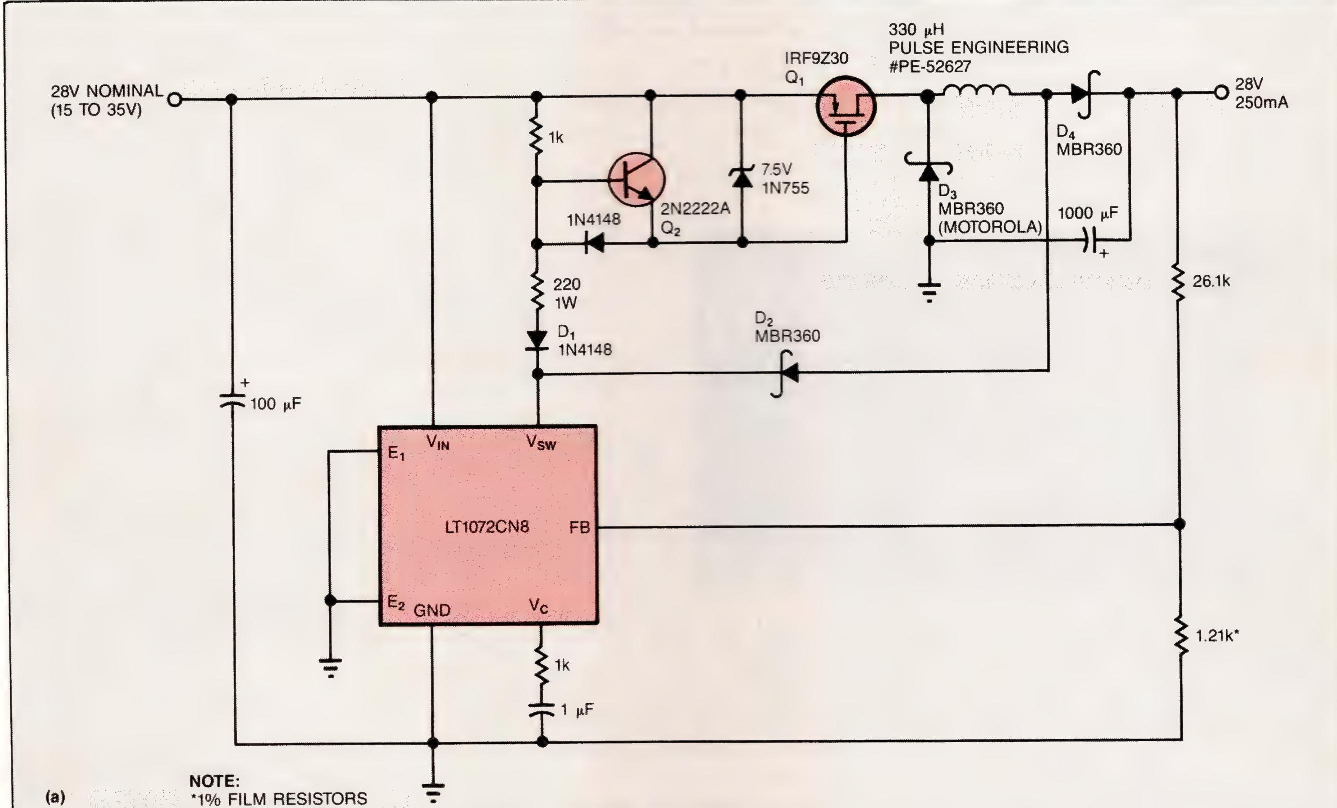
(b)

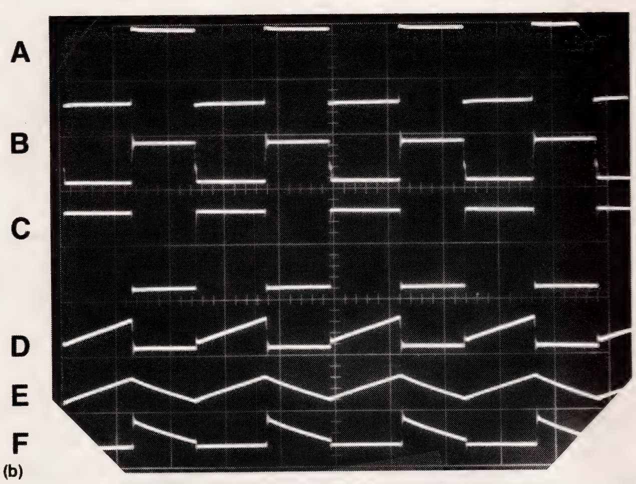
TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	10 µSEC/DIV
B	4A/DIV	10 µSEC/DIV
C	10V/DIV	10 µSEC/DIV
D	4A/DIV	10 µSEC/DIV
E	20V/DIV	1 µSEC/DIV
F	2A/DIV	1 µSEC/DIV

Fig 5—Able to handle inputs ranging from 3.5 to 35V dc, *this circuit's coupled-inductor design will accommodate buck, boost, or buck-boost converter configurations.*

zener diode. Traces C and D show the voltage on Q_1's drain and the current through Q_1, respectively. The similarities between the two circuits end here.

In **Fig 6**'s circuit, the inductor is within one diode drop (D_2) above ground, instead of being tied to the output, as it is in **Fig 5**. As a result, the voltage drop across the inductor—except for Q_1's V_{BE} drop and saturation losses—is now equal to the input voltage. D_1 is reverse-biased, and it prevents the output capacitor from discharging into the V_{SW} pin. When the V_{SW} pin is off, Q_1 and D_2 cease to conduct. Because the current in the inductor (trace E) continues to flow, D_3 and D_4 forward-bias, allowing the inductor energy to transfer into the load. Trace F illustrates the current





TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	10 µSEC/DIV
B	10V/DIV	10 µSEC/DIV
C	20V/DIV	10 µSEC/DIV
D	2A/DIV	10 µSEC/DIV
E	2A/DIV	10 µSEC/DIV
F	2A/DIV	10 µSEC/DIV

***Fig 6—The buck-boost topology is useful** in circuits where the input voltage can be either lower or higher than the output voltage.*

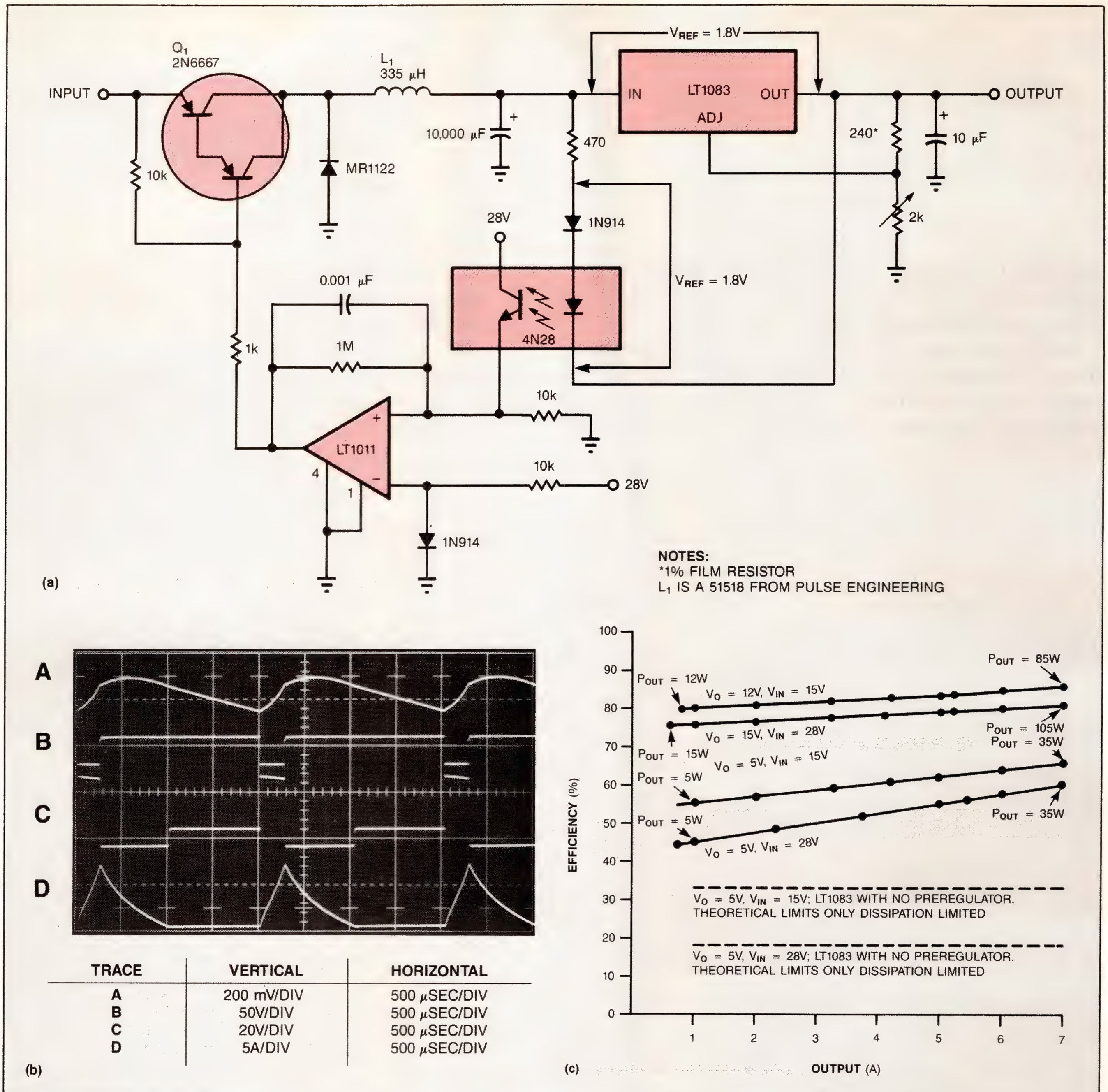


Fig 7—Although typical linear converters have efficiency and temperature-rise problems, *this design efficiently controls high power under widely varying input and output conditions.*

flow through D_3. D_2 prevents Q_1 from staying on when the circuit is operating in buck mode. D_1, on the other hand, blocks current flow into the gate-drive circuit when the converter is operating in boost mode.

A look at a linear-type solution

In a sense, linear regulators are extremely wide-range dc/dc converters. They don't encounter the dynamic problems that switching regulators face under varying input and output ranges. Linear regulators simply dissipate excess energy as heat. This elegantly simple energy-management mechanism creates a significant amount of inefficiency and temperature rise. **Fig 7** illustrates a design that allows a linear regulator to control high power efficiently under widely varying input and output conditions.

The regulator resides within a switched-mode loop that servocontrols the voltage *across* the regulator. In this arrangement, the regulator functions normally, while the loop maintains the voltage across the regulator at a minimal value regardless of line-, load- or output-setting changes. Although this approach can't match the efficiency of a classical switching regulator, it maintains the low noise and fast transient response inherent in the linear regulator.

The LT1083 functions conventionally, supplying a regulated, 7.5A output. The remaining components form the switched-mode, dissipation-limiting control loop. This loop forces the potential across the LT1083 to equal the 1.8V value of V_{REF}. The optoisolator pro-

CIRCLE NO 210

Large-area devices may appear attractive because of their low saturation, but you must evaluate drive losses carefully.

vides a convenient way to look at the differentially sensed voltage across the LT1083 as though it were a single-ended input. When the regulator input (trace A in **Fig 7b**) decays far enough, the LT1011 output (trace B) switches low and turns Q_1 on (trace C), allowing current to flow from the circuit input (trace D) into the 10,000-μF capacitor and raise the regulator's input voltage.

When the regulator input rises high enough, the comparator goes high, turning off Q_1; the capacitor stops charging. The MR1122 damps the current-limiting inductor's flyback spike. The 0.001-μF/1-MΩ combination sets the loop hysteresis at about 100 mV p-p. This free-running, oscillation-control mode substantially reduces dissipation in the regulator without degrading its performance. Despite changes in the input voltage, regulated outputs, or load shifts, the loop always ensures minimum dissipation in the regulator.

Fig 7c plots the efficiency of the circuit in **Fig 7a** at various operating points. Thanks to the loop's performance, the circuit losses are relatively small at high output-voltage levels, and the circuit's efficiency is quite good. Its efficiency suffers at low output-voltage levels, but compares very favorably with the theoretical data for an LT1083 operating with no preregulator. At the higher theoretical dissipation levels, the LT1083 will shut down, precluding practical operation.

Meeting applications' high voltage needs

Fig 8's design features a fully floating output. This provision allows you to reference the output away from system ground, a technique that's often desirable for applications in which you want to limit noise or provide biasing. In this converter, galvanically isolated equivalents replace the LT1072's internal error amplifier and reference. Power for the replacement parts is bootstrapped from the output via source-follower Q_1 and its 2.2-MΩ ballast resistor. IC_1 and the LT1004 (both

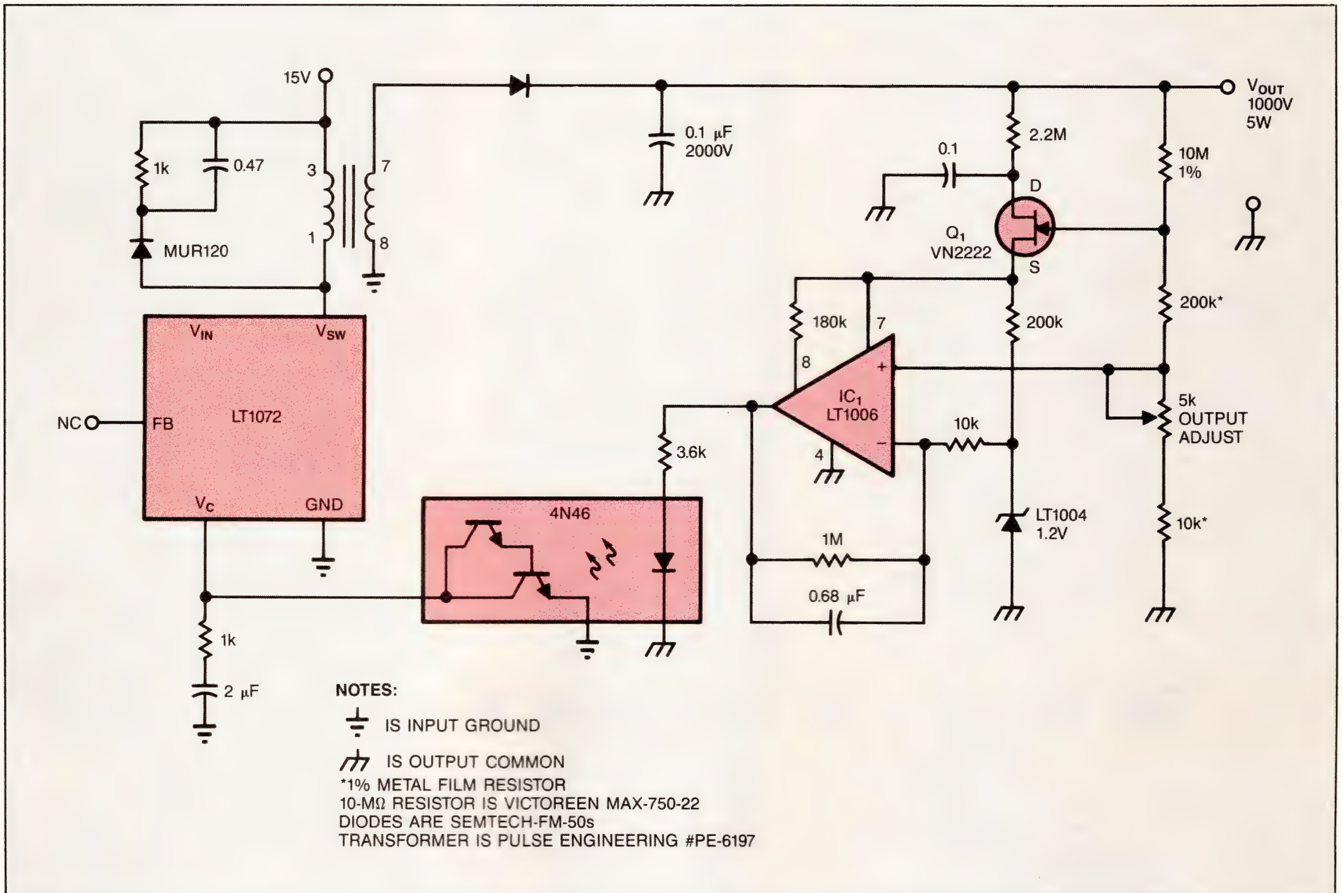


Fig 8—With a fully floating output, *this converter configuration allows you to reference the output away from system ground, a technique that's often desirable for applications in which you want to limit noise or provide biasing.*

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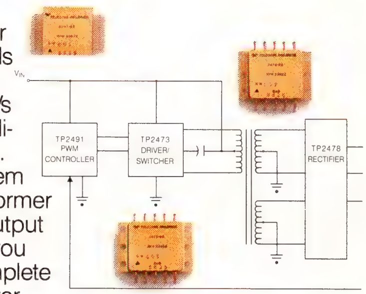

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Squeezing the utmost efficiency out of a converter requires some finesse, some witchcraft, and some luck.

are micropower components) minimize dissipation in the Q_1/ballast-resistor combination.

Q_1's gate bias, tapped from the output divider string, produces about 15V at its source. IC_1 compares the scaled divider output with the LT1004 reference. The error signal (IC_1's output) drives the optocoupler, which operates at low levels, saving power. The optocoupler's output pulls down on the V_C pin to close the loop. Frequency compensation at the V_C pin and IC_1 stabilizes the loop.

Transformer and optocoupler restrictions impose limitations on the common-mode breakdown performance in **Fig 8**'s converter. Isolation amplifiers, certain transducer measurements, and ESD-sensitive applications require high breakdown capability. In addition, very precise floating measurements such as signal conditioning for high-impedance bridges can require extremely low leakeage to ground.

You need to take a different design approach to achieve high common-mode voltage capability with minimal leakage. Some feel that a magnetic approach is the only viable way to achieve the isolated transfer of appreciable amounts of electrical energy. That idea is simply not correct: You can employ ceramics to solve the high-energy/low-leakage problem. In fact, the high voltage breakdown and low electrical conductance associated with ceramics surpasses the isolation characteristics of magnetic approaches. In addition, the acoustic transformer is a simple device.

You can form the transformer by bonding a pair of leads to each end of the ceramic material. In such a simple structure, the insulation resistance can exceed $10^{12}\Omega$, and primary-secondary capacitances can measure in the 1- to 2-pF range. The resonant frequency is a function of the material and its characteristics. You can think of the device as a high-Q resonator

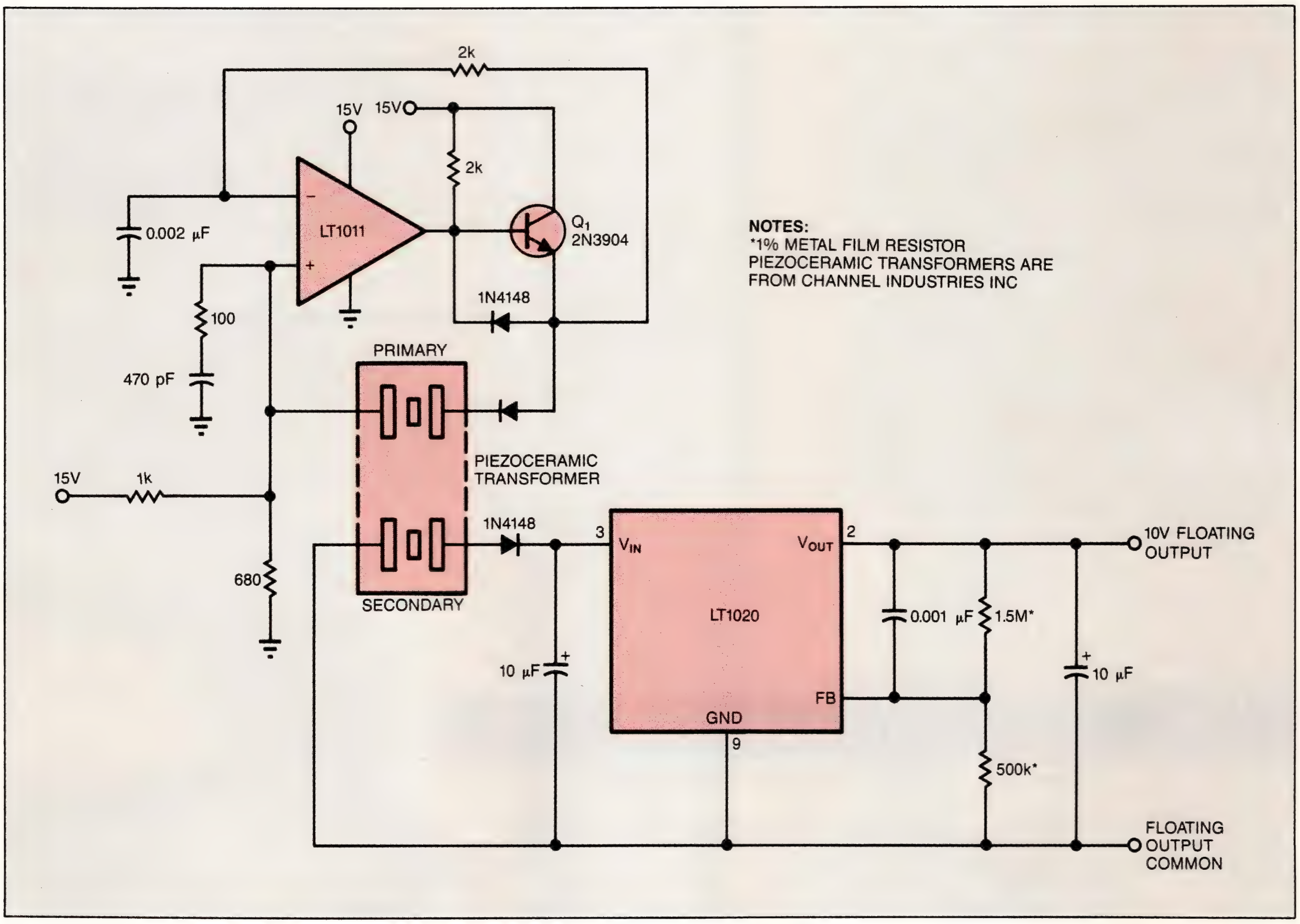
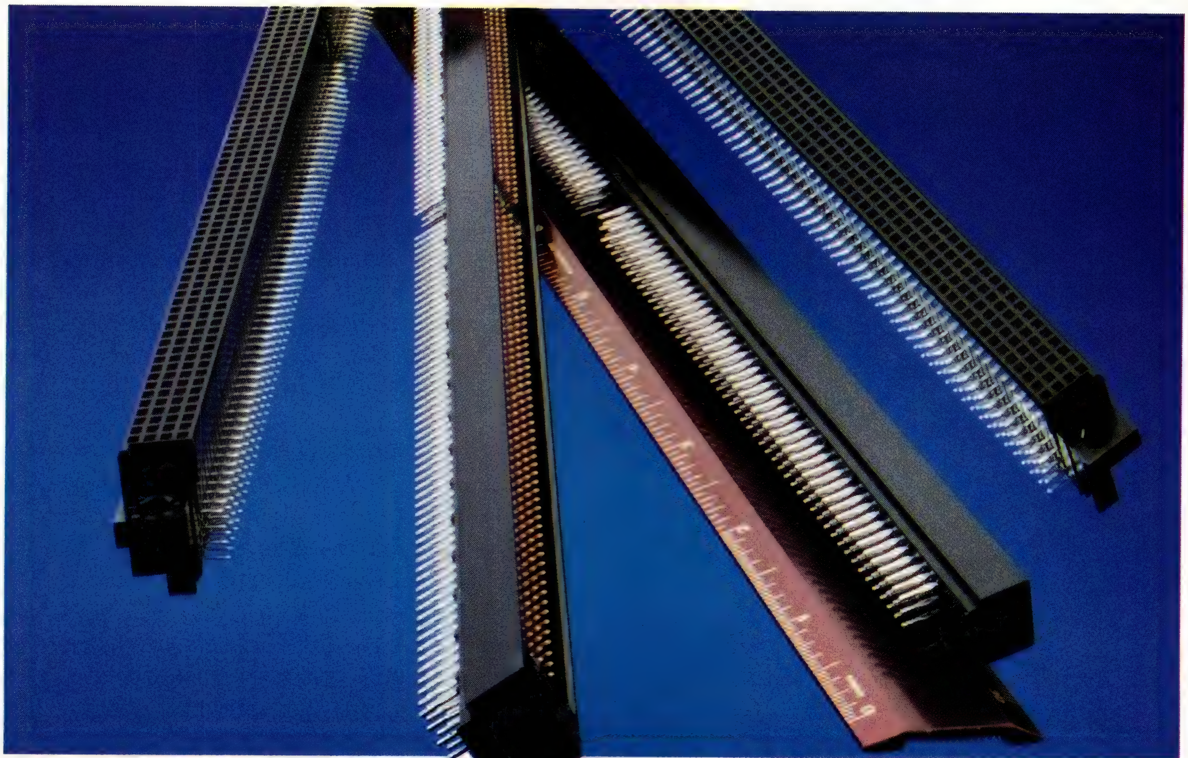


***Fig 9—A ceramic-based design approach** proves to be a viable way to achieve the isolated transfer of appreciable amounts of electrical energy.*



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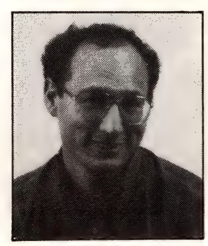
similar to a quartz crystal. You must design drive circuitry to excite the device in the positive-feedback path of a wideband gain element.

In this design, unlike a design using a crystal, you must configure the drive circuitry so that a substantial amount of current passes through the ceramic, and you must maximize power in the transformer. In **Fig 9**, the piezoceramic transformer is in the LT1011 comparator's positive feedback loop. Q_1 serves as an active pull-up for the open-collector LT1011 device. The 2-kΩ/0.002-μF path biases the LT1011's inverting input.

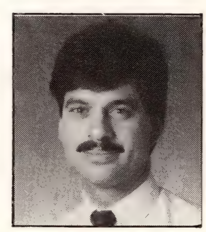
Positive feedback occurs at the transformer's resonance frequency, and oscillation commences. The transformer, like a quartz crystal, has significant harmonic and overtone modes. The 100Ω/470-pF damper circuit suppresses spurious oscillations and mode hopping. The transformer appears as a highly resonant filter to the resultant wave that it propagates internally. The transformer's secondary voltage is sinusoidal.

The transformer also provides some voltage gain. The diode and the 10-μF capacitor convert the secondary voltage to dc. The LT1020 low-quiescent-current regulator provides a stabilized 10V output. This converter has an output-current capability of only a few milliamps, but you can improve this performance by devoting more attention to transformer design. EDN

Authors' biographies



Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.



Brian Huffman is an applications engineer at Linear Technology Corp. A member of the IEEE, he holds a BSET degree from Indiana State University and an MSEE from Santa Clara University. In his spare time, Brian enjoys plays, concerts, and the beach, and he likes to travel.

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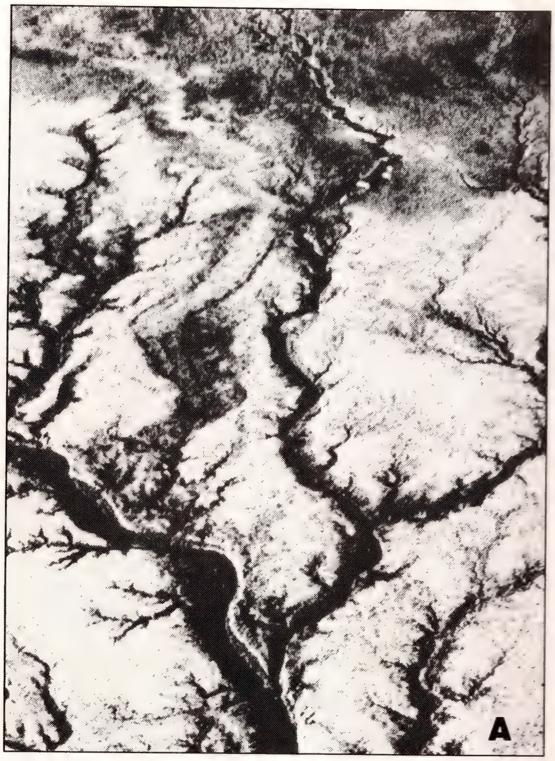

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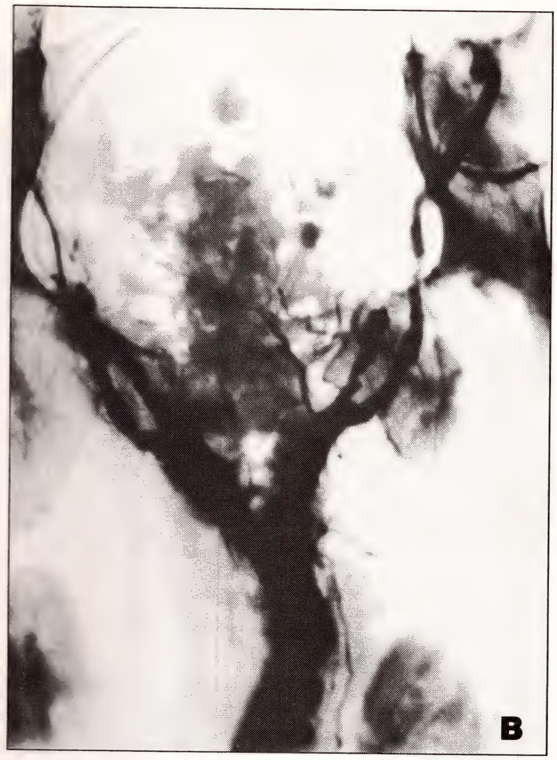

B

Delta or Aorta? Which is Which?

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A. Satellite view of river delta. **B.** Arterial angiogram.

Note: These began as continuous tone images which were processed in black and grey by a TDU-850. The TDU-850 images, however, had to be converted to conventional halftones in order to be shown in this magazine. Thus the high quality of the original TDU-850 images have been obscured. For true results ask to see a demonstration.

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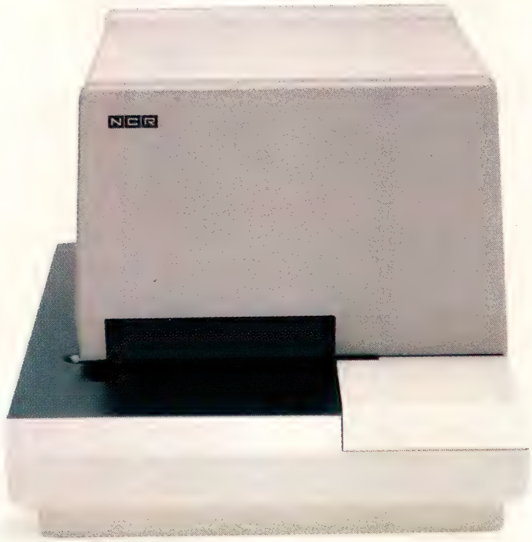

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Creating value

The registered PROM can replace PALs in large state machines

If you're wrestling with a sequential logic design, the RPROM might help you overcome the product-term restrictions of PALs. An RPROM compiler available from the author can simplify incorporating these devices into your designs by translating your machine code into a bit map for programming the PROM.

Christopher Mercer, *Nixdorf Computer*

Designers tend to neglect the registered PROM (RPROM) when constructing sequential digital systems. Instead, they turn to PALs and the newer microsequencer-based devices (**Refs 1** and **2**), both of which were designed with these types of systems in mind. But in some sequential design systems, such as bit-rate adapters, the RPROM is the chip of choice. In these and other applications, logic designers should give RPROMs a chance.

The RPROM's main advantage over the PAL is its capability to implement a large pool of product terms. A PAL typically has 10 product terms for each programmable-array output. But you can create 2^A logic combinations with an RPROM with "A" address lines, and these logic combinations can simulate significantly more than 10 product terms per PROM output. The PAL is perfect for implementing state machines with as many as 20 states, but you'll have to do some logic juggling to create machines with more than 20 states. An RPROM can readily implement state machines with hundreds of states.

Different means for different machines

Fig 1 shows the internal architectures of three devices for designing sequential machines. The first, Altera's EP310 (**Fig 1a**), is an erasable version of the industry-standard 16R8 PAL. The EP310 has nine product terms for each output of the programmable array, plus feedback loops from each of the eight output macrocells. In addition to four output macrocells and four output registers, AMD's 23S8 PAL contains six buried registers, letting you implement machine states without using up valuable output pins (**Fig 1b**). The 23S8 has six to 12 product terms for each array output and is well suited for implementing multiple small state machines synchronized to the same clock. Both PALs are 20-pin devices.

The 2735 1k×8-bit RPROM comes in a 24-pin package (**Fig 1c**). The device has eight outputs and 13 useful inputs: 10 address lines, a word initiate line that can be used to reset the RPROM to a preprogrammed state, a clock line, and either a synchronous or an asynchronous output enable line. Although the RPROM is less flexible than either of the PALs for

The RPROM's main advantage over the PAL is its capability to implement a large pool of product terms.

decoding logic equations and implementing a variety of small state machines, its 1k-byte memory space is capable of storing a huge pool of logic combinations for realizing large state machines.

Currently, the byte densities for commercially available RPROMs range from 512 to 8k bytes; however, the number of available outputs, eight, places a restriction on the number of state variables. For example, each state variable in the synchronous Moore machine requires a feedback loop from one of the outputs to one of the input address lines (**Ref 1** and **2**). An RPROM with six state variables can provide only two output lines. Since the RPROM described above has 10 address lines, it can store all 16 combinations of the remaining four address lines. Therefore, the RPROM can use any of the state variables with any of the 2^4 input combinations. This capacity would be doubled with a 16-output RPROM; but, unfortunately, they are not commercially available.

To get around the eight-output restriction, you could construct a discrete 16-output RPROM by using a 16-bit PROM and some external registers. In selecting these devices, you must make sure that they meet your application's speed requirements (see **box,** "Calculating the speed of an RPROM"). You could also expand the number of outputs by operating two RPROMs in parallel. But, because the two devices must communicate with each other, this procedure will not double the number of available outputs.

To efficiently design state machines using RPROMs,

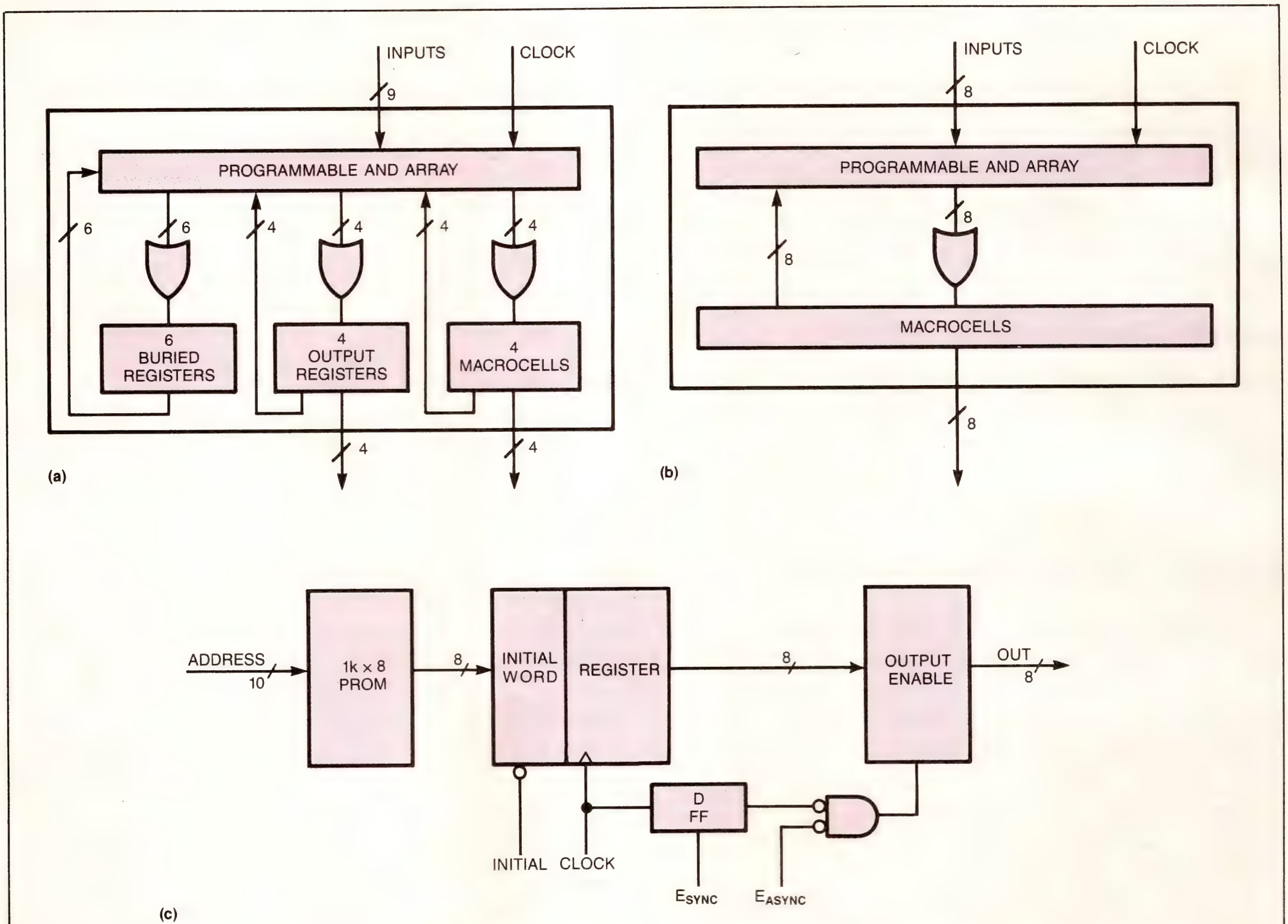


Fig 1—Three state machine devices have different internal architectures. *Altera's EP310 has eight output macrocells with nine product terms for each array output **(a)**. AMD's 23S8 PAL contains four output macrocells, four output registers, and six buried registers; there are six to 12 product terms for each array output **(b)**. The 1k×8-bit storage space of the 2735 RPROM can create a huge pool of product terms **(c)**.*

you need an RPROM compiler that translates your machine code into a bit map for programming the PROM. You can obtain one from the author for a small fee to cover the media, postage, and handling. The RPROM compiler is written in C on an IBM-formatted disk and compiled with Microsoft's C compiler (version 5) on an IBM PC/AT-compatible computer. The source code is portable, but portability is not guaranteed.

You must input three types of parameters when using the RPROM compiler:

- The definitions for the input and output pins
- The next-state definitions, which go into a switch statement
- The output-state definitions, which also go into a switch statement.

The program is best described as a block that contains all of the state machine definitions. This block generates all of the possible address combinations for producing a bit map for the PROM. The small main module uses the following special functions:

- stategen(), which generates the transition table for the next state
- outputgen(), which generates the state-machine outputs
- dectobin(), a decimal-to-binary converter used by the stategen() and outputgen() functions
- hextobin(), a hexadecimal-to-binary converter used by the stategen() and outputgen() functions
- jedhed(), which generates the JEDEC file header.

The main variables in the program are statar(6), which contains the current state variable; OUTPUT(DATWIDTH), which contains the current output; and binum(ADDWIDTH), which represents the address inputs to the RPROM. The program produces a JEDEC file in ASCII binary-code 3 format suitable for

Calculating the speed of an RPROM

The response times of the RPROM and any surrounding circuitry affect the clocking speed of a sequential circuit. When choosing an RPROM for a state machine design, you should consider the factors that limit its clocking speed: the minimum address-set-up time and the maximum clock-to-output delay time. AMD's AM27S35A-C is one of the fastest RPROMs around and specifies a minimum address time of 35 nsec and a maximum clock-to-output delay of 20 nsec.

The circuit configuration is also a factor in speed calculations. How you use the RPROM affects how you calculate the maximum operating speed. If you use the AM27S35A-C in a feedback arrangement, such as in the example presented here, you can determine the minimum clock period by adding the minimum address time and the maximum clock-to-output delay time. Thus, the minimum clock period is 55 nsec, corresponding to a maximum operating speed of 18 MHz.

Sometimes peripheral logic circuitry imposes additional constraints on the minimum clock period. **Fig A** illustrates a conditional feedback loop that depends on the input data to an external logic gate. In this case, the maximum gate delay must be added to the two RPROM speed-setting parameters to obtain the minimum clock period. Assuming a maximum gate delay of 15 nsec for the input logic gate, the minimum clock period increases to 70 nsec, corresponding to a maximum operating speed of 14 MHz.

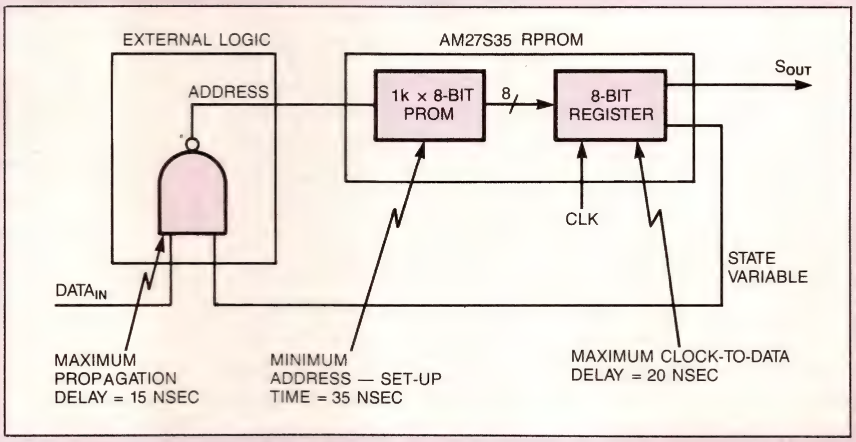


***Fig A—The propagation delay of any external logic circuitry** must be added to the minimum address-set-up time and the maximum clock-to-output delay in order to determine the minimum clock period that can operate the circuit.*

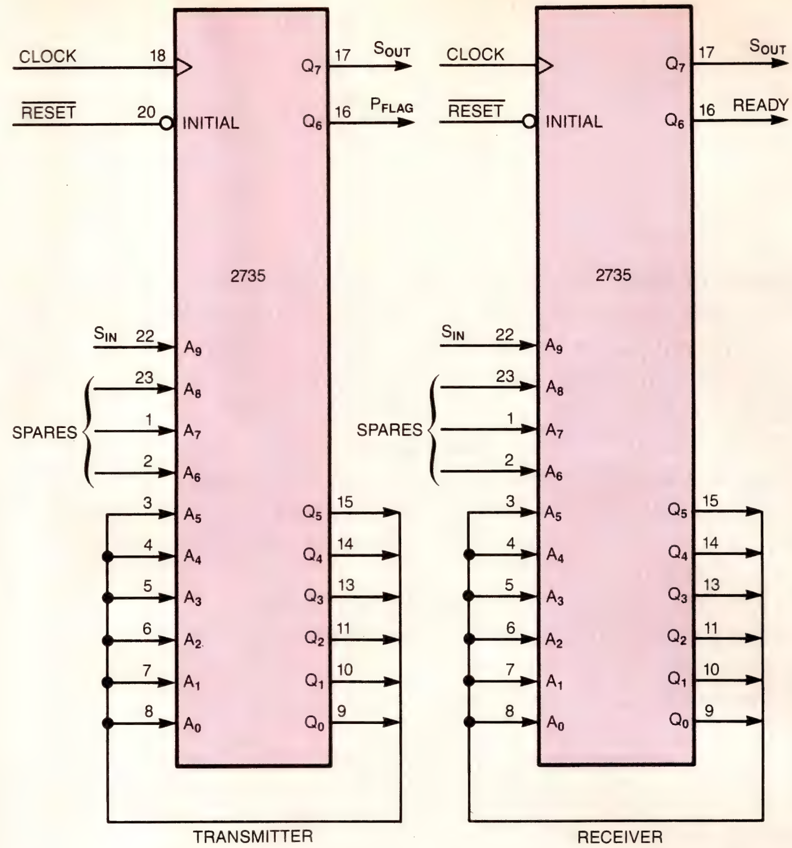


Fig 2—You can implement a transmitter and a receiver that adapt the bit rate *of a data stream by using two 2735 RPROMs. Spare inputs can be used as speed-select lines.*

downloading to the IODATA PROM programmer. Other formats are possible by using jedhed().

To illustrate the use of RPROMs in a state machine, consider the example of a bit-rate adapter that alters the speed of a serial bit pattern from 9.6k to 64k bps for data transmission. The transmitter sends a 40-bit frame containing the 9.6k-bps data and frame synchronization bits. The receiver included in the design reconstructs the original 9.6k-bps data from the 64k-bps bit stream. The receiver must search the transmitted data for the synchronization characters in order to lock onto the frame and decode the original data.

You can implement the transmitter and receiver for the bit-rate adapter by using a 1k×8-bit RPROM for each function **(Fig 2)**. In the bit-rate adaptation scheme, a 40-bit frame is organized into five bytes **(Fig 3)**, and a 64-kHz clock sequentially transmits each bit in the pattern, beginning with bit 0. The bits labelled "D" in the data pattern represent 9.6k-bps data. If you allocate the first two bits of each byte as data slots, the transmitter adapts the bit rate from 16k to 64k bps. But, by filling only three of every five available data slots with data, the transmitter adapts the bit-stream rate from 9.6k to 64k bps. The scheme also works with a 128k-bps clock that is gated with an 8-kHz signal. Using this clock arrangement, the transmitter adapts the data to the synchronous B channel inputs for basic access to ISDN.

The state machine diagram for the transmitter is a loop with 40 states **(Fig 4)**. The transmitter assembles the 40-bit frame by inserting the synchronization bits and the data bits into the appropriate slots. The synchronization bit pattern must, of course, be unique; it is inserted in states S_{34} through S_{39}. When the loop

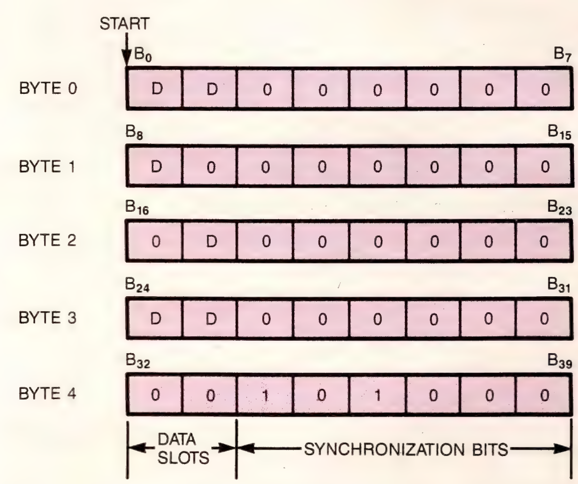


Fig 3—The 9.6k- to 64k-bps bit-rate adapter uses a 40-bit frame *organized into five bytes. The first two bits of each byte are available for data. The scheme adapts the bit rate by inserting data into three of every five available data slots. Six bits are used for frame synchronization.*

To efficiently design state machines using RPROMs, you need an RPROM compiler that translates your machine code into a bit map for programming the PROM.

repeats, or when an external reset occurs, the machine jumps to state S_0. **Listing 1** shows a program listing of the transmitter state machine using the RPROM compiler.

The receiver design is slightly more complex. First, states S_0 through S_5 of the receiver state machine search the incoming bit pattern to locate the synchronization bits **(Fig 5)**. Once the state machine establishes the synchronization pattern, subsequent states that place the Ready line high decode the data bits. States S_{32} through S_{45} check the synchronization bits on each received frame to verify that the receiver is locked on the frame. Since the state machine must first locate the synchronization bits, the received frame begins with these bits and must default to state S_6 at the end of each frame.

You can enhance the design by transmitting additional data in the spare slots of the 64k-bps data stream

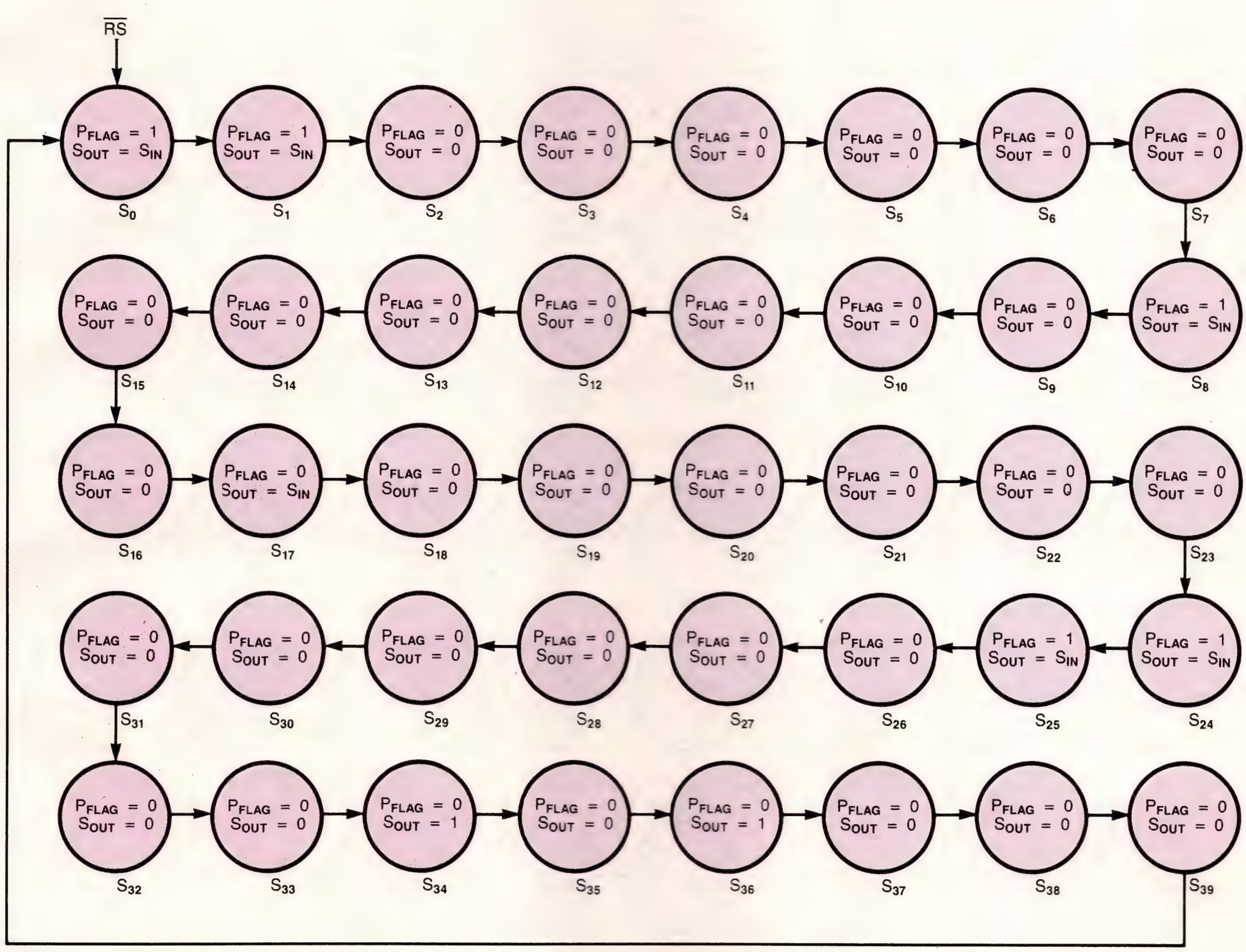


***Fig 4—The transmitter's 40-state state diagram** sets the P_{FLAG} line high for each state that contains data. It inserts the synchronization bits in states S_{34} through S_{39} and all states have a reset to S_0.*

outputs of commercially available
Ms place a restriction on the num-
f state variables.

as long as the data do not clash with the synchronization pattern. For example, you could use the three spare inputs on the transmitter section to provide the receiver with automatic speed detection. The three spare inputs could transmit data at an additional eight speeds. A problem arises at the receiver end, however, since there aren't any spare outputs for relaying this information to a peripheral device, such as a UART.

This problem could be solved by running two RPROMs in parallel at the receiver end to create the

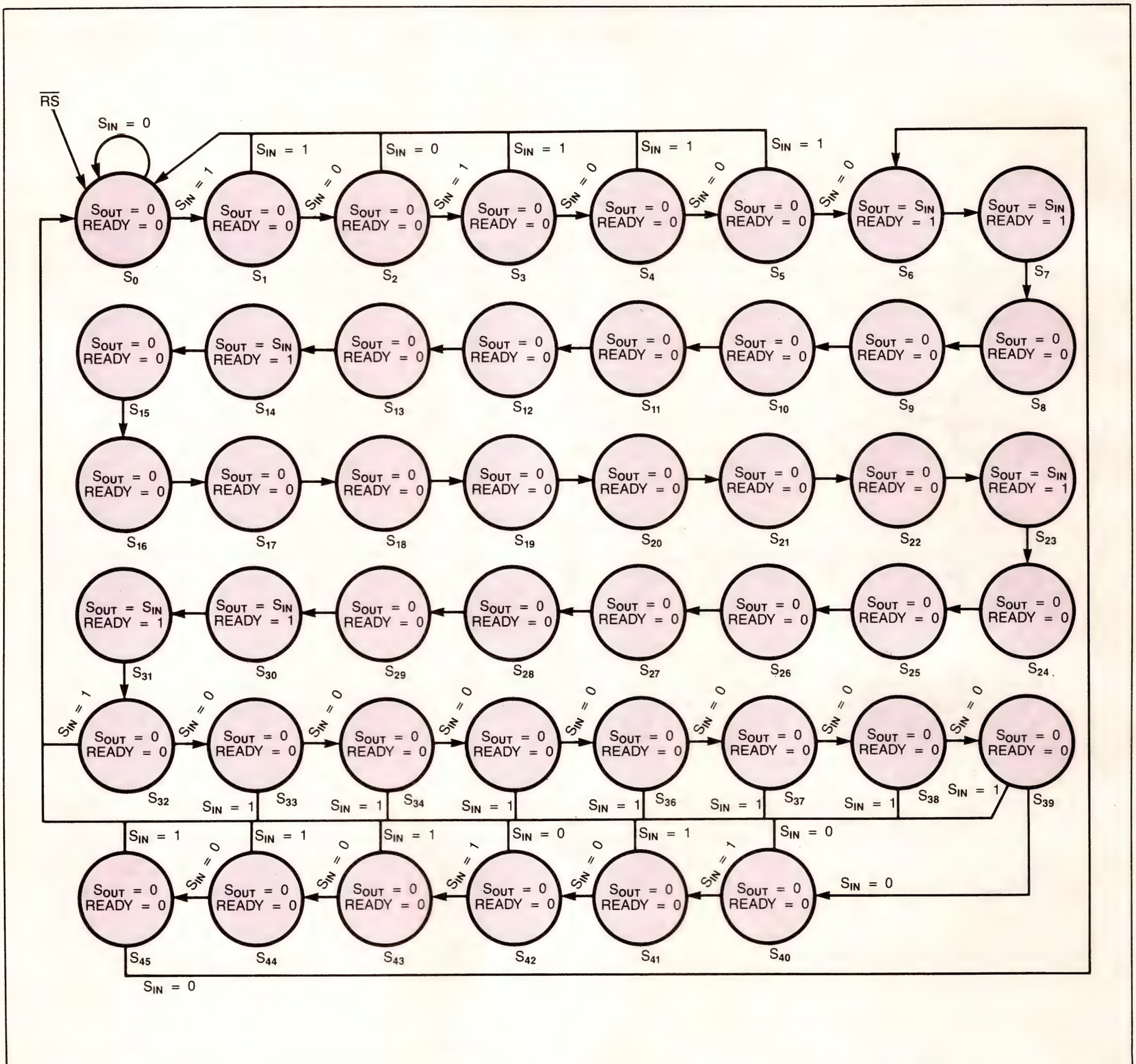


Fig 5—In the receiver's 46-state state diagram, *states S_0 through S_5 locate the frame synchronization bits. The subsequent states set the Ready line high wherever data bits are present. The synchronization bits for each frame are checked by states S_{40} through S_{45}. S_{45} loops back to state S_6 if the frame synchronization bits are detected. All states return to state S_0 upon a reset signal.*

An RPROM in combination with a PAL can create a potent machine.

additional outputs. A more powerful method for solving the problem is adding extra states to the receiver state machine that operate on the additional information. You can then attach a PAL to the state variable lines to decode the information for use by a peripheral. Combining these two devices, an RPROM and a PAL, can create a potent machine. EDN

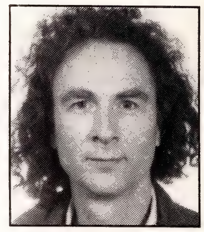
References

1. Kopec, Stanley, "State machines solve control-sequence problems," *EDN*, May 26, 1988, pg 177.
2. Kopec, Stanley, "Asynchronous state machines challenge digital designers," *EDN*, June 9, 1988, pg 179.
3. Fletcher, William I, *An Engineering Approach to Digital Design*, Prentice-Hall, New York, NY 1980.
4. AMD, *Programmable logic handbook/data book*, 1986/1987.

Mailing address

For a copy of the RPROM compiler, please mail your requests to: Christopher Mercer, Heese Strasse 9A, 1000 Berlin 41, West Germany. Mailbox: Telecom Gold/Microlink-72:MAG90392.

Author's biography



Christopher Mercer designs ISDN terminal adapters for Nixdorf Computer in Berlin. Previously he worked for British Telecom as a system designer on the system-X SPC exchange and as a reseacher with the Polytechnic of Central London. He received a BSC degree with honors in Electrical & Electronic Engineering and a BSC in Power Engineering from the Polytechnic of Central London in 1980. In his spare time he enjoys squash, badminton, rock climbing, and music.

Article Interest Quotient (Circle One)
High 488 Medium 489 Low 490

LISTING 1

```
RATE ADAPTION TRANSMITTER STATE MACHINE.

/*general definitions*/
#define datfil test4.jed
#define TRUE 1
#define FALSE 0
#define ADDWIDTH 16
#define ADDSIZE 20
#define DATWIDTH 8
/*State machine variables*/
/*inputs*/
#define SIN  *(pfbinum)
#define BBB*(pfbinum+1)
#define CCC*(pfbinum+2)
#define PS0 *(pfbinum+3)/*present states*/
#define PS1 *(pfbinum+4)
#define PS2 *(pfbinum+5)
#define PS3 *(pfbinum+6)
#define PS4 *(pfbinum+7)
#define PS5 *(pfbinum+8)
/*outputs*/
#define PFLAG *(poutput+0)
#define SOUT *(poutput+1)
#define NS0 *(poutput+2)/*next states*/
#define NS1 *(poutput+3)
#define NS2 *(poutput+4)
#define NS3 *(poutput+5)
#define NS4 *(poutput+6)
#define NS5 *(poutput+7)
/*external declarations*/
/*messages for the jedec file see IODATA book*/
char *msg1="CHM BERLIN 31:05:88";
char *msg2="AM27S35 Registered prom     ";
char *msg3="Design=RA_TX: prom5.c      *";
char *msg4="QP24*                      ";
char *msg5="QF8192*                    ";
char *msg6="0000";/*this disables the DATAIO checksum*/
```

Listing continued on page 238

LISTING 1 *(Continued)*

```
char *msg7="L0000";
int statar[6];
int OUTPUT[DATWIDTH];
int dind;
double NEXTSTATE;


MAIN()
          {
          int INPUT[11],*PINPUT,*poutput,binum[ADDWIDTH];
          int BADDRESS,index,p=0
          int *pstatar;
          long int ADDRESS;
          int *pbinum;
          double stat;
          FILE *fp_1;
          fp_1=fopen("prom5.jed","w");

                    pbinum=binum;
                    pstatar=statar;
                    PINPUT=INPUT;
                    poutput=OUTPUT;
                    dind=0;

          for (index=0;index<6;index++)
                    statar[index]=0;
          for (index=0;index<ADDWIDTH;index++)
                    binum[index]=0;
          for (index=0;index<8;index++)
                    OUTPUT[index]=0;

                    putc('\x02',fp_1);/*STX*/

                    for (ADDRESS=0x000;ADDRESS<0x400;ADDRESS++)

          for (index=0;index<6;index++)
                    statar[index]=0;
          for (index=0;index<ADDWIDTH;index++)
                    binum[index]=0;
          for (index=;index<8;index++)
                    OUTPUT[index]=0;

                              hextobin(ADDRESS,binum) ;/*convert ADDRESS from hex nu

                              stategen(binum) ;/*generates next state table*/
                              outputgen(binum) ;/*generates output table*/

                              putc('B',fp_1) ;
                              p++;
                              for (index=0;index<8;index++)
                              fprintf(fp_1,"%d",*(poutput+index));
                              fprintf(fp_1,"F ");
                              if (p==4)
                                        {
                                        p=0;
                                        putc('\r',fp_1) ;
                                        putc('\n',fp_1) ;
                                        }
                              }/*for*/
          putc('\x03',fp_1) ;/*ETX*/
          fcloseall();

          }/*main*/

dectobin(m)
/*inputs the decimal number m, then converts it to binary.
  The pointer to the binary string is passed to the
  function by the caller.
*/

double m;
          {
          extern statar[],dind;
          double n;
          int *pstatar;
          int testc,zz,index;
          double z,d;
          unsigned int yy,y;

                    pstatar=statar;
          for (index=0;index<6;index++)
                    statar[index]=0;
                    for(index=0;index<6;index++)
                              {
```

LISTING 1 *(Continued)*

```
                        if (m==0) break;
                        z=(m/2.0) ;
                        zz=(int) z;
                        n=modf(z,&d) ;
                        n=10*n;
                        if (n==) *(pstatar+index)=0;
                        else *(pstatar+index)=1;
                        m=(double) zz;
                        if (zz==0) break;
                        }
        }

hextobin(hexnum,fbinum)
/*converts a 4 digit hex number to its equivalent 16 bit
  binary string, hexnum is a hex integer and fbinum is treated as a
  character array. fbinum is passed as a pointer.*/
long int hexnum;
int fbinum[];
        {/*start function*/
        int n,m;
        int *pfbinum,p,shdigit;
   int hdigit;
        extern dind;

                pfbinum=fbinum;
                m=0;
                for (n=0;n<4;n++)
                        {/*start for n*/
                        switch (n)
                                {/*start switch*/
                                case 0 : hdigit= (int)(hexnum << 12);hdigit
                                default:printf("error1\n");
                        }/*end switch*/

                shdigit=(int) hdigit;

                switch (shdigit)
                        {/*start switch*/
                        case 0x0:*(pfbinum+m)=0;*(pfbinum+m+1)=0;*(pfbinum+m+
                        case 0x1:*(pfbinum+m)=1;*(pfbinum+m+1)=0;*(pfbinum+m+
                        case 0x2:*(pfbinum+m)=0;*(pfbinum+m+1)=1;*(pfbinum+m+
                        case 0x3:*(pfbinum+m)=1;*(pfbinum+m+1)=1;*(pfbinum+m+
                        case 0x4:*(pfbinum+m)=0;*(pfbinum+m+1)=0;*(pfbinum+m+
                        case 0x5:*(pfbinum+m)=1;*(pfbinum+m+1)=0;*(pfbinum+m+
                        case 0x6:*(pfbinum+m)=0;*(pfbinum+m+1)=1;*(pfbinum+m+
                        case 0x7:*(pfbinum+m)=1;*(pfbinum+m+1)=1;*(pfbinum+m+
                        case 0xfff8:*(pfbinum+m)=0;*(pfbinum+m+1)=0;*(pfbinum
                        case 0xfff9:*(pfbinum+m)=1;*(pfbinum+m+1)=0;*(pfbinum
                        case 0xfffa:*(pfbinum+m)=0;*(pfbinum+m+1)=1;*(pfbinum
                        case 0xfffb:*(pfbinum+m)=1;*(pfbinum+m+1)=1;*(pfbinum
                        case 0xfffc:*(pfbinum+m)=0;*(pfbinum+m+1)=0;*(pfbinum
                        case 0xfffd:*(pfbinum+m)=1;*(pfbinum+m+1)=0;*(pfbinum
                        case 0xfffe:*(pfbinum+m)=0;*(pfbinum+m+1)=1;*(pfbinum
                        case 0xffff:*(pfbinum+m)=1;*(pfbinum+m+1)=1;*(pfbinum
                        default:printf("error2 \n") ;
                        }/*end switch*/
                m=m+4;
                }/*end for n*/
        }/*end function*/

stategen(fbinum)
/*generates the state transition table for NEXTSTATE.
  NEXTSTATE is then stuffed into the array OUTPUT.
*/
int fbinum[];
        {
        int *pfbinum,STATE,n;
        extern OUTPUT[],dind,statar[];
        int *poutput,*pstatar,index;

                poutput=OUTPUT;
                pfbinum=fbinum;
                pstatar=statar;

                STATE =PS0+(PS1*2)+(PS2*4)+(PS3*8)+(PS4*16)+(PS5*32);

                switch (STATE)
                        {
                          case 0:
                              NEXTSTATE=1;break;
                          case 1:
                              NEXTSTATE= 2;break;
```

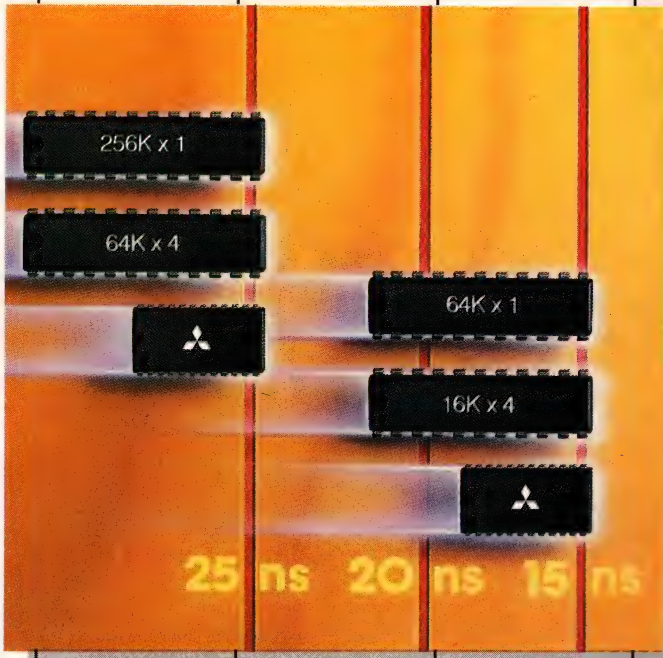
Listing continued on page 240

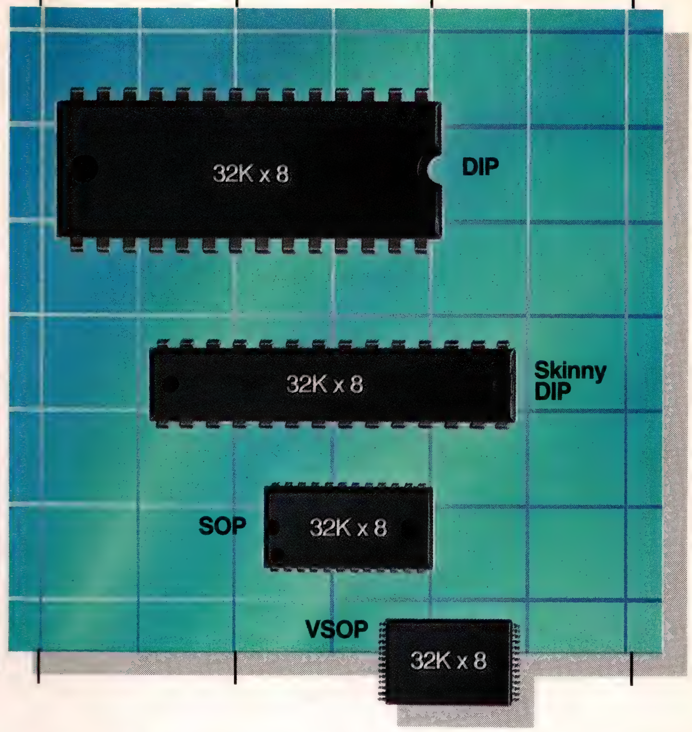
LISTING 1 *(Continued)*

```
                        case 2:
                            NEXTSTATE= 3;break;
                            .
                            .
                            .
                        case 39:
                            NEXTSTATE= 0;break;
                                            default:NEXTSTATE=0;
                                }/*switch*/

                dectobin(NEXTSTATE);/*convert NEXTSTATE to binary & stuff int
                NS0=statar[0];/**(pstatar+0) ;*/
                NS1=statar[1];/**(pstatar+1) ;*/
                NS2=statar[2];/**(pstatar+2) ;*/

        }

outputgen(fbinum)
/*generates the state machine output, these outputs are then
  stuffed into the array OUTPUT.
*/
int fbinum[];
        {
        int *pfbinum,STATE;
        extern OUTPUT[],dind;
        int *poutput,index;
        int NNEXTSTATE;

                NNEXTSTATE=(int) NEXTSTATE;
                poutput=OUTPUT;
                pfbinum=fbinum;
                switch (NNEXTSTATE)
                        {
                  case 0:
                      PFLAG= 1;
                      SOUT= SIN;
                  break; case 1:
                      SOUT= SIN;
                      PFLAG= 1;
                  break; case 2:
                      SOUT= 0;
                      PFLAG= 0;
                  break; case 3:
                      PFLAG= 0;
                      SOUT= 0;
                  break; case 4:
                      PFLAG= 0;
                      SOUT= 0;
                  break; case 5:
                      PFLAG= 0;
                      SOUT= 0;
                  break; case 6:
                      PFLAG= 0;
                      SOUT= 0;
                  break; case 7:
                      PFLAG= 0;
                      SOUT= 0;
.
.
.
                  break; case 31:
                      PFLAG = 0;
                      SOUT = 0;
                  break; case 32:
                      PFLAG = 0;
                      SOUT = 0;
                  break; case 33:
                      PFLAG = 0;
                      SOUT = 0;
                  break; case 34:
                      PFLAG = 1;
                      SOUT = 0;
                  break; case 35:
                      PFLAG = 0;
                      SOUT = 0;
                  break; case 36:
                      PFLAG = 0;
                      SOUT = 0;
                  break; case 37:
                      PFLAG = 0;
                      SOUT = 0;
                  break; case 38:
                      PFLAG = 0;
                      SOUT = 0;
```

Listing continued on page 242

STATIC RAM Performance and Technology





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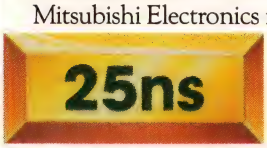

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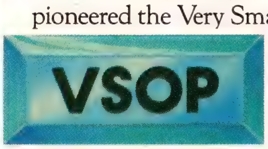

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			ACCESS TIME (ns)											PACKAGE OPTIONS*			
DENSITY	ORGANIZATION	PART NO.	15	20	25	35	45	55	70	85	100	120	150	PDIP	SOP	SOJ	VSOP
16K	16K x 1	M5M21C67					■	■						■			
	4K x 4	M5M21C68					■	■						■			
64K	64K x 1	M5M5187	■	■	■	■	■	■						■		■	
	16K x 4	M5M5188	■	■	■	■	■	■						■		■	
		M5M5189 ($\overline{OE}$)	■	■	■	■								■		■	
	8K x 8	M5M5178				■	■	■						■			
72K	8K x 9	M5M5179				■	■	■						■			
256K	256K x 1	M5M5257			■	■	■	■						■		■	
		M5M5260 ($\overline{OE}$)			■	■								■		■	
	64K x 4	M5M5258			■	■	■	■						■		■	
	32K x 8	M5M5255 (CS/$\overline{CS}$)							■	■	■	■	■	■	■		
		M5M5256							■	■	■	■	■	■	■		■

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LISTING 1 *(Continued)*

```
                    break; case 39:
                        PFLAG = 0;
                        SOUT = 0;break;
                                    default:PFLAG = 0;SOUT = 0;
                          }/*switch*/

        }

jedhed(fp)
FILE *fp;

{
int index;
char ch;

putc ('\x02',fp) ;
for (index=0;index<30;index++)
{
ch=msg1[index] ;
putc(ch,fp) ;
if (ch=='\0') break;
}
putc('\r',fp);
putc('\n',fp);
for (index=0;index<30;index++)
{
ch=msg2[index] ;
putc(ch,fp) ;
if (ch=='\0') break;
}
putc('\r',fp) ;
putc('\n',fp) ;
for (index=0;index<30;index++)
{
ch=msg3[index] ;
putc(ch,fp) ;
if (ch=='\0') break;
}
putc('\r',fp) ;
putc('\n',fp) ;
for (index=0;index<30;index++)
{
ch=msg4[index] ;
putc(ch,fp) ;
if (ch=='\0') break;
}
putc('\r',fp) ;
putc('\n',fp) ;
for (index=0;index<30;index++)
{
ch=msg5[index] ;
putc(ch,fp) ;
if (ch=='\0') break;
}
{
ch=msg7[index] ;
putc(ch,fp) ;
if (ch=='\0') break;
}
putc('\r',fp) ;
putc('\n',fp) ;
}
#if 1
chksum(fp)
FILE *fp;
{
int index;
char ch;
putc('\x03',fp) ;
for (index=0;index<30;index++)
{
ch=msg6[index] ;
putc(ch,fp) ;
if (ch=='\0') break;
}
}
#endif
```

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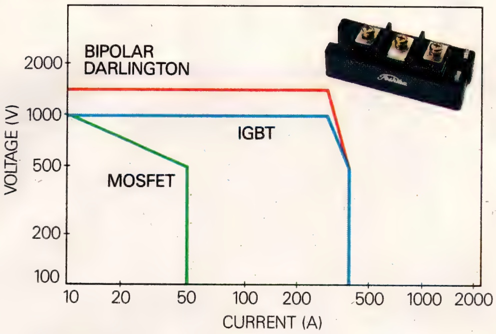

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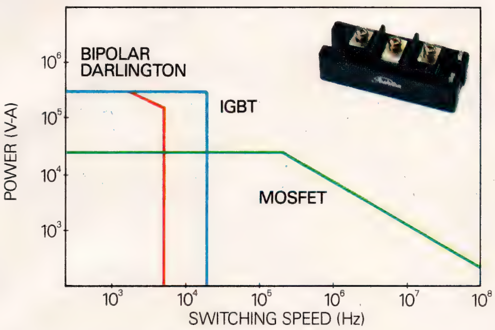

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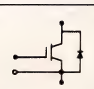
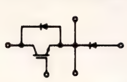
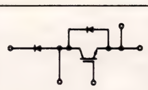
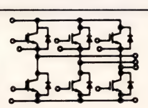
Compare Selection

IGBT (Insulated Gate Bipolar Transistor) Selection Guide

CIRCUIT	SYMBOL	V_{CES}(V)	MAXIMUM RATING COLLECTOR CURRENT Ic (A) 8	15	25	50	75	100	150	200	300	400
	BS	500		GT15H101† MG15H1BS1	GT25H101† MG25H1BS1	GT50G101† (400V) MG50H1BS1	MG75H1BS1*	MG100H1BS1				
		1000	GT8N101†*	GT15N101† MG15N1BS1	MG25N1BS1	MG50N1BS1	MG75N1BS1*					
	US	500									MG300H1US1	MG400H1US1
		600									MG300J1US1*	MG400J1US1*
		1000								MG200N1US1*	MG300N1US1*	
		1200								MG200Q1US1*	MG300Q1US1*	MG400Q1US1*
	YS	500			MG25H2YS1	MG50H2YS1	MG75H2YS1	MG100H2YS1	MG150H2YS1	MG200H2YS1		
		600					MG75J2YS1*	MG100J2YS1*	MG150J2YS1*	MG200J2YS1*		
		1000		MG15N2YS1	MG25N2YS1	MG50N2YS1	MG75N2YS1	MG100N2YS1	MG150N2YS1*			
		1200			MG25Q2YS1*	MG50Q2YS1*	MG75Q2YS1*	MG100Q2YS1*	MG150Q2YS1*	MG200Q2YS1*		
		1400			MG25S2YS1*							
	JS	1000			MG25N1JS1							
	ZS	500				MG50H1ZS1						
		1000			MG25N1ZS1							
	ES	500		MG15H6ES1*								
		1000	MG8N6ES1*	MG15N6ES1*								

†Non Isolated Type TO-3P *Under Development

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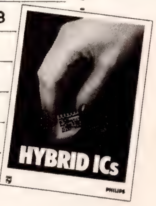

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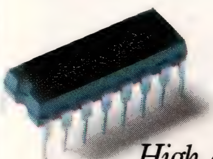

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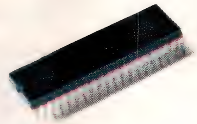

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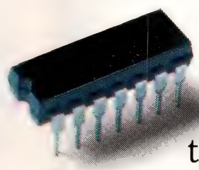

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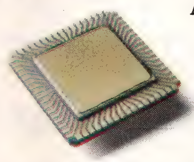

Toshiba's semi-custom families use 1.5μ and 1.0μ CMOS processes to give you the competitive edge. And our cell-based Super Integration technique combines Z80, 82CXX and specialty megacells with logic for true "system-on-a-chip" ASIC solutions.

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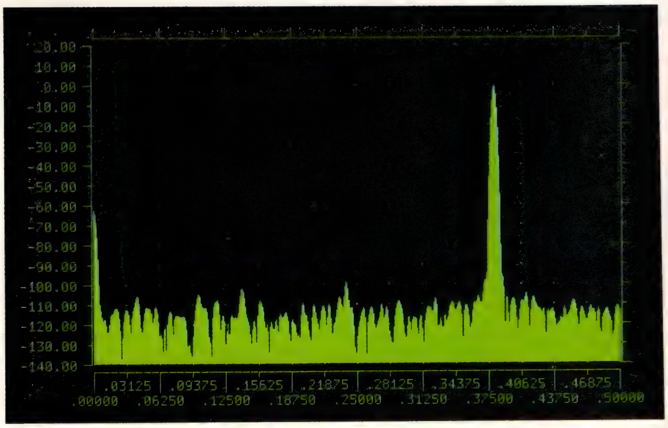
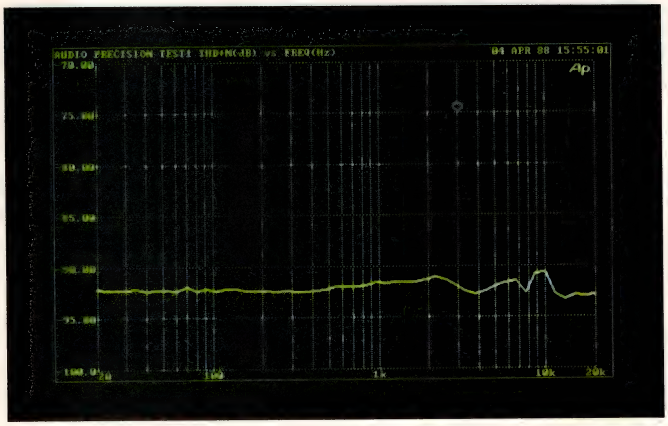
CIRCLE NO 222

Stop, look, listen.



FFT: Detailed distribution of noise and harmonic distortion vs. input signal. Measurement of sample and hold and ZAD2716 A/D converter only. Computer analysis receives digital information from A/D converter (to avoid DAC reconstruction distortion).



Using an Audio Precision system, a sine wave is digitized by the ZAD-2716, then reconstructed by the ZDA-1801, and filtered by Apogee's 944S linear phase filter. Graph shows combined total harmonic distortion and noise vs. frequency.

Introducing the world's finest professional 16-bit stereo digitizing subsystem and 18-bit deglitched reconstruction DAC.

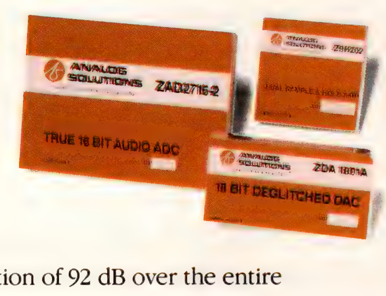
Want to position yourself at the leading edge of digital audio? Then hear this.

Analog Solutions gives you a new family of professional audio products with confirmed "Golden Ear" performance using the industry's two most powerful test criteria. The eye. And the ear.

If seeing is believing, you'll be impressed by the harmonic distortion and noise plots of our ZAD2716/ZSH202 digitizing subsystem (left) and ZDA1801 deglitched reconstruction DAC (right). Nobody's ever seen plots like those before.

But there's more to the story than a good plot.

The ZAD2716-2 coupled with the ZSH202 Dual Sample-Hold can provide stereo digitizing at a 50 kHz sampling rate per channel. The ZSH202 allows simultaneous sampling of both channels within ± 2 nsec with guaranteed −96 db/channel separation. And there's no sacrifice of phase linearity or sin x/x. In fact, we guarantee sin x/x performance of 0.01dB and phase linearity of 0.1 (degree) over 0 to 20 kHz. (Performance that brings a smile to any Golden Ear.) Cost savings are significant on a per channel basis, because you only need one converter for two channels.



Our ADC is also available in a ZAD2716-1 model with integral sample and hold amplifier and 100 kHz sampling speed for 2X oversampling applications.

Your needs extend over the entire audio spectrum. And that's how our products are tested. We test the way they're used. So we can guarantee signal-to-noise plus harmonic distortion of 92 dB over the entire 0-20 kHz audio range.

We maintain the same outstanding performance at the back end of your system with the ZDA1801. This 18-bit DAC, with a built-in deglitcher operating up to 200 kHz for up to 4X oversampling, offers guaranteed signal-to-noise plus harmonic distortion of 94 dB over the full audio range.

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CIRCLE NO 223

Evaluate your ADC by using the crossplot technique

You don't need expensive or specialized test equipment to dynamically evaluate high-performance A/D converters. By performing the crossplot bench-test technique—and interpreting the results correctly—you can determine how closely an ADC's actual performance corresponds to its data-sheet specifications.

Ron Knapp, *Maxim Integrated Products*

Before you commit a particular high-speed A/D converter to your design, you must verify its performance and accuracy at the desired conversion speed. Unfortunately, relying on the spec sheets alone to make your decision may not be enough. Some ADCs are specified very conservatively; others are made to operate right at their limits. Because data sheets give no indication of how rapidly an ADC's performance degrades beyond the maximum conversion speed, you must be sure you never exceed that speed unless you know what to expect. Further, it may be risky to depend on an ADC that's operating close to its limits, particularly when you take the clock-speed tolerance and temperature coefficient (which is often unspecified) into account.

To find out how well an ADC meets its performance specs, you'll need to perform additional testing. ADCs, however, are difficult to test. A range of ADC inputs may give only one output, a phenomenon that's sometimes referred to as quantization error. To measure the actual transfer function of the converter under test, you must sweep the input through a range of voltages and map output codes to input ranges. You can use a technique known as a "crossplot" to perform this mapping operation (see **box**, "An overview of the crossplot test").

Crossplot indicates fastest conversion speed

You can construct a crossplot test fixture from readily available components and standard laboratory equipment. The crossplot test allows you to check the ADC's accuracy dynamically at its rated conversion speed. Beyond that, the test will help you determine the fastest conversion speed possible for your ADC. By "dialing in" any code, you can determine the ADC's integral linearity, differential linearity, and noise, and you can also find other unexpected problems. (The **box** "Distinguish ADC resolution from accuracy" defines and clarifies some ADC specifications.)

You can use the crossplot technique to test an A/D converter such as the AD578, a 12-bit, high-speed successive-approximation converter (**Fig 1**). You can easily extend the test method and interpretation to other converters.

Examining some typical crossplot codes will help you

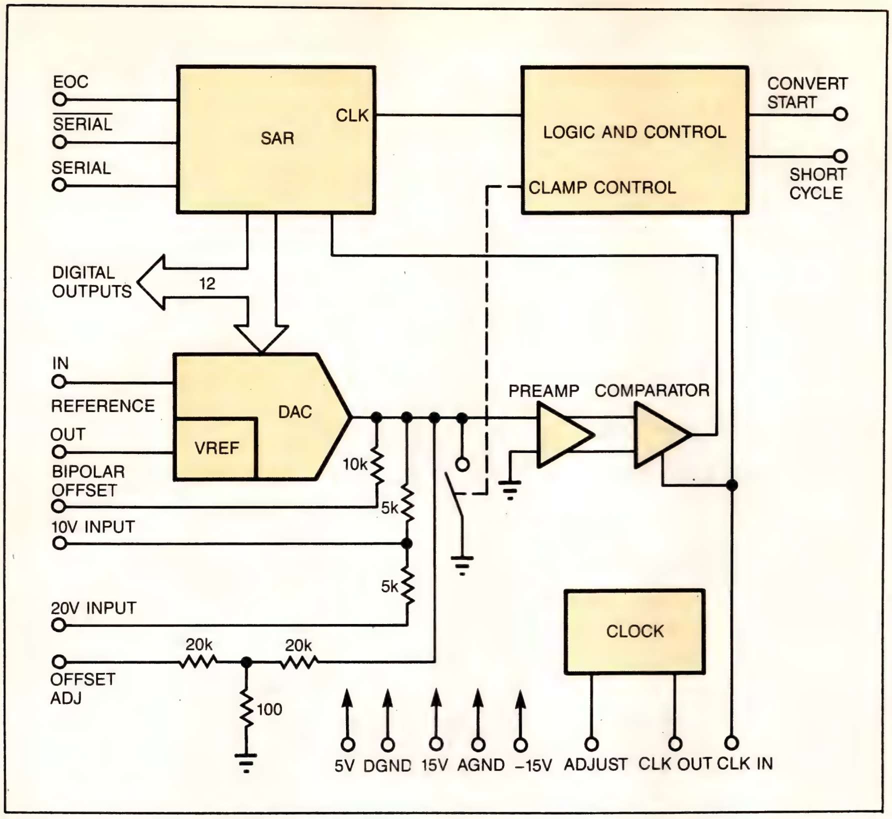

Fig 1—You can use the crossplot technique to test an A/D converter such as the AD578, a 12-bit, high-speed successive-approximation converter from Analog Devices (Maxim is an alternate source for the part).

diagnose specific converter problems. A perfect code, shown in **Fig 2**, is exactly one division wide, is the same width as all the other codes, and is centered on the CRT in such a way that the transitions line up on the vertical lines. If your ADC has integral-linearity error, all the codes on the CRT will shift left or right **(Fig 3)**. If the data-sheet limit is ±½ LSB, the maximum allowable shift is ±½ division. In **Fig 3**, the differential linearity is perfect when all code widths are equal to 1 LSB.

If the integral linearity is perfect, but there are differential-linearity errors, the codes will not be shifted, but one or more codes will be narrow, at the expense of an adjacent one that's wider by the same amount **(Fig 4)**. Differential-linearity errors of this type are normally due to dynamic errors, either within the ADC, such as insufficient DAC settling at major transitions, or externally, from insufficient input amplifier bandwidth (and/or settling time) or from improper grounds.

To find whether the errors are dynamic-linearity errors (and not, for example, static or dc errors caused by a mistrimmed bit in the internal DAC), you should decrease the ADC's conversion speed by a factor of two or more. If the codes become good, dynamic errors are degrading the performance. Evaluating your grounding scheme at this point may uncover a layout problem that you can solve easily. Grounding is so critical for high-speed ADCs that it's usually the root of the problem. You should also take another look at

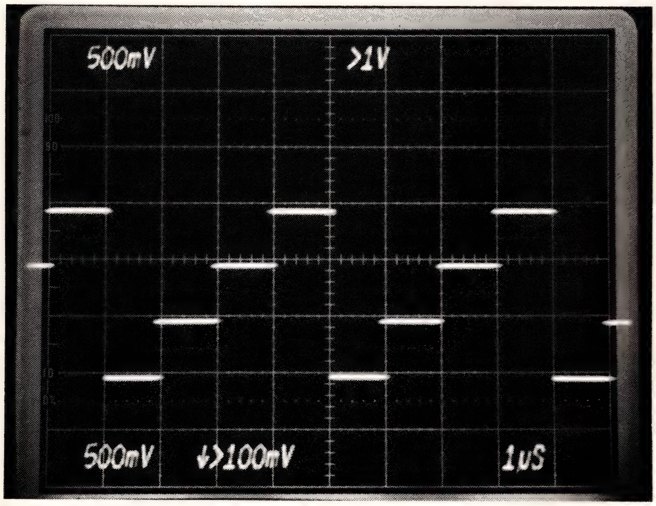

*Fig 2—**In a perfect code,** all the code widths are equal, and all the code transitions occur on the scope's vertical lines.*

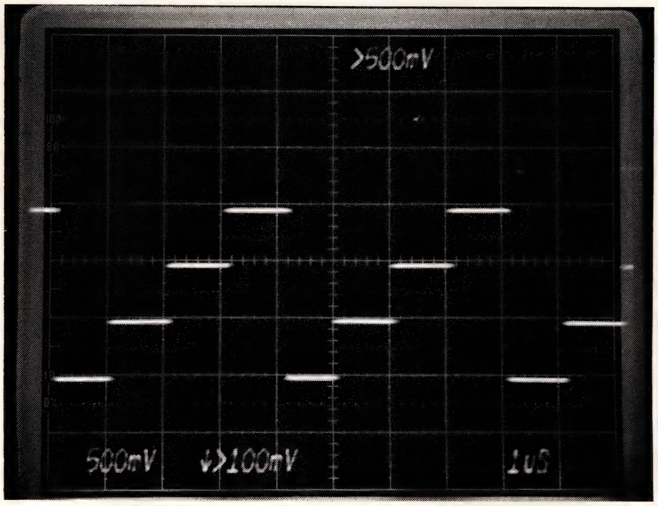

*Fig 3—**An integral-linearity error in the ADC** causes all the codes to shift (in this case, they shift left by 1 LSB).*

Data sheets alone may not be enough to help you select the best ADC for your application; additional testing will tell you what the data sheets don't.

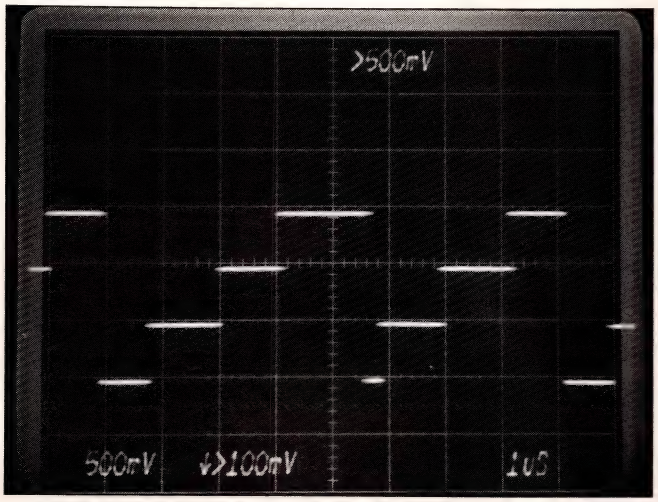

Fig 4—A differential-linearity error in the ADC *causes one code to narrow while the adjacent code widens.*

Fig 5—Missing codes occur *when an ADC's differential nonlinearity is >1 LSB.*

the amplifier's bandwidth spec. If the linearity is just as bad at slow speeds as at fast ones, the errors are probably due to the ADC alone, and the only solution is to replace it or correct the errors in software.

Differential-linearity errors greater than 1 LSB are called missing codes, because the ADC output jumps two or more codes for every LSB voltage increment. The code is "missing" because there is no input voltage that will produce that code. **Fig 5** shows an ADC with one missing code. A convenient way for you to determine the fastest possible conversion speed for your ADC is to increase the conversion frequency (assuming the ADC has either an external or an adjustable clock), until you first detect missing codes. The clock rate at this point is the device's maximum conversion speed. Data sheets rarely give you this kind of accuracy-vs-conversion-speed information.

You can tell whether the DAC's internal settling time is the primary speed limitation in the ADC by testing various codes and noting which code-test bit is the first to drop out as you increase the speed. If it's bit 2 (second from the MSB at ¼ of full scale) and/or bits 1 and 2 (at ¾ of full scale) (**Table 1**), in most cases it's the DAC that's preventing the ADC from going faster. In some successive-approximation ADCs, the algorithm allows extra time for the MSB to settle after the DAC is reset to ½ full scale. On the next clock, the DAC will go to either ¼ or ¾ of full scale, depending on whether bit 1 was accepted or rejected. This signal swing is the largest one in the conversion process that must be performed to rated accuracy at full clock speed.

TABLE 1—CROSSPLOT TEST CODES AND SWITCH SETTINGS

FRACTION OF FULL SCALE	BITS	DECIMAL	SWITCH SETTINGS (TEST CODES)
INDIVIDUAL BITS			
1/2	1	2048	1000 0000 0000
1/4	2	1024	0100 0000 0000
1/8	3	512	0010 0000 0000
1/16	4	256	0001 0000 0000
1/32	5	128	0000 1000 0000
1/64	6	64	0000 0100 0000
1/128	7	32	0000 0010 0000
1/256	8	16	0000 0001 0000
1/512	9	8	0000 0000 1000
1/1024	10	4	0000 0000 0100
1/2048	11	2	0000 0000 0010
1/4096	12	1	0000 0000 0001
SUMMATIONS			
1/2	1	2048	1000 0000 0000
3/4	1+2	3072	1100 0000 0000
7/8	1+2+3	3584	1110 0000 0000
15/16	1+2+3+4	3840	1111 0000 0000
31/32	1+2+. . +5	3968	1111 1000 0000
63/64	1+2+. . +6	4032	1111 1100 0000
127/128	1+2+. . +7	4064	1111 1110 0000
255/256	1+2+. . +8	4080	1111 1111 0000
511/512	1+2+. . +9	4088	1111 1111 1000
1023/1024	1+2+. . +10	4092	1111 1111 1100
2047/2048	1+2+. . +11	4094	1111 1111 1110
4095/4096	1+2+. . +12	4095	1111 1111 1111

ables you to map output es, and thereby determine er function for your ADC.

ikely, the crossplot codes on the oscilloscope's will have both integral- and differential-linearity rs associated with them. The differential-linearity rors are straightforward enough, because the code width is relative to the oscilloscope's horizontal divisions and is measured independently of the integral-linearity shift. However, it's difficult to separate integral-linearity errors in the presence of differential-linearity errors, which displace the code transitions.

Fig 6 gives an example of how both integral and differential nonlinearity can appear: The codes on one half of the display are perfect, but an integral-linearity error in the codes on the other half produces a large differential-linearity error where the two steps of the staircase waveform meet. This error is often caused by an interquad divider in the DAC inside the ADC. Many 12-bit DACs are designed with interquad dividers, which are three similar sections of four binary-weighted current sources or R-2R ladder sections. These quads are summed together with the output of a current divider. The current divider is laser trimmed so that the total sum of one quad equals the first bit of the next quad minus one LSB. If it's the ADC's internal circuit that's causing the error, you have no choice but to try another device.

Linearity errors represent only part of the picture. You must also take noise into account. Noise makes the voltage ranges overlap at the transitions between adjacent codes. You'll have to make a tradeoff between noise and accuracy; how much noise you can tolerate in your ADC depends on your accuracy requirement.

Manufacturers rarely specify ADCs' inherent noise in the parts' data sheets, and even when they do, they specify it only in vague terms. To measure the noise

An overview of the crossplot test

An ideal transfer function for a 3-bit ADC is shown in **Fig A**. Note that there is no unique analog value for each digital code and that the ADC output is valid over a range of input signals. The spread of the input signal for a given output code is called the "width" of the code and is ideally 1 LSB.

The crossplot test procedure allows you to determine the actual transfer function of your device. By summing a dc signal with a low-frequency asynchronous triangular or sine-wave signal and applying the result to the ADC under test, you "dither" the ADC output through several codes; either side of the code represents the dc voltage.

The least-significant ADC output bits are decoded by a simple resistive ladder network and plotted vertically on the scope; the ac analog input is plotted horizontally. The result is a repetitive staircase waveform, which is in essence the real transfer function. For testing most ADCs, it is sufficient to decode the two LSBs of the output, thereby obtaining a 4-step waveform.

Before performing the crossplot test, you must calibrate your fixture to the scope display so that you have a known reference point from which to recognize errors. You should calibrate the scope so that one horizontal position represents 1 LSB, and so that code transitions occur on the vertical lines of the display.

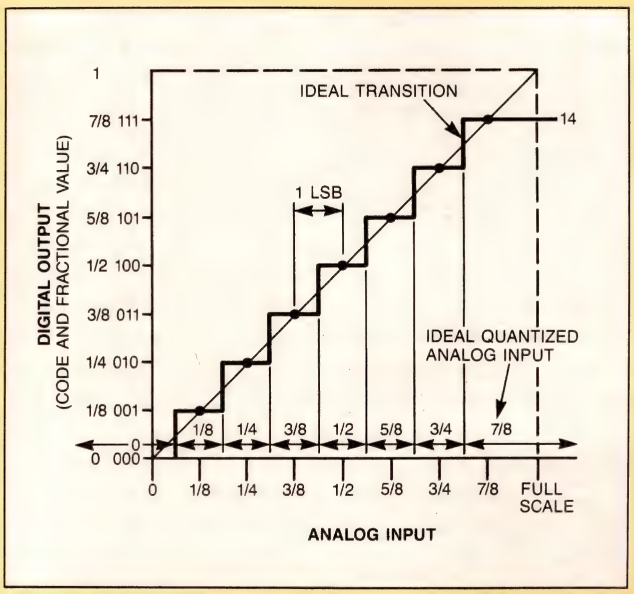

***Fig A—The ideal transfer function** of an ideal 3-bit ADC has even code widths that are equal to 1 LSB.*

The dc signal is provided by a front-end DAC that's controlled by a set of switches. You can select the test for a particular code by setting the switches to the same code. By "dialing in" the codes, you can test any or all of the 2^n possible output codes of your n-bit ADC.

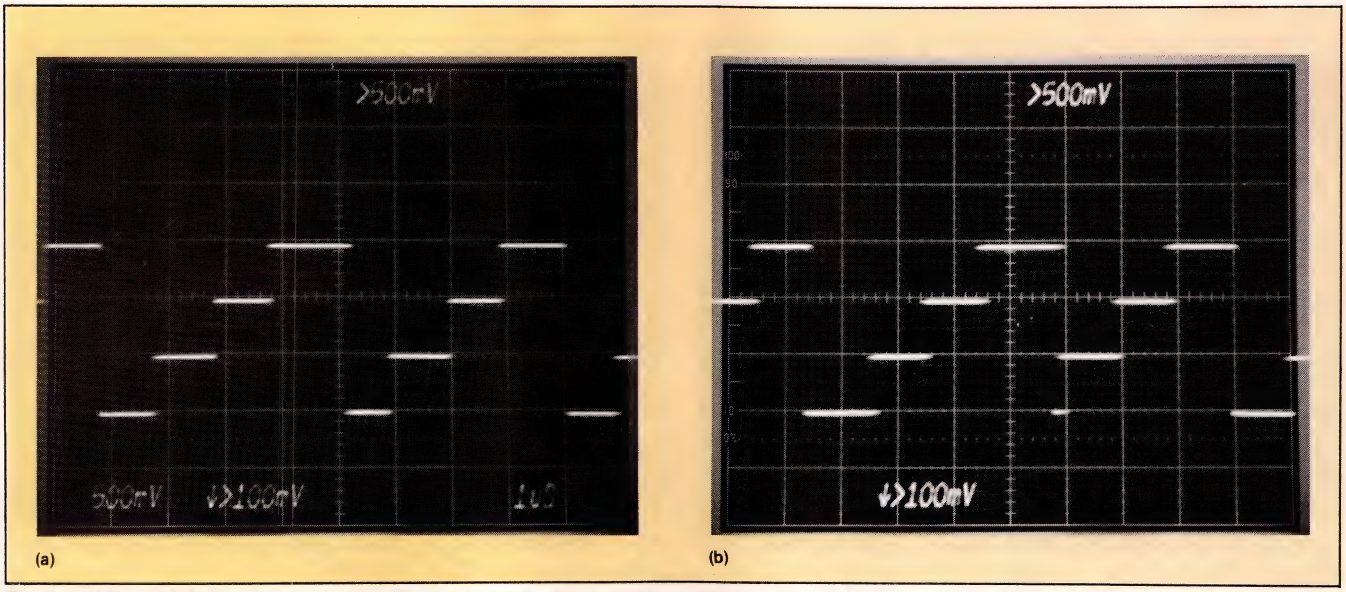

*Fig 6—**Differential-linearity errors** can be produced by integral-linearity errors. In both photos, the codes in the right half of the display are correct, but in the left half, codes shifted left cause wide code at the top **(a)**, and codes shifted right cause narrow code at the bottom **(b)**.*

in an ADC, it's useful to quantify the width of these transition-noise bands. A convenient method of measuring the peak noise is to use a digital storage oscilloscope in the peak-hold or envelope mode (**Fig 7**). Analog scopes don't always give you the true picture of noise, because of the CRT's write-speed and persistence limitations. The rms value of noise is approximately ⅙ of the peak-to-peak transition width.

You can find the noise source by observing where the noise appears in the codes. If the ADC is very noisy at + full scale but acceptable at − full scale when the DAC is off (unipolar mode), the noise is probably coming from the ADC's voltage reference. At − full scale, the reference-voltage noise is attenuated well below the noise of the other components. To find whether the noise is caused by the reference, you place a large capacitor (10 μF) on the reference output or connect a low-noise external reference to the reference input. If the transition noise is reduced, the reference is the problem. If the transition noise doesn't change, there could be noise problems in the internal DAC.

If noise is equally distributed throughout the ADC's range, its cause is something other than the signal level or code. That eliminates the DAC and its reference. Most likely the comparator is at fault. Unfortunately, there is nothing you can do to improve it except to get a better ADC.

The crossplot technique can help you verify that your device meets its accuracy and noise specifications, but it doesn't stop there. ADCs sometimes have problems that result in undesirable effects, even though the devices meet all their data-sheet specifications. These problems may be caused by other inherent design inadequacies within the parts, or they may be induced by external factors such as grounding, shielding, coupling, and other components in your system.

The crossplot can reveal such problems as hysteresis, oscillation, and uneven codes, for instance. The crossplot result in **Fig 8** shows a form of hysteresis,

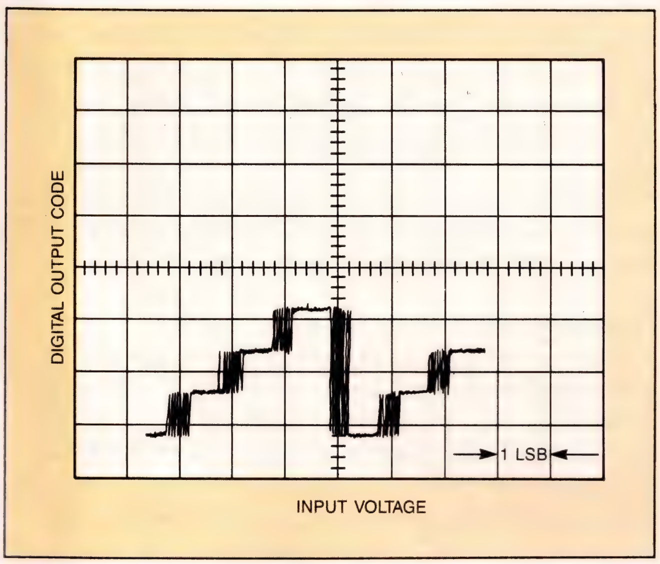

*Fig 7—**You can use the peak-hold function** of a digital oscilloscope to measure the code-transition noise of the device under test.*

The test fixture is made from readily available components and standard laboratory equipment.

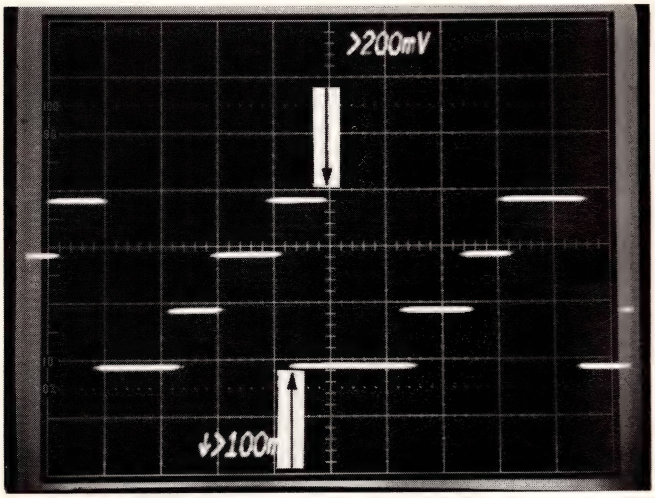

Fig 8—In the crossplot, hysteresis appears as an overlap *of two adjacent codes.*

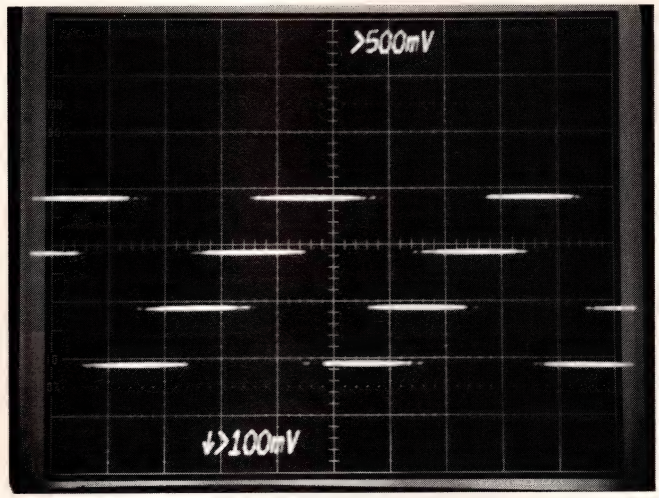

Fig 9—Transition pulses appearing in the crossplot results *may be caused by comparator oscillation.*

or overlapping codes. What's occurring is that the staircase signal is tracing two different paths when the scope sweeps right and left. In other words, the code width depends on whether the ADC previously converted to a higher input voltage or a lower one. Hysteresis is most often caused by DAC problems, such as excessive dielectric absorption in the output capacitance, or by disturbances introduced at the internal-summing-junction connection between the DAC output and the comparator input.

Normally, you'd expect the transition noise to be purely random—that is, if it's actually caused by component noise in the ADC. But if you can discern any pattern that looks like pulses **(Fig 9)**, some comparator oscillation is probably occurring when the comparator inputs are nearly equal. To help avoid oscillation problems, most high-speed comparators in fast ADC applications employ a strobed output. Such an output is strobed on for a minimal time after the DAC's output has settled and the bit decision is ready to be clocked into the successive-approximation register.

Test-fixture layout is critical

You would expect to see differential nonlinearity or code-width variations primarily on the major vertical transitions. But when differential-nonlinearity problems are scattered throughout the codes **(Fig 10)**—and the errors are just as bad at − full scale (when all internal-DAC bits are equal to zero) as they are at + full scale (when all internal-DAC bits are equal to one)—chances are that, barring a serious design problem in the ADC, the problems are caused by ground loops and/or crosstalk between the analog and digital sections of the system. To confirm that ground loops and/or crosstalk—and not just gross mismatch of the LSBs—are the source of the trouble, you decrease the ADC's conversion speed. If the codes become uniform, the ADC is fine, and you must clean up the grounding and the circuit layout.

The design and layout of your fixture is a critical factor in obtaining accurate test results. A ground-plane pc board is desirable, but it's not necessary if you maintain a star-ground system in which the ADC analog ground is the center. The crossplot fixture shown in **Fig 11** consists of an input buffer amplifier, two octal-output data registers, a dual one-shot config-

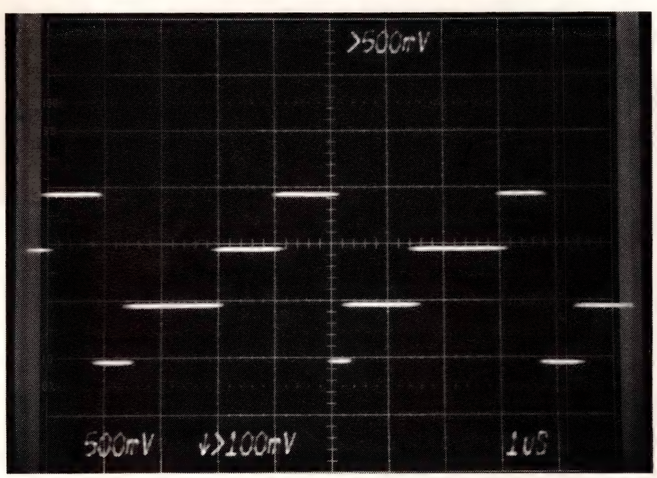

Fig 10—A repeating pattern of uneven codes *looks like differential nonlinearity, but it's wise to check the grounding and bypassing before blaming the ADC.*

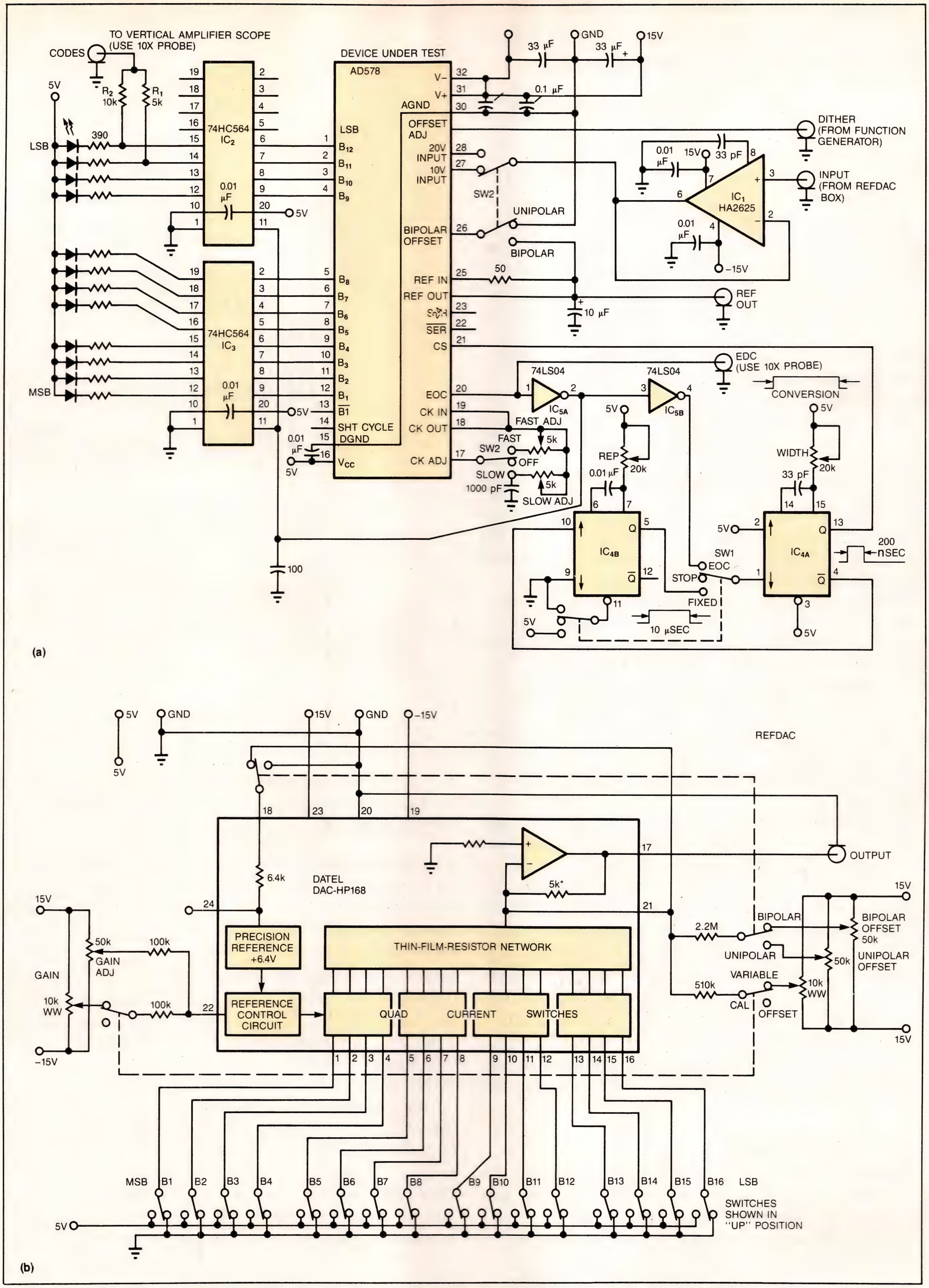

Fig 11—The crossplot test fixture consists of a buffer amplifier, data registers, and a dual one-shot (**a**), and a reference DAC (**b**).

The crossplot test easily picks up missing codes and differential-linearity errors.

ured as a convert-start-pulse generator, and a reference DAC that's normalized to the ADC under test. Instead of adjusting the offset and gain of the ADC, you can simply force the offset and gain of the reference DAC to conform to the ADC. This procedure gives you a more general test fixture, because different ADCs have different calibration schemes and adjustment ranges, and some don't have any provision at all for calibration.

Further, remember that unless you connect remote offset and gain potentiometers as closely as possible to the ADC's inputs, you might degrade the ADC's performance. Although you'd normally use the reference DAC with its mode switch in the Variable position, it also has a Calibrate (Cal) position. When the mode switch is in the Calibrate position, the gain and offset are preset for zero error.

The D/A converter you use as the reference DAC must have much better linearity than the ADC under test. The test-fixture design in **Fig 11** uses the Datel DAC-HP16B to test the 12-bit AD578 (½ LSB=0.012%). The DAC is a 16-bit part with 15 bits of linearity (½ LSB=0.0015%). To test 12-bit ADCs, you use only the top 12 bits of the 16-bit reference DAC. The initial gain and offset of the DAC are not important as long as they're adjustable to zero and they're stable.

You must buffer the reference DAC's output voltage with a high-speed op amp as close to the ADC's input as possible. You may wonder why a high-speed op amp is necessary when only manually switched dc test voltages are applied to the ADC's input. The problem is that the input load current in a successive-approximation ADC changes by as much as several milliamps at each clock or bit decision during the conversion. The output of the buffer or S/H amplifier must recover from this abrupt change and settle back to within a fraction of an LSB (0.012% for ½ LSB of a 12-bit ADC) within the clock period. The internal comparator also requires sufficient setup time so it can make a correct decision.

Choose the right op amp

Many different op amps could buffer the reference DAC adequately, but you can't easily find them just by looking at data-sheet specs, because very few data sheets list the parts' settling time to 0.01%. For testing the 3-μsec AD578, the Harris HA-2625 op amp works well as long as you apply about 33 pF of external compensation and bypass the supplies. For faster

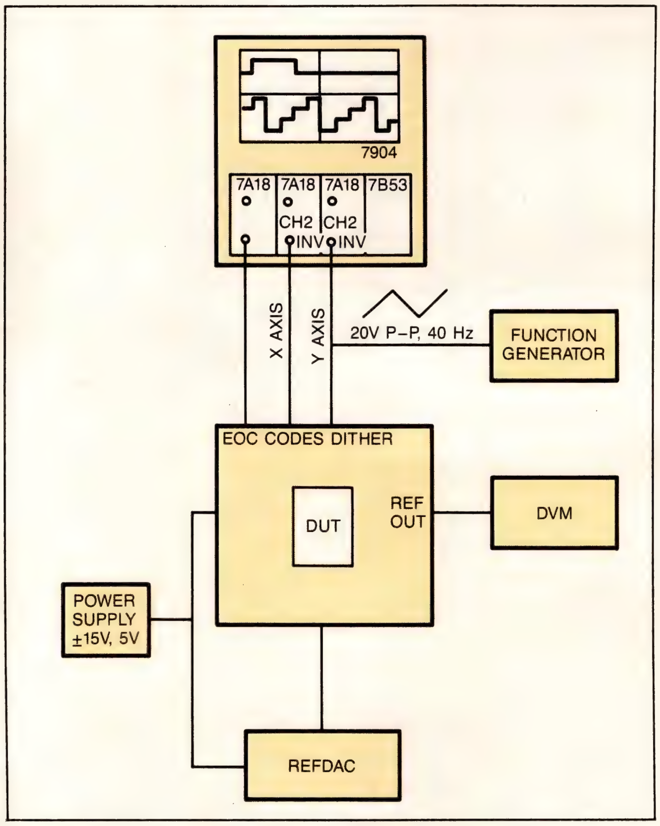

Fig 12—You can use this diagram as a guide *in connecting your crossplot setup.*

ADCs, you may need to use a booster configuration: an op amp and a high-speed buffer in a feedback loop. The buffer, an LH0033 or LH0053, for example, will absorb the transients from the ADC. Because the buffer is inside the op amp's feedback loop, signal accuracy is maintained at the ADC input. For ADCs that don't have an offset- or zero-adjust input, you'll also need to sum the Dither input into the input buffer amplifier. This summing is not difficult, but your choice of amplifier is critical.

Because intermediate codes appear at the output during the conversion, octal registers IC_2 and IC_3 clock the valid data only at the end of each conversion. When testing an ADC with complementary-binary-output coding, you should replace IC_2 and IC_3 with a 74HC574, which is a noninverting octal register. The end-of-conversion signal (EOC) also serves to trigger a one-shot, IC_{4A}, which initiates the next conversion with SW1 in the EOC mode. If you want to set the repetition rate independently of the conversion speed, you can use IC_{4B} to retrigger IC_{4A}, as long as you set

SW1 to the Fixed position. A center-off toggle switch permits you to stop the conversion process.

The LEDs driven by the output registers help you make sure you're actually testing for the code you dialed in. If the code is the same, the illuminated pattern will match that of the code you selected with the switches on the reference DAC's input. R_1 and R_2 decode the last two LSBs. You can think of R_1 and R_2 as a single-pair R-2R ladder. You can test more bits by using an R-2R-4R set of resistors, which will produce an 8-step staircase on the oscilloscope. Alternatively, you can test for 10-bit performance by moving R_1 and R_2 up to the next two most significant bits.

Fig 12 shows how to connect the test fixture. With an oscilloscope such as the Tektronix 7904, which accepts as many as four plug-in amplifiers, you can simultaneously look at the codes in X-Y mode and at the EOC signal, which displays conversion speed. To do so, you need to configure one of the vertical amplifiers as a timebase amplifier. You set the vertical amplifier control to Alternate and set the timebase mode to Chop.

To make the crossplot results easy to interpret, you need to calibrate the scope display so that each code width fits into one division and all the transitions line up on the vertical lines. You simultaneously turn the OFFSET ADJ pot of the reference DAC and the X-amplifier CAL ADJ knob on the scope. It's best to ignore the bottom codes for this adjustment, because these codes are the most likely to have differential-linearity errors. Instead, you calibrate the scope so that each third high-side transition is separated from the next by exactly four divisions (**Fig 13**).

Next, you need to choose the place on the scope display where the code under test will fall when there are no errors in the system. The typical position is one division to the right of center. To choose that position, you need to make adjustments for system offset and

Distinguish ADC resolution from accuracy

It's important not to confuse resolution with accuracy when selecting an ADC. The resolution (or number of bits) that an ADC has is a measure of the smallest increment of input voltage it can detect that's represented by a change in the LSB of the digital output code. The accuracy, also specified in LSBs, can be lower or higher than the resolution.

The ADC's "accuracy" is determined by the integral and differential linearity of its digital codes. Integral nonlinearity is a measure of how many LSBs an output code is from the theoretically perfect transfer function of the converter. In other words, integral nonlinearity is the deviation of the real transfer function from the ideal straight line.

Differential nonlinearity is the minimum and maximum range of input voltage that causes the codes to change by one count; it's the deviation of the code width from the ideal 1 LSB. For an ADC to have "no missing codes" operation (which implies that no code jumps will be greater than 1 LSB), its differential nonlinearity must be lower than the resolution (1 LSB), and its integral linearity must be less than ½ LSB, because a ½-LSB error on each of the binary weighted output bits would add up to 1 LSB (that is, 1 LSB = ½ + ¼ + , etc).

Most ADCs that have 12 bits or less of resolution have linearity specs that match the resolution, but it's common to find 16-bit ADCs with 14-bit accuracy, which means that the output data can be off by as much as 4 LSBs. On the other hand, some ADCs may have higher accuracy than resolution. For example, in a 12-bit ADC with 14-bit accuracy, the output code will have no more than a ⅛-LSB error, and the code width will be between ⅞ and 1⅛ LSB.

The absolute accuracy of the data from an ADC converter depends on many factors. An ADC's linearity is the most important of these, because the only adjustments you can make to correct it are software adjustments. However, to determine the ADC's worst-case error—and therefore its overall accuracy—you need to make a more complete list of error sources, including not only linearity, but also linearity drift, gain, gain drift, offset, offset drift, gain PSRR, and noise.

To determine the accuracy of the overall system, you must also consider error sources from the other components around the ADC, such as the input preamplifier, the multiplexer, the sample/hold amplifier, and the external voltage reference, if you use one.

Integral-linearity errors cause the codes displayed on the CRT to shift left or right.

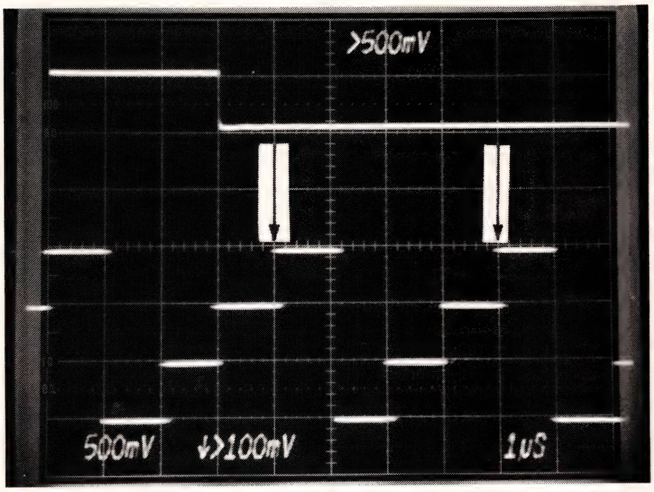

Fig 13—To make the crossplot results easy to interpret, *calibrate the scope so that each third high-side transition (see arrows) is separated from the next by exactly four divisions. This way, each code width will fit into one division, and all the transitions will line up on the vertical lines.*

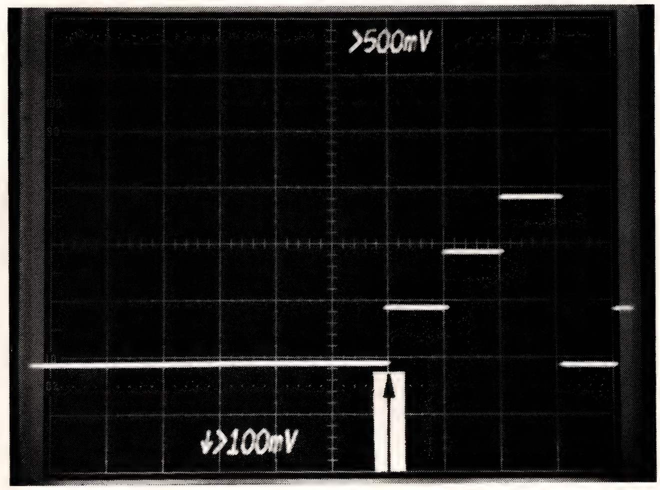

Fig 14—To test an ADC's digital output codes, *you need to choose the place on the scope display where correct codes will fall. For example, if you choose the scope division just to the right of center, you must switch the reference DAC inputs to zero, and, with the OFFSET ADJ pot, you place the first transition on the first vertical line to the right of center.*

gain. First, you switch the reference DAC inputs to zero; then, by using the OFFSET ADJ pot, you place the very first transition on the first vertical line to the right of center. This action places the zero code in the selected box **(Fig 14)**. You must make sure that both the crossplot fixture and the reference DAC are set to the same range, either the unipolar (10V) or the bipolar (20V) range. If the image on the CRT is upside down and/or backwards, you should invert the x and/or the y input as necessary.

Similarly, you adjust the test fixture for gain by switching the first 12 reference DAC inputs to 1 and setting the GAIN ADJ pot so that the last transition falls directly on the center line **(Fig 15)**. This procedure places + full scale in the designated division just to the right of center.

Note that the crossplot test method uses "end-point" linearity calibration, so there's never a linearity error at − full scale or + full scale, which are being normalized. The normalization process rotates the actual transfer-function curve so that + full scale and − full scale are on the ideal straight line. If the ADC exhibits gain-linearity errors, those errors will now occur at ½ full scale. A limitation of this method of calibration is that you can't clearly distinguish gain errors from integral-linearity errors.

The ADC is now ready to be tested. Whatever code is set on the reference DAC's input switches should be in the designated location on the oscilloscope display; that is, it should be one division to the right of center. Any deviation is measured as linearity error. Because the scope is calibrated for a horizontal scale of 1 LSB/div, the errors are measured directly in LSBs.

You can test every ADC output code if you wish, but that's generally considered overkill. The test codes for a 12-bit ADC (shown in **Table 1**) are usually accepted as a thorough test-code set; they test the ADC in its operating range for decimal inputs from 1 to

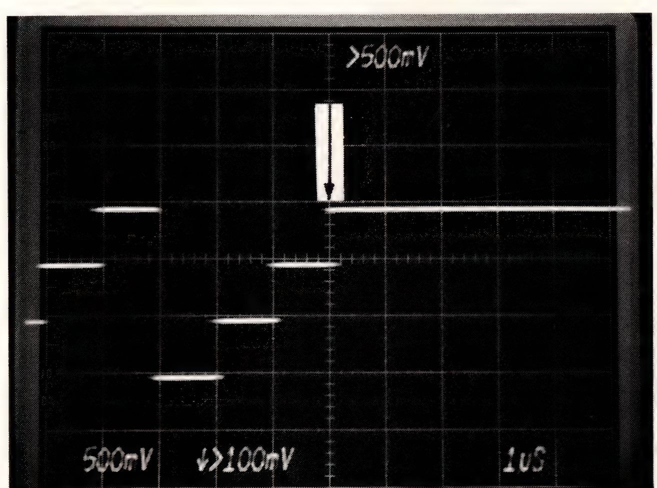

Fig 15—To adjust the test fixture for gain, *you must switch the reference DAC's first 12 inputs to all ones and use the gain-adjustment pot on the reference DAC to line up the last transition on the center of the scope display.*

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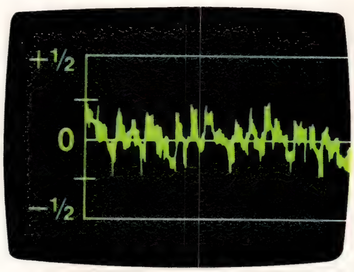

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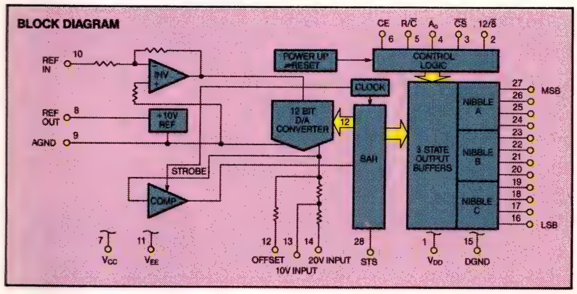

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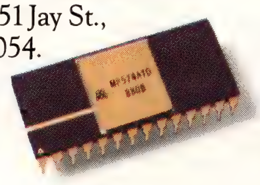

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4095. For those test codes whose two least significant bits are zero, the staircase will be at its lowest level in the division just to the right of center on the scope's CRT. Any code whose last two bits are "01" will display the first staircase level in that scope division. A code whose last two bits are "10" will display the second staircase level in that division, and one whose last two bits are "11" will display the third and top level there. EDN

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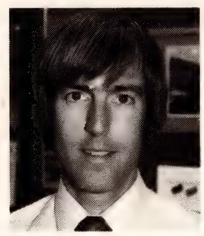
1. Sheingold, Daniel H, ed (Analog Devices Inc), *Analog-Digital Conversion Handbook*, Prentice-Hall Inc, Englewood Cliffs, NJ, 1986.
2. Jung, W, *IC Converter Cookbook*, Howard W Sams Inc, Indianapolis, IN 1978.

Author's biography



Ron Knapp was a senior member of the technical staff at Maxim Integrated Products (Sunnyvale, CA) when he wrote this article. He's currently employed as a project manager at Power Integrations (Mountain View, CA). He holds a BS in systems engineering from Boston University and an MSEE from Worcester Polytechnic Institute, and is vice president of the Northern California Chapter of the International Society for Hybrid Microelectronics (ISHM). In his spare time, Ron enjoys flying, sailing, tennis, and skiing.

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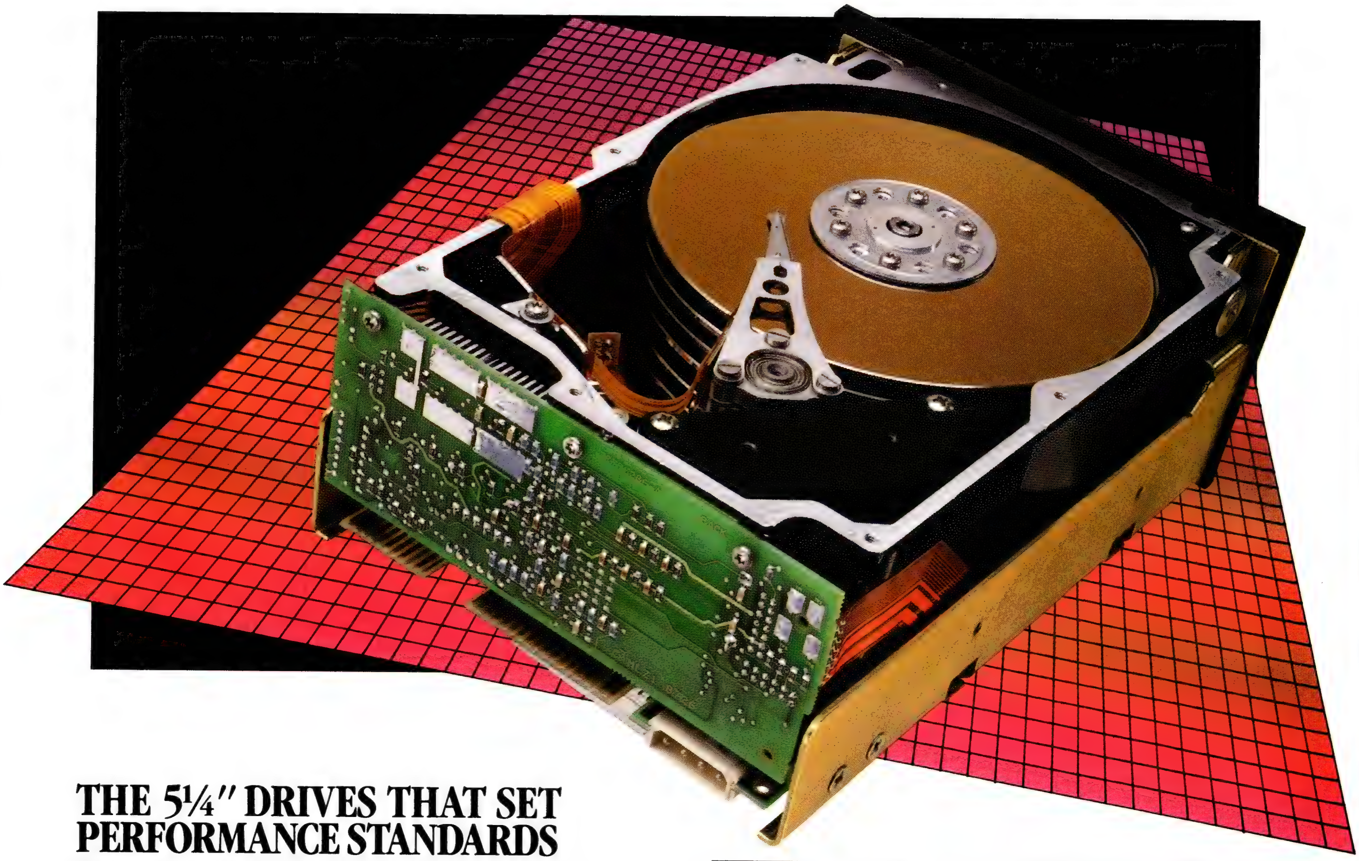

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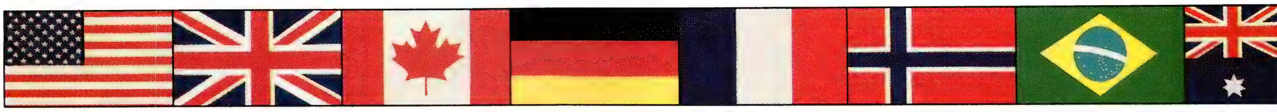
Wren V	442	16	ESDI	10
Wren V	383	14.5	ESDI	10
Wren V H.H.	209	18	SCSI	10-15
Wren IV	376	17.5	SCSI	10-15
Wren III	182	16.5	ESDI	10
Wren III	182	16.5	SCSI	10
Wren III H.H.	106	18	ESDI	10
Wren III H.H.	106	18	SCSI	10
Wren II (RLL)	135	28	ST506-(RLL)	7.5
Wren II	96/86	28	ST506, ESDI	5
Wren II H.H. AT	80/74	28	AT	7.5
Wren II H.H. RLL	77	28	ST506-(RLL)	7.5
Wren II H.H.	51	28	ST506	5

All capacity figures are shown as unformatted.
H.H. = Half Height models



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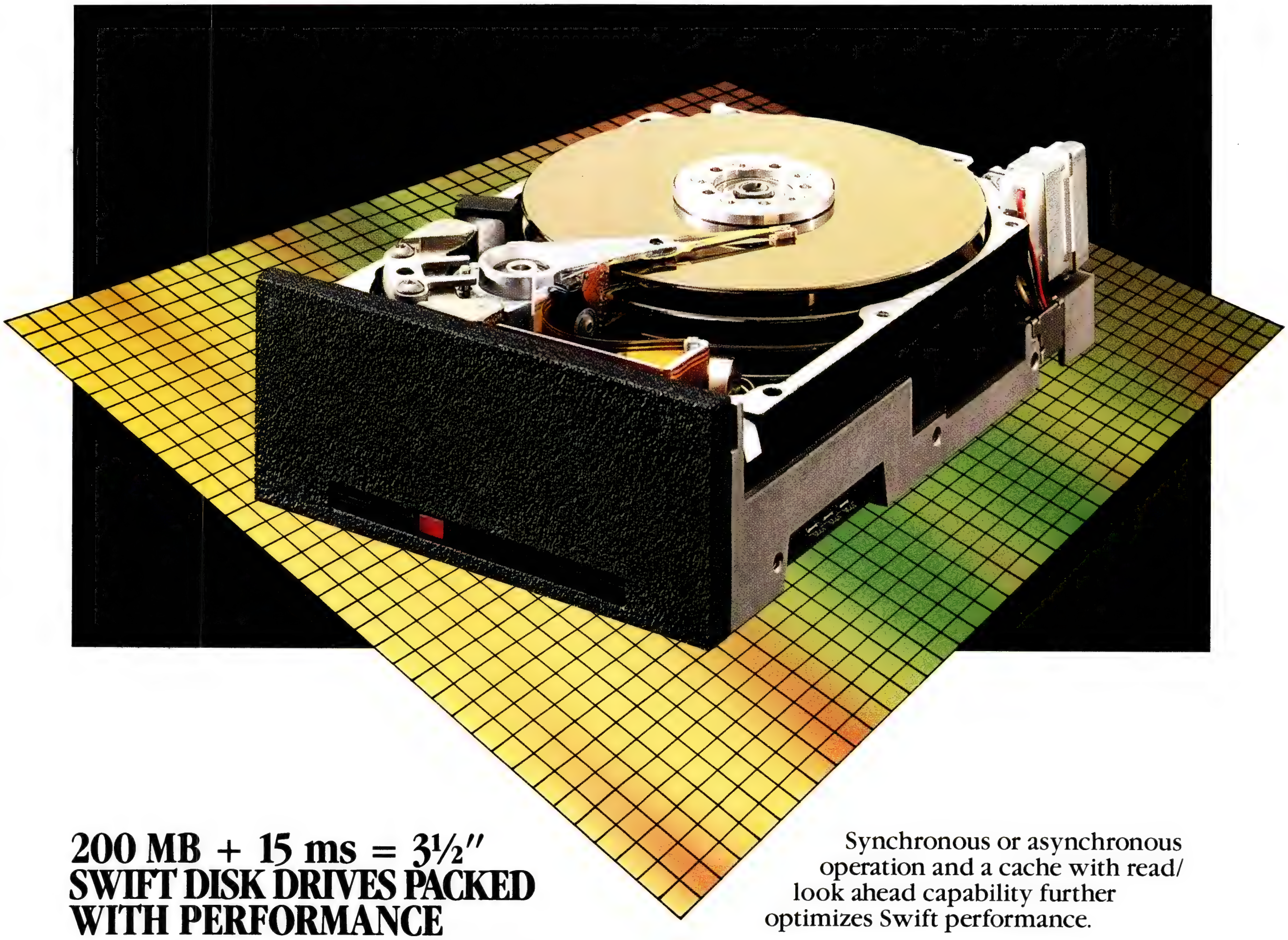

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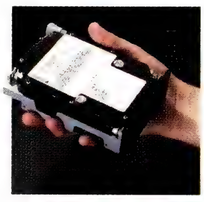

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Swift	150	15	SCSI, ESDI, AT	10
Swift	150	15	ST506/412 (RLL)*	7.5
Swift	100	15	ST506/412 (MFM)*	5

* Not available with 1-to-1 interleave

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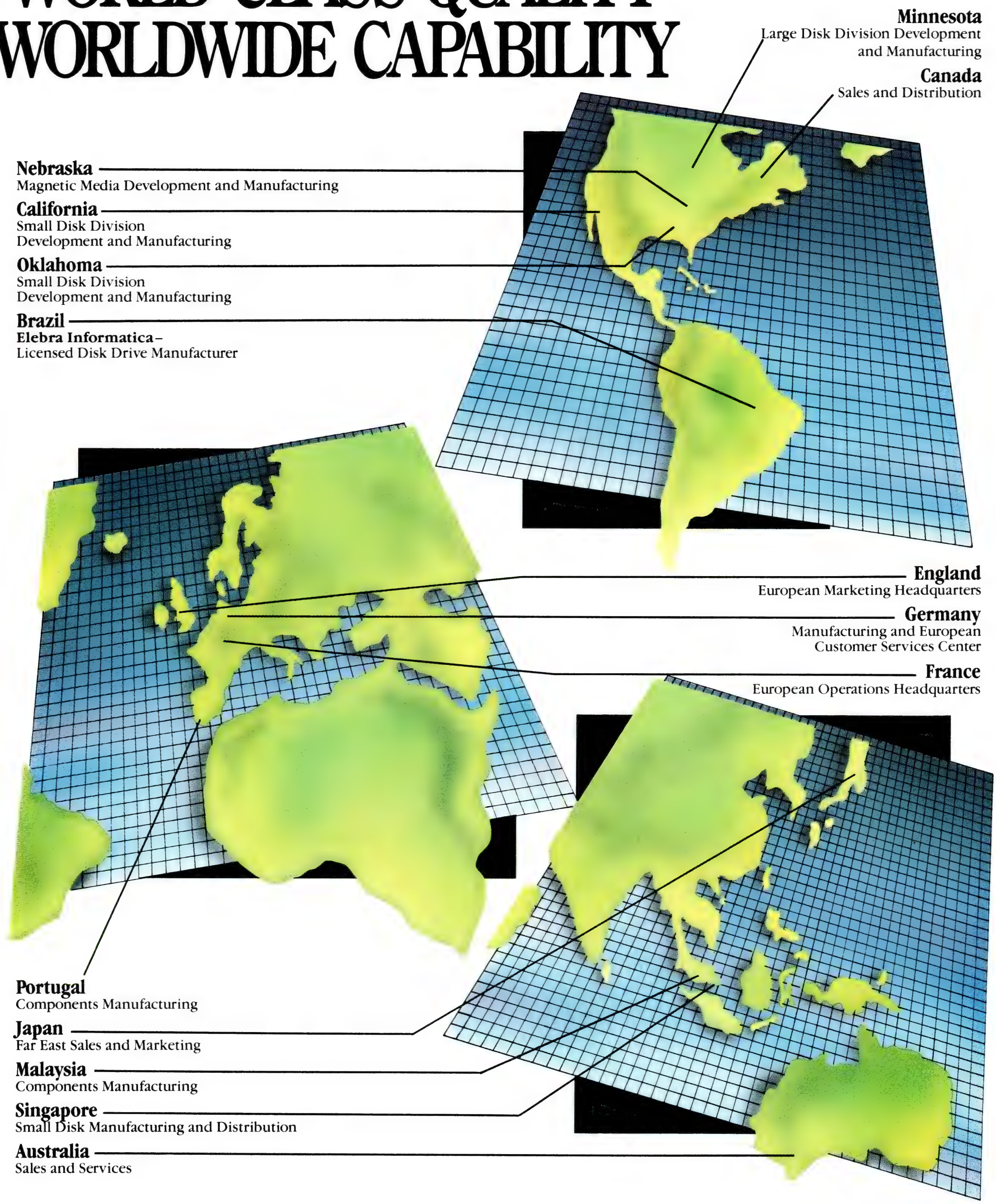

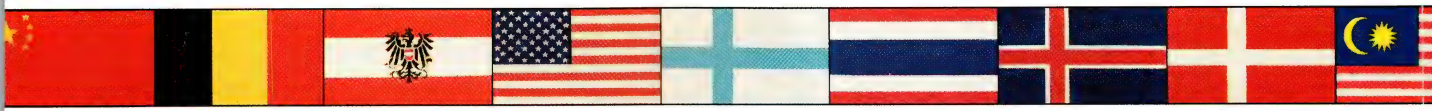

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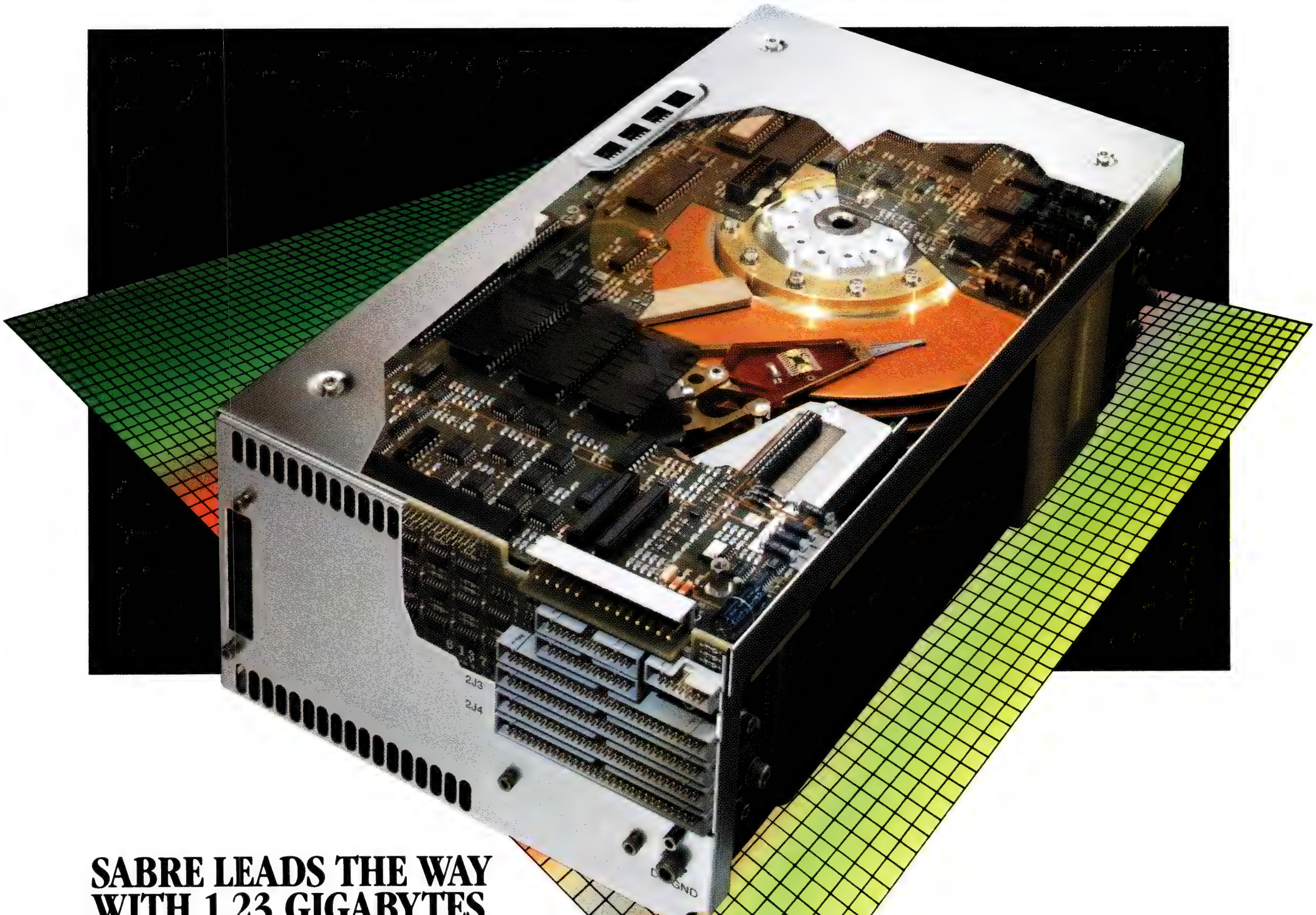

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5V/180A	12V/15A	12V/15A	5V/5A
5V/180A	15V/12A	15V/12A	5V/5A
800w			
5V/120A	12V/12A	12V/12A	
5V/120A	15V/12A	15V/12A	
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A simple technique boosts performance of active filters

To achieve the best rolloff from an active filter, you must keep component values as close as possible to the ideal values so as to preserve critical ratios. Precision components are expensive, but you can gain significant performance improvements without incurring any extra expense by adjusting the impedance levels.

Brent F Balch, *Sensormatic Electronics Corp*

In order to get outstanding performance from complex active filters, especially those of third and higher orders, you have to exercise tight control over component ratios. The usual method of achieving ideal values (which you derive from filter-design tables) is either to purchase high-precision components or to select them individually from a batch of lower-grade components. Unfortunately, precision capacitors are not only expensive, but often have long delivery times; likewise, component selection adds to the cost of manufacture because of its time-consuming nature. However, you do have an alternative: Using a simple computer program, you can select a set of standard 1% (or even 5%) values that most closely matches the ideal values.

This article is not intended to teach filter design. It assumes that you are familiar with filter-design procedures and have access to filter-design tables such as those contained in standard books on the subject (**Refs 1 and 2**). Rather, the article shows you a technique for using a simple computer program (**Listing 1**, pg 284) to extract a few extra decibels from your completed filter designs. The computer program was written in Microsoft Basic because most PC-DOS and MS-DOS machines come with some version of this language. Symbol notation for the various filter parameters conforms to that found in the Williams book (**Ref 2**).

The goal is to maximize performance, and therefore the program assumes that you'll use 1% resistors, which are readily available and cost only pennies. Actually you can even use 5% resistors, but the improvement in performance won't be as dramatic. You obtain increasing benefit from this technique as the filter complexity or the Q of the filter increases, because both cases impose tighter control over component ratios. The best time to make use of this technique is at the point when you select the circuit impedance; at this juncture, the capacitors become the dependent variables. Although you could apply the technique to L-C as well as R-C filter circuits, you'd achieve fewer benefits because inductors are often custom wound for each application. For this reason, the following discussion is limited to R-C active filters.

As a typical design problem, suppose you are developing a product that requires a 1200-Hz, highpass filter

TABLE 1—COMPONENT REFERENCES AND NORMALIZED ELLIPTIC-FILTER VALUES

PASSIVE LOWPASS	ACTIVE LOWPASS	PASSIVE HIGHPASS	ACTIVE HIGHPASS	7P6Z	5P4Z	3P2Z
				105.37 dB*	70.46 dB*	35.55 dB*
L1	R1	$\frac{1}{C1}$	$\frac{1}{C1}$	2.30574	2.23588	2.0251
C1	R2C	$\frac{1}{L2}$	$\frac{1}{C2L}$	1.02339	0.98117	0.8223
L2	R2L	$\frac{1}{C2}$	$\frac{1}{C2C}$	0.05153	0.09644	0.2360
L3	R3	$\frac{1}{C3}$	$\frac{1}{C3}$	3.03231	2.92215	2.0251
C4	R4C	$\frac{1}{L4}$	$\frac{1}{C4L}$	0.96029	0.88914	
L4	R4L	$\frac{1}{C4}$	$\frac{1}{C4C}$	0.24912	0.25766	
L5	R5	$\frac{1}{C4}$	$\frac{1}{C5}$	2.93508	2.09208	
C6	R6C	$\frac{1}{L6}$	$\frac{1}{C6L}$	0.95372		
L6	R6L	$\frac{1}{C6}$	$\frac{1}{C6C}$	0.16907		
L7	R7	$\frac{1}{C7}$	$\frac{1}{C7}$	2.19598		

*DENOTES A(MIN) VALUES

with unity gain and a rejection of at least 65 dB below 600 Hz. The passband ripple must be no more than 1.5 dB. System and manufacturing constraints dictate the best performance possible but forbid the trimming of components because of the attendant cost.

After you determine the required filter parameters, the next step is to compute the filter steepness factor, A_S, as follows:

$$A_S=\frac{f_C}{f_S}=\frac{1200\ \text{Hz}}{600\ \text{Hz}}=2.$$

Filter-design tables indicate that you need a fifth-order elliptic filter. To provide an A_S of 2, the value of the filter parameter Ω_S must not exceed 2.000. This figure results in a value of $\theta=30°$.

Using **Table 1,** select a fifth-order filter that makes the transition from the passband to at least 70 dB of attenuation in the stopband within a frequency ratio (A_S) of 2. If you're using a filter-design table from a standard reference book, look for a design that has the notation C05 50 $\theta=30°$. C indicates a Chebyshev type; 05 indicates a fifth-order filter; 50 (ρ) is the reflection coefficient of the filter. You'll find that the filter has the following parameters: $n=5$; ripple$=1.25$ dB; $\Omega_S=2.000$; and $A_{MIN}=70.46$ dB. **Fig 1a** shows the T configuration of a lowpass filter with normalized values obtained from **Table 1.**

The next design step is to transform the lowpass circuit into a highpass type; you perform this change by converting all the inductors into capacitors and all the capacitors into inductors, using reciprocal values. **Fig 1b** shows the transformed, normalized highpass filter. You likewise reflect the transmission zeros around the cutoff frequency by using reciprocal values.

At this time you denormalize the filter values by using a frequency scaling factor of $\Omega_0=2\pi fc$ and by selecting a circuit-impedance level, Z. It's usual to de-

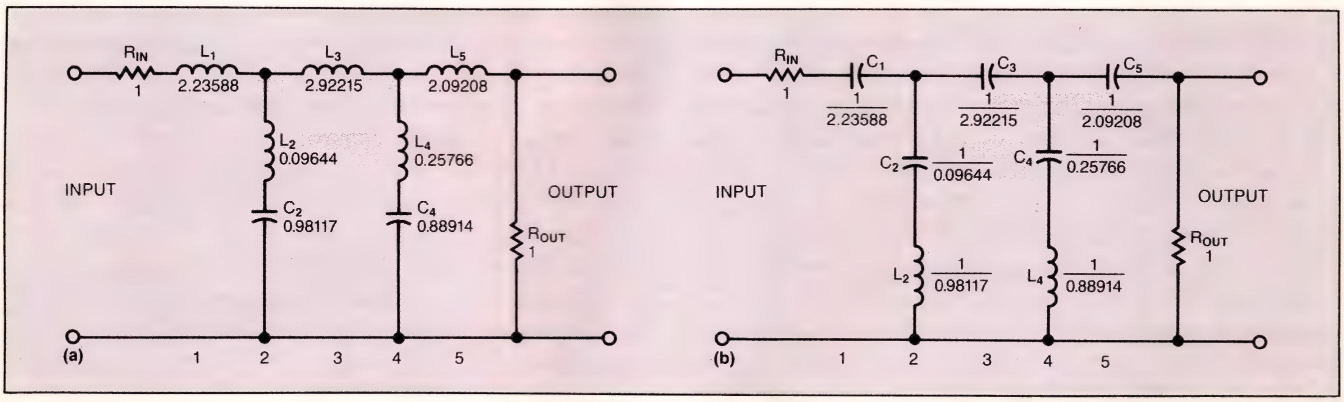

Fig 1—You can get normalized component values *for a lowpass filter* ***(a)*** *from standard-reference design tables. To transform the lowpass filter to a highpass one* ***(b),*** *change the capacitors to inductors and vice versa, and use reciprocal values.*

It's possible to significantly improve filter performance without resorting to expensive precision capacitors.

sign filters according to $Z_{IN} = Z_{OUT} = Z$. Textbooks and reference books on filter design usually indicate that the selection of Z is arbitrary and proceed to use a convenient value between 10k and 50k Ω. Be aware that you can select any values you like, but subsequent component values will be based on this selection. For now, use a circuit-impedance level of $Z = R = 10k\ \Omega$.

If $\Omega_0 = 2\pi fc = 6.283 \times 1200 = 7540$ rads/sec, and $R = 10.0k$, then using reciprocals to transform the lowpass configuration into a highpass configuration and scaling for frequency and circuit impedance, will yield

$$C_1 = \frac{1}{L_1 R \Omega_0} = \frac{1}{2.23588 \times 10{,}000 \times 7540}$$

	IDEAL VALUE	USE
	$= 0.00593\ \mu F$	$0.0056\ \mu F$

Similarly,

	IDEAL VALUE	USE
$C_{2C} = 1/L_2)\ (R)\ (\Omega 0)$	$= 0.13753\ \mu F$	$0.15\ \mu F$
$C_{2L} = 1/(C_2)\ (R)\ (\Omega 0)$	$= 0.01352\ \mu F$	$0.015\ \mu F$
$C_3 = 1/(L_3)\ (R)\ (\Omega 0)$	$= 0.00454\ \mu F$	$0.0047\ \mu F$
$C_{4C} = 1/(L_4)\ (R)\ (\Omega 0)$	$= 0.05147\ \mu F$	$0.047\ \mu F$
$C_{4L} = 1/(C_4)\ (R)\ (\Omega 0)$	$= 0.01492\ \mu F$	$0.015\ \mu F$
$C_5 = 1/(L_5)\ (R)\ (\Omega 0)$	$= 0.00634\ \mu F$	$0.0068\ \mu F$

The filter topology of choice for this example appears in **Fig 2.** (Other types would work just as well, however.) **Fig 2** shows the transformed, active highpass filter values. The actual active filter consists of amplifiers IC_1 through IC_4 and associated components. Because the circuit uses equal resistor values for R_{IN} (R_1) and R_{OUT} (R_{10}), the filter introduces a 6-dB loss. Noninverting amplifier IC_5, together with R_{11} and R_{12}, yield a stage gain of 2 to restore the overall circuit gain to unity. (For more details on the use of this filter topology, consult **Ref 3.**)

Fig 3a shows the computed frequency response of the filter (using the ideal values) vs the measured response (using standard components and setting $R = 10.0k\ \Omega$. The use of standard-value components rather than ideal values noticeably degrades the performance. The performance of a production unit may be even poorer when you consider worst-case tolerance buildup.

The degree to which the realized response deviates from the ideal will vary, however. Contributing factors

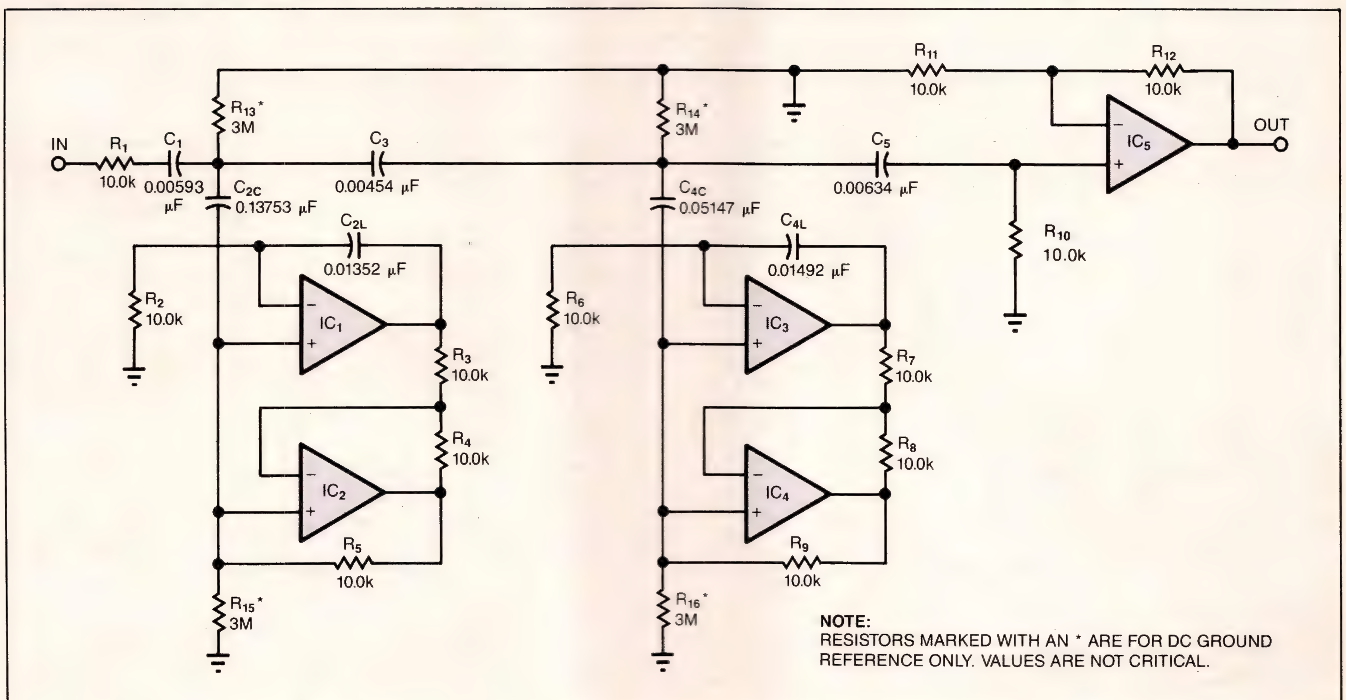

***Fig 2—This 1-kHz active highpass filter** uses ideal component values computed for 10k-Ω input and output impedances.*

TABLE 2—PARTIAL OUTPUT OF LISTING 1

Freq. = 1200 DIFFERENCE = 5 %

R	C1	C2C	C2L	C3	C4C	C4L	C5	SCORE
10000	0.00593	0.13753	0.01352	0.00454	0.05147	0.01492	0.00634	0001010
10200	0.00582	0.13483	0.01325	0.00445	0.05047	0.01462	0.00622	1000010
10500	0.00565	0.13098	0.01287	0.00432	0.04902	0.01421	0.00604	1000100
10700	0.00554	0.12853	0.01263	0.00424	0.04811	0.01394	0.00592	1000100
11000	0.00539	0.12502	0.01229	0.00413	0.04679	0.01356	0.00576	1110101
11300	0.00525	0.12170	0.01196	0.00402	0.04555	0.01320	0.00561	0111101
11500	0.00516	0.11959	0.01175	0.00395	0.04476	0.01297	0.00551	0111101
11800	0.00503	0.11655	0.01146	0.00385	0.04362	0.01264	0.00537	0111001
12100	0.00490	0.11366	0.01117	0.00375	0.04254	0.01233	0.00524	1001010
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25500	0.00233	0.05393	0.00530	0.00178	0.02019	0.00585	0.00249	0101010
26100	0.00227	0.05269	0.00518	0.00174	0.01972	0.00572	0.00243	1001010
26700	0.00222	0.05151	0.00506	0.00170	0.01928	0.00559	0.00237	1000010
27400	0.00216	0.05019	0.00493	0.00166	0.01879	0.00544	0.00231	1010110
28000	0.00212	0.04912	0.00483	0.00162	0.01838	0.00533	0.00226	1110111
28700	0.00207	0.04792	0.00471	0.00158	0.01794	0.00520	0.00221	0110101
29400	0.00202	0.04678	0.00460	0.00154	0.01751	0.00507	0.00216	0111101
30100	0.00197	0.04569	0.00449	0.00151	0.01710	0.00496	0.00211	0111101
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41200	0.00144	0.03338	0.00328	0.00110	0.01249	0.00362	0.00154	1110101
42200	0.00141	0.03259	0.00320	0.00108	0.01220	0.00353	0.00150	0110101
43200	0.00137	0.03183	0.00313	0.00105	0.01192	0.00345	0.00147	0100111
44200	0.00134	0.03111	0.00306	0.00103	0.01165	0.00337	0.00143	0001111
45300	0.00131	0.03036	0.00298	0.00100	0.01136	0.00329	0.00140	0001010
46400	0.00128	0.02964	0.00291	0.00098	0.01109	0.00321	0.00137	0001010
47500	0.00125	0.02895	0.00285	0.00096	0.01084	0.00314	0.00133	1001010

are the complexity of the filter, the sensitivity of the component ratios, and how closely the real component values approximate the ideal ones. Because your application will usually govern the first two factors, the third factor (often overlooked) offers an easy means of improving performance.

You can optimize the design

You don't have to resort to precision capacitors or trimmed components. Instead, calculate the denormalized component values required for various values of R, and then provide a means of judging the best combinations. Although the task of testing successive R values on a calculator is error-prone and tedious, it becomes simple and convenient if you make your personal computer do it for you.

To optimize the filter in the previous example, return to the normalized component values you obtained from **Table 1.** Enter those values into lines 250 through 310 of **Listing 1.** The program also requires the cutoff frequency (f_C) or the center frequency (f_0) if you are optimizing a bandpass filter.

The next step is to run the program. The program will print out a table (a portion of which appears as

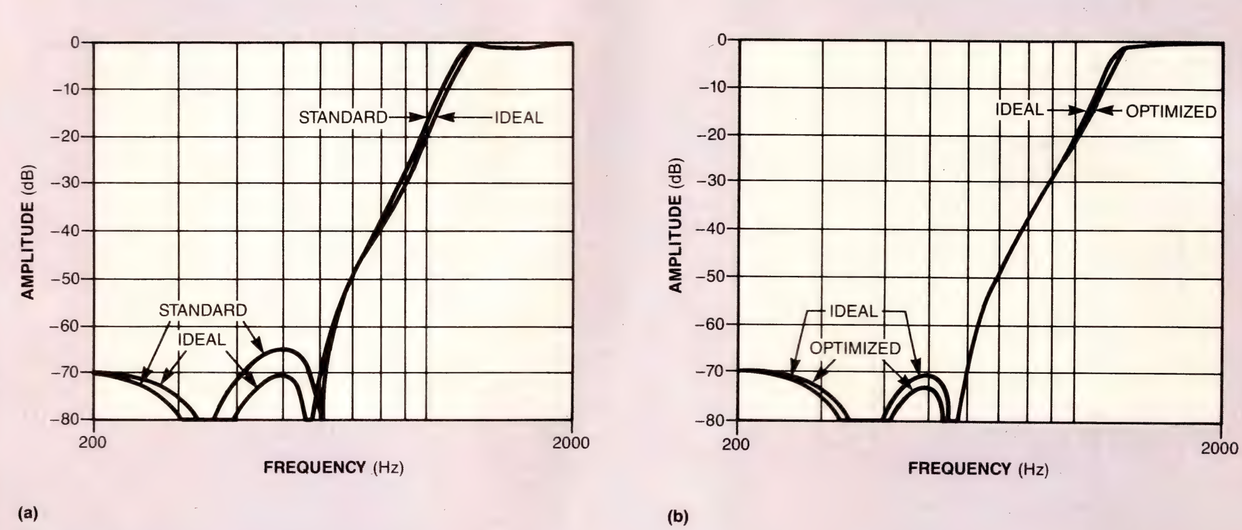


Fig 3—The use of unoptimized, standard-value components *degrades filter performance, especially in the stopband area* ***(a)****. Using the optimization technique, you can bring performance closer to that of a filter using the ideal values* ***(b)****.*

Table 2). The left-most column lists R values in 1% increments from 10.0k to 47.5k Ω. The next seven columns list the ideal capacitor values that correspond to the impedance (R) shown in the left-most column. The right-most column contains a "score"; this 7-bit binary number contains a 1 for each capacitor whose ideal value falls within a user-specified percentage (DIFFERENCE) of a standard 5% value. The bit positions correspond directly to the column position in the row—that is, the left-most bit refers to the C_1 value, and the right-most bit to the C_5 value. The more 1s in the score, the better the overall match and the closer the resulting filter will approach the ideal response.

As you examine **Table 2,** it becomes obvious that the initial choice of 10.0k Ω for R was not optimum. Only two of the seven capacitors required are within 5% of a standard 5%-tolerance part. However, for an R value of 28.0k Ω, six of the seven values fall within 5% of the standard-value parts. For the sample filter, this R value is the only one that yields such a high score. Quite often, however, you'll find that two or more R values have the same score at a DIFFERENCE value of 5%. In such cases, to determine which value is a better choice, reduce the value of DIFFERENCE (in line 360) and run the program again.

The program's sample output clearly indicates that the design should use an R value of 28.0k Ω. The program calculated the ideal capacitor values for each position; you should now use the closest standard-value parts, as follows:

IDEAL VALUE	USE
C_1=0.00212 μF	0.0022 μF 5%
C_{2C}=0.04912 μF	0.047 μF 5%
C_{2L}=0.00483 μF	0.0047 μF 5%
C_3=0.00162 μF	0.0015 μF 5%
C_{4C}=0.01838 μF	0.018 μF 5%
C_{4L}=0.00513 μF	0.0056 μF 5%
C_5=0.00226 μF	0.0022 μF 5%

The results of a circuit simulation, using a version of Spice, indicate that the optimized 28k-Ω filter design **(Fig 3b)** shows an improvement of only one- or two-tenths of a decibel over the standard 10k-Ω design **(Fig 3a)** in the passband area. However, an examination of the stopband area tells a different story. **Figs 4a** and **4b** show expanded views of the stopband areas of **Figs 3a** and **3b.** From **Fig 4a,** you'll see that the 10.0k-Ω design degrades the stopband performance by almost 6 dB compared with the ideal response. On the other hand, **Fig 4b** shows that the stopband performance of the 28.0k-Ω design is actually *better* than that of the ideal filter. The tradeoff is a slight increase in passband ripple. The inequality of the return lobes between the transmission zeros is primarily a result of C_3's value of 0.0015 μF. This standard value was furthest from the ideal value.

Because the use of this optimization technique is equivalent to fine-tuning a traditional design, the results are not always dramatic, but they are nonetheless real. The degree of improvement you achieve increases as the filter becomes more complex and performance

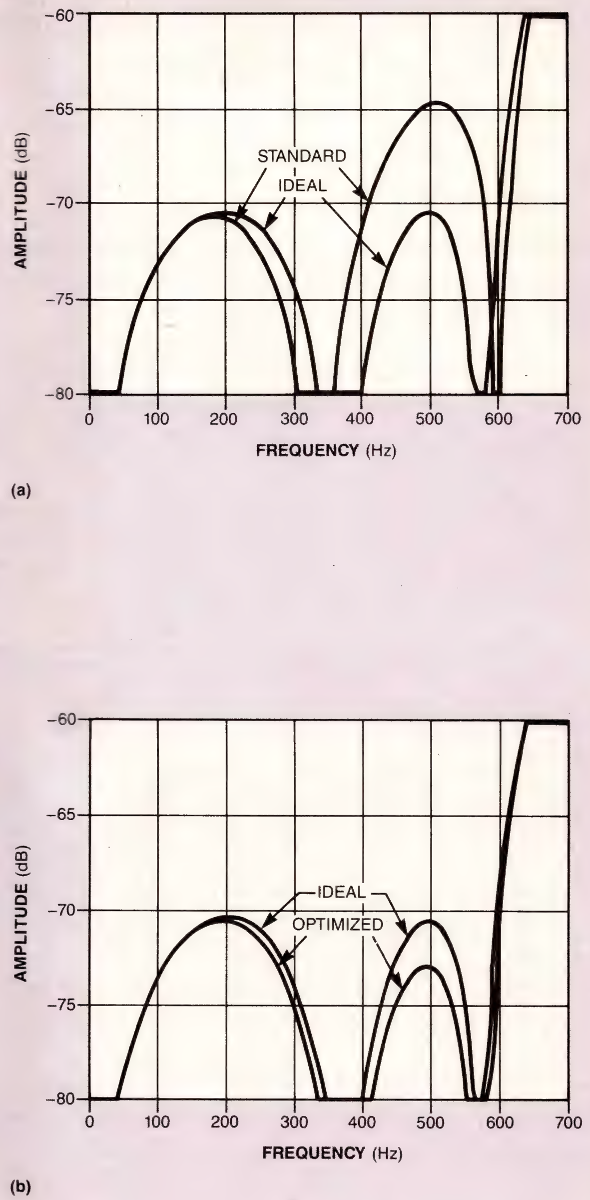


***Fig 4—These enlargements of** the stopband areas of **Fig 3** show that a filter with optimized component values performs better than one using ideal values.*

Selecting an appropriate filter-impedance value yields a set of standard-value components that preserves critical ratios.

requirements more stringent. For moderate circuits like the one in the example, stopband improvements in A_{MIN} of 3 to 6 dB are typical.

Perhaps the most significant improvement lies in the overall closer approach to the ideal design: You achieve a better balance of components, and therefore worst-case tolerance accumulation is less of a problem than if you arbitrarily select some convenient value for Z. You'll still have some decisions to make, and perhaps you'll still have to do some experimental simulation to confirm your choice. Suppose, for example, that the program offers you two sets of values. Do you select the one in which all the components differ slightly (and by the same proportion) from the ideal values, or do you choose the one that gives you six very closely matched values and a seventh that is way off?

The choice of certain component values in filter design is not as arbitrary as you've been led to believe. Although this statement is true when applied to all filter topologies, the approach described here seems most effective in terms of active highpass-filter design, where you must first select the circuit-impedance level upon which capacitor values are dependent. You'll find the most noticeable improvement in applications that

Optimization program is pliable

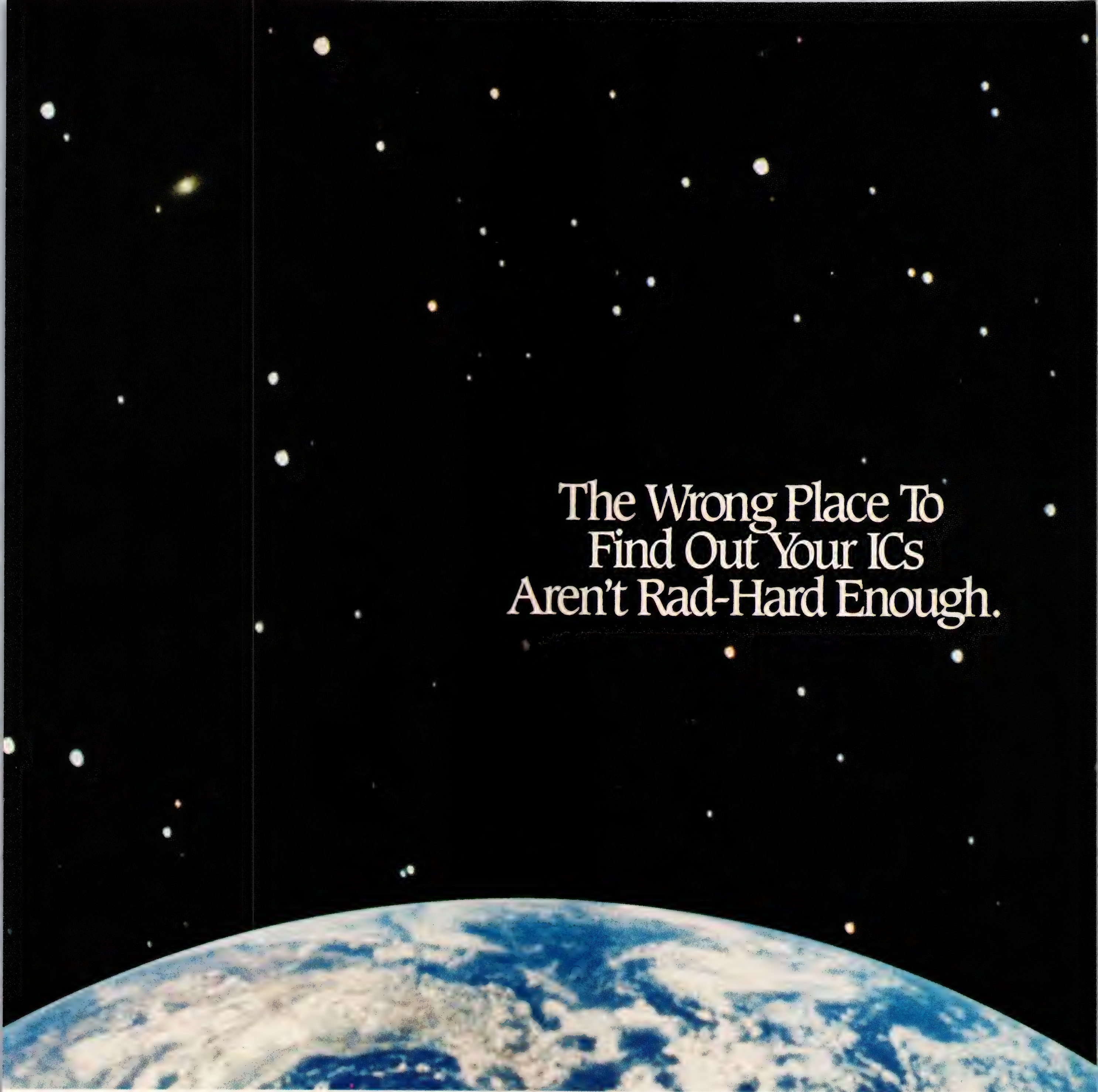
The optimization program around which the accompanying article is based contains extensive comments, but further elaboration may help you to modify it according to your needs. Theoretically, you could add INPUT statements to accept the values that the program needs (lines 250 through 390), but because you probably won't be doing this type of filter optimization very often, you'll probably find it more efficient to modify the program each time you need it. If you do decide to gather data with INPUT statements, you should also add an INPUT statement before the END statement at line 935, asking if you want to perform another run or if you want to exit. Developing a general-purpose program that applies to a variety of filters would be possible, but would probably take more time than it's worth.

Lines 100 through 210 dimension and load the resistor array with the 1% standard-value increments between 10.0 and 47.5 that are contained in the DATA statements. If you expand the array to include a greater number of values, be sure to change the DIM statement in line 100 and the corresponding value of LASTVAL in line 390. However, it's unlikely that you'll find any particular advantage in using a wider range of resistor values; the existing range always presents several possibilities from which to select a practical circuit impedance, and higher R values merely increase the chances of making the design vulnerable to noise problems.

Lines 250 through 310 assign values to the passive filter components shown in **Fig 1.** Enter the normalized values that you obtain for your design from filter-design tables **(Refs 1, 2, 3,** or **Table 1**). Depending on the filter topology, you may need to use more or fewer component values; if so, you'll also have to modify lines 560 through 880 to reflect the change. Lines 360 through 390 contain run-time values that you may wish to change, depending on your filter application.

After line 430, insert an LPRINT statement that will generate any control codes that your printer requires to set type size and spacing. If you have more than seven component columns, these codes should set up your printer for condensed mode. Lines 460 through 480 print a header for the output table. Lines 520 through 670 calculate the ideal capacitor values required by the active-filter topology of **Fig 2,** and lines 760 through 880 print the SCORE column.

The first subroutine (lines 950 through 1150) scales the ideal capacitor value and then compares it in standard 5% increments to determine which is the nearest standard value. The routine returns a value (DIFF) that corresponds to the amount by which the ideal value differs from a standard 5% capacitor increment. The subroutine at line 1190 prints the SCORE bit for the component; the bit is a 1 if the value of DIFF is equal to or less than the user-defined variable DIFFERENCE, and a 0 if DIFF is greater than DIFFERENCE.



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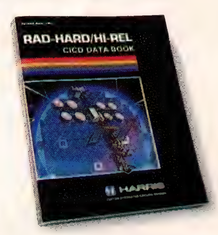

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CIRCLE NO 228

The choice of certain component values in filter design is not as arbitrary as some textbooks would lead you to believe. Better balance leads to better performance.

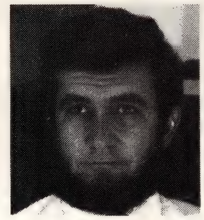
require high Q, low passband ripple, or multipole elliptic topologies, but for which cost constraints forbid the use of 1% or 2% capacitors.

It's worthwhile taking the time to experiment with this approach. The program of **Listing 1** is simple and straightforward (see **box,** "Optimization program is pliable"). Once you understand the concept, you can easily adapt the program to your particular design. **EDN**

References

1. Zverev, Anatol I, *Handbook of Filter Synthesis*, John Wiley and Sons, NY, NY, 1967.
2. Williams, Arthur B, *Electronic Filter Design Handbook*, McGraw-Hill Book Co, NY, NY, 1981.
3. Delagrange, Arthur D, "Design active elliptic filters with a 4-function calculator," *EDN*, March 3, 1982, pg 135.

Author's biography



Brent F Balch is a principal engineer with Sensormatic Electronics Corp in Deerfield Beach, FL, where he is responsible for the design and development of magnetic-field-disturbance sensor systems for protecting retailers against shoplifters. Brent holds a BS in neurophysiology from Florida Atlantic University. He's an avid reader, but also enjoys racquetball, backpacking, and fishing.

Article Interest Quotient (Circle One)
High 491 Medium 492 Low 493

LISTING 1

```
10 'Program: VALUES.BAS        2-14-88          Rev: 3
20 'This program lists the exact capacitor values required
30 'in a 5-pole, 4-zero elliptic HP filter for various
40 'impedance levels.  Also indicates which capacitor values
50 'are within a user-specified percentage of the nearest
60 'standard value part.
70 '
90 '        DIMension array variables.
100 DIM RES(66)
120 '       Read 1% resistor increments into RES array.
125 '       (There are 66 1% values between 10K and 47.5K)
130 FOR I = 1 TO 66: READ RES(I): NEXT
140 '
150 DATA 10.0,10.2,10.5,10.7,11.0,11.3,11.5,11.8,12.1,12.4
160 DATA 12.7,13.0,13.3,13.7,14.0,14.3,14.7,15.0,15.4,15.8
170 DATA 16.0,16.5,16.9,17.4,17.8,18.2,18.7,19.1,19.5,20.0
180 DATA 20.5,21.0,21.5,22.1,22.6,23.2,23.7,24.3,24.9,25.5
190 DATA 26.1,26.7,27.4,28.0,28.7,29.4,30.1,30.9,31.6,32.4
200 DATA 33.2,34.0,34.8,35.7,36.5,37.4,38.3,39.2,40.2,41.2
210 DATA 42.2,43.2,44.2,45.3,46.4,47.5
220 '
240 'These are the IDEAL normalized table values:
250 L1 = 2.23588
260 L2 = .09644
270 C2 = .98117
280 L3 = 2.92215
290 L4 = .25766
300 C4 = .88914
310 L5 = 2.09208
320 '
340 ' These are the literal variables the user may want to change:
360 DIFFERENCE          = .05              ' Max deviation from ideal value allowed
370 FC                  = 1200             ' 3dB frequency for filter
385 KOHMS               = 1000             ' Scale factor for Res[]
390 LASTVAL             = 66               ' There are 66 choices for Res[]
395 '
410 OMEGA = 2 * 3.1415926# * FC
420 '
430 ' Output header to printer.
```

Listing continued on page 286

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LISTING 1 *(Continued)*

```
435 ' This is the point to insert appropriate control codes to set your
440 ' particular printer into condensed mode if your filter requires more
445 ' than seven values.  The header information in line 470 should also be
450 ' modified as required.
455 LPRINT
460 LPRINT "Freq. = ";FC;                           ' List the cutoff frequency
465 LPRINT "      DIFFERENCE = ";DIFFERENCE * 100;"%";  ' List DIFFERENCE
467 LPRINT
470 LPRINT"   R        C1        C2C        C2L        C3        C4C        C4L        C5"
475 LPRINT"        SCORE"
480 LPRINT"________________________________________________________________________________"
485 LPRINT"______________"
490 '
500 '======================== MAIN PROGRAM ================================
520 FOR I = 1 TO LASTVAL
530   IF I = 55 THEN LPRINT CHR$(12)              ' Advance to next page
540   R = RES[I] * KOHMS
560 ' Calculate optimum real values, scaled for impedance and frequency
570 C1  = 1000000!/(L1 * R * OMEGA)
580 C2C = 1000000!/(L2 * R * OMEGA)
590 C2L = 1000000!/(C2 * R * OMEGA)
600 C3  = 1000000!/(L3 * R * OMEGA)
610 C4C = 1000000!/(L4 * R * OMEGA)
620 C4L = 1000000!/(C4 * R * OMEGA)
630 C5  = 1000000!/(L5 * R * OMEGA)
640 '
650 ' Print out the table of IDEAL cap values
660 LPRINT R;" ";
665 LPRINT USING "#.#####  ";C1;C2C;C2L;C3;C4C;C4L;C5;
670 LPRINT "  ";
680 '
700 ' The following section prints a column indicating whether the ideal values
710 ' fall within an allowable error ('DIFFERENCE') of a standard value
720 ' capacitor.  If several circuit impedance levels result in equal "scores,"
730 ' then reducing the value of 'DIFFERENCE' and running the program again
740 ' will zero in on the optimum circuit impedance level.
750 '
760 TEMPVAL = C1  : GOSUB 950: GOSUB 1190
780 TEMPVAL = C2C : GOSUB 950: GOSUB 1190
800 TEMPVAL = C2L : GOSUB 950: GOSUB 1190
820 TEMPVAL = C3  : GOSUB 950: GOSUB 1190
840 TEMPVAL = C4C : GOSUB 950: GOSUB 1190
860 TEMPVAL = C4L : GOSUB 950: GOSUB 1190
880 TEMPVAL = C5  : GOSUB 950: GOSUB 1190
900 '
910 LPRINT
920 NEXT I
930 LPRINT CHR$(12)                              'Eject table from printer
935 END
937 '
940 '======================== SUBROUTINES ===================================
950 ' Determine which standard value 5% cap is nearest the desired ideal value.
960 '
970 ' Scale ideal capacitor values to the decade 0.1 - 1.0 for comparison.
990 IF TEMPVAL < 9.000001E-02 THEN TEMPVAL = TEMPVAL * 10: GOTO 990
1000 DIFF = 0
1030 IF ABS(TEMPVAL-1!)<ABS(TEMPVAL-.82) THEN DIFF=(TEMPVAL-1!)/1!:    RETURN
1040 IF ABS(TEMPVAL-.82)<ABS(TEMPVAL-.68) THEN DIFF=(TEMPVAL-.82)/.82: RETURN
1050 IF ABS(TEMPVAL-.68)<ABS(TEMPVAL-.56) THEN DIFF=(TEMPVAL-.68)/.68: RETURN
1060 IF ABS(TEMPVAL-.56)<ABS(TEMPVAL-.47) THEN DIFF=(TEMPVAL-.56)/.56: RETURN
1070 IF ABS(TEMPVAL-.47)<ABS(TEMPVAL-.39) THEN DIFF=(TEMPVAL-.47)/.47: RETURN
1080 IF ABS(TEMPVAL-.39)<ABS(TEMPVAL-.33) THEN DIFF=(TEMPVAL-.39)/.39: RETURN
1090 IF ABS(TEMPVAL-.33)<ABS(TEMPVAL-.27) THEN DIFF=(TEMPVAL-.33)/.33: RETURN
1100 IF ABS(TEMPVAL-.27)<ABS(TEMPVAL-.22) THEN DIFF=(TEMPVAL-.27)/.27: RETURN
1110 IF ABS(TEMPVAL-.22)<ABS(TEMPVAL-.18) THEN DIFF=(TEMPVAL-.22)/.22: RETURN
1120 IF ABS(TEMPVAL-.18)<ABS(TEMPVAL-.15) THEN DIFF=(TEMPVAL-.18)/.18: RETURN
1130 IF ABS(TEMPVAL-.15)<ABS(TEMPVAL-.12) THEN DIFF=(TEMPVAL-.15)/.15: RETURN
1140 IF ABS(TEMPVAL-.12)<ABS(TEMPVAL-.1) THEN DIFF=(TEMPVAL-.12)/.12:  RETURN
1150 IF ABS(TEMPVAL-.1)<ABS(TEMPVAL-.08) THEN DIFF=(TEMPVAL-.1)/.1:    RETURN
1170 '
1180 'Show whether ideal value is within DIFFERENCE of a standard 5% cap value
1190 IF ABS(DIFF) <= DIFFERENCE THEN LPRINT "1"; ELSE LPRINT "0";
1200 RETURN
```

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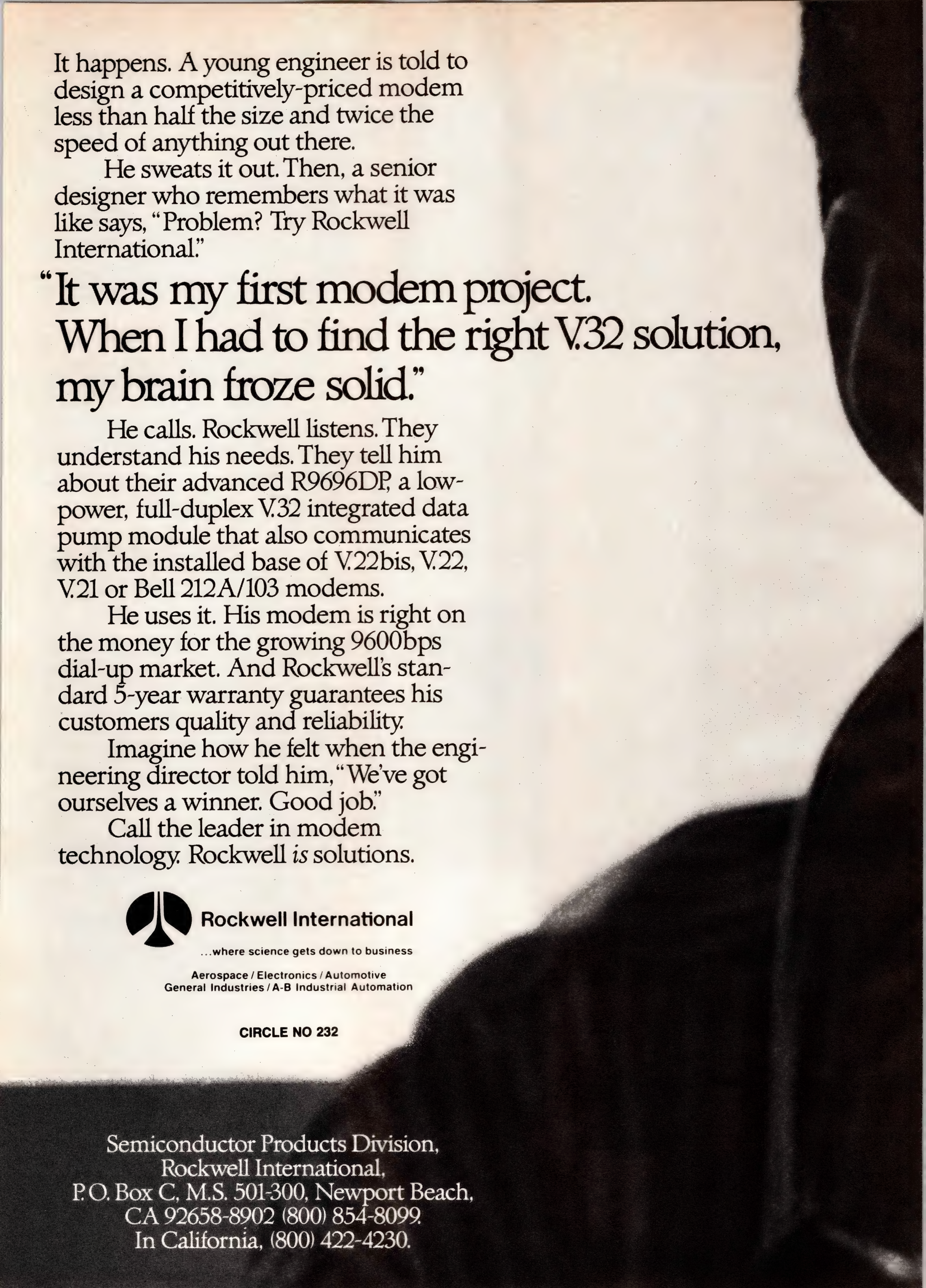
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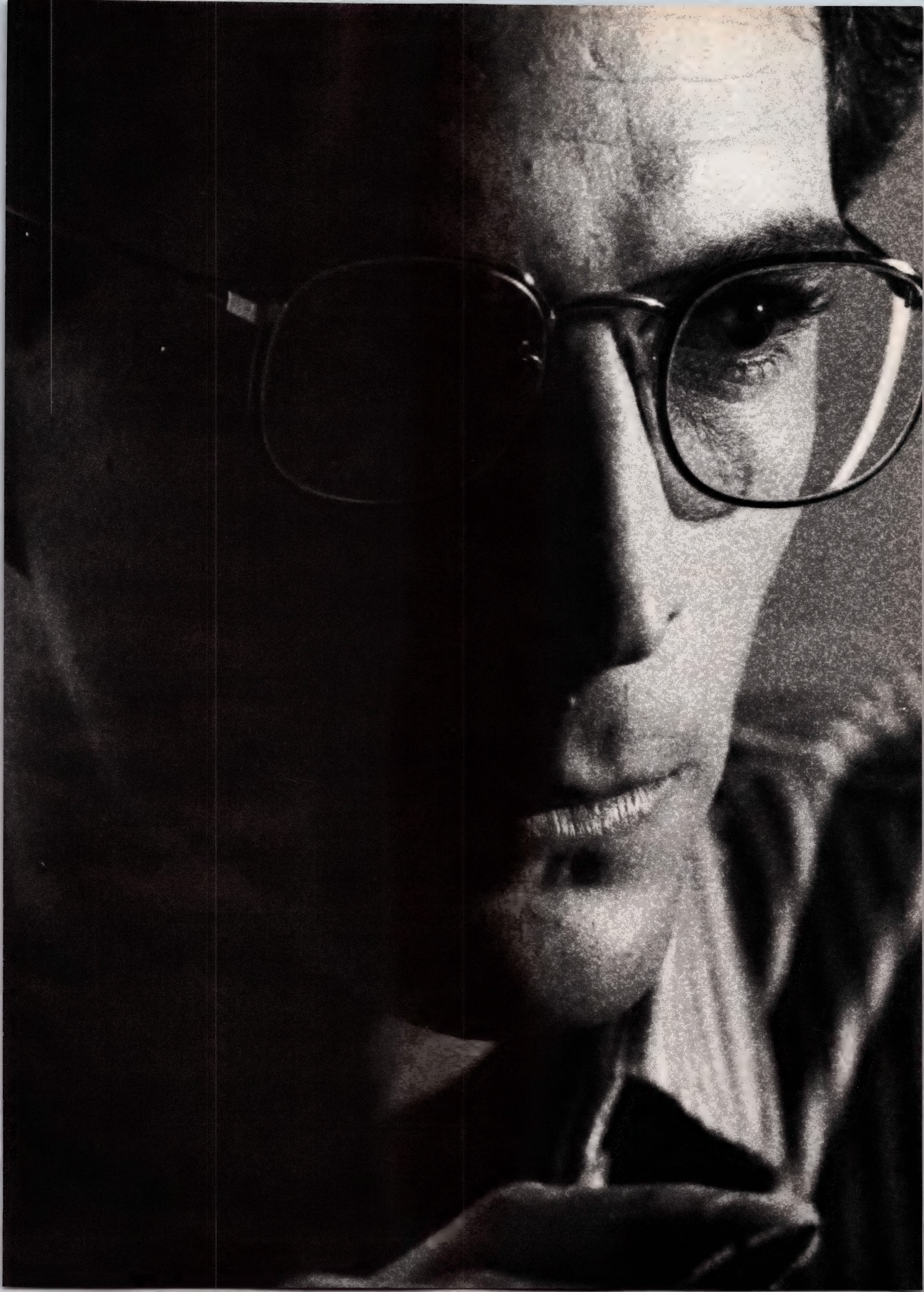

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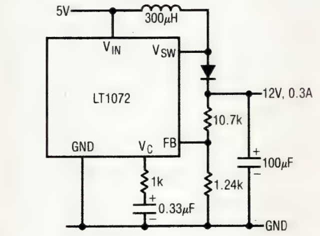

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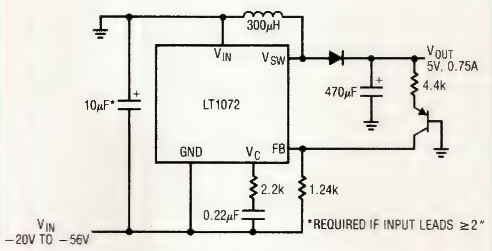

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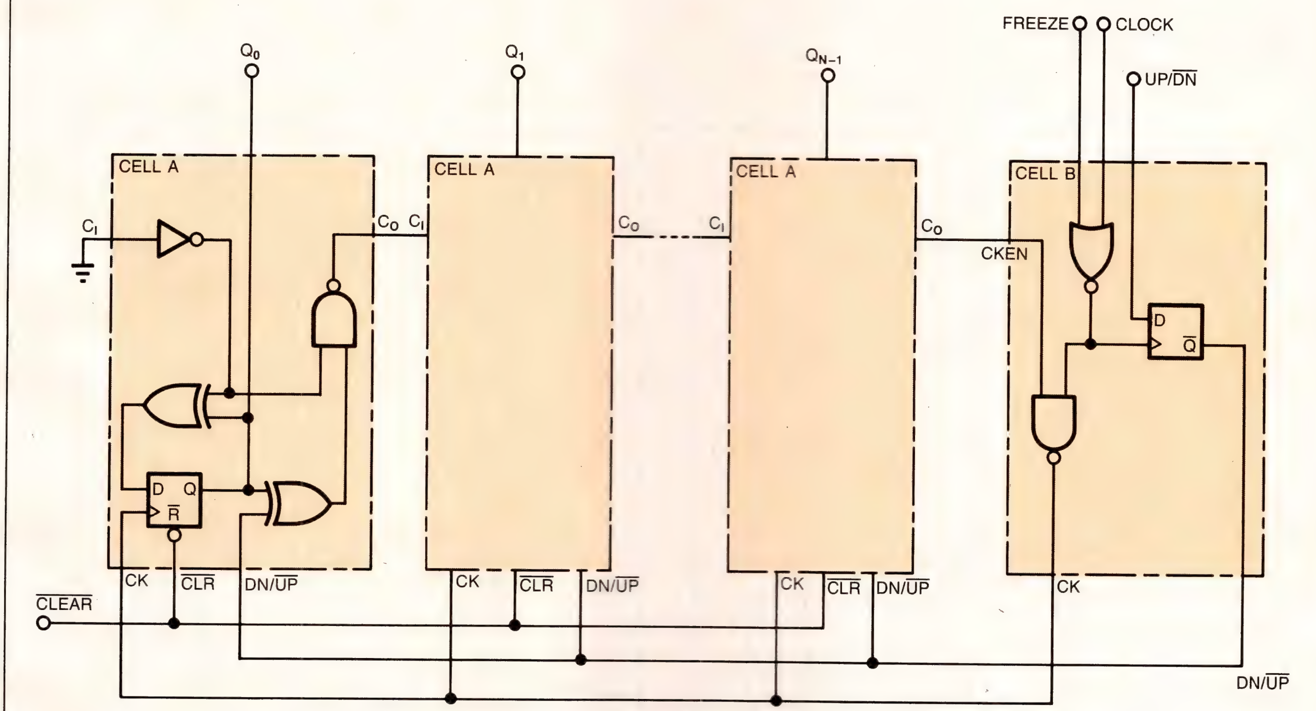
Up/down counter freezes at extreme counts

Sheng T Lin
Diasonics Inc, Milpitas, CA

The discrete-gate up/down-counter design in **Fig 1** has the unusual property of freezing—or saturating—when it reaches its lowest count in the down-count mode or its highest count in the count-up mode instead of rolling over and resetting as do most counters. This property proves especially useful in position-control systems where, for example, you wouldn't want a robot's arm to slowly move to full extension as the counter counts up and then have it suddenly slam back to its rest position as the counter resets to zero.

You can cascade as many of the A cells as you need because the counter's outputs are synchronous. The B cell accepts the carry bit from the most significant bit's A cell and provides the clock control that stops the counter. Make sure that the Freeze input to the B cell doesn't get asserted when the Clock input is low; otherwise, the counter may make an extra count. EDN

To Vote For This Design, Circle No 749



STATE TABLE

FREEZE	UP/DN	CLOCK	CURRENT STATE $Q_{N-1} \ldots Q_0$	NEXT STATE $Q_{N-1} \ldots Q_0$
L	H	↑	11...10	11...11
L	H	↑	11...11	11...11
L	L	↑	00...01	00...00
L	L	↑	00...00	00...00
H	X	X	Q_X	Q_X

***Fig 1—This expandable counter** will saturate at both its maximum and its minimum count.*

PLD implements interrupt controller

Stephen D Holle
Technology 80 Inc, Minneapolis, MN

The PLD program of **Listing 1** implements a simple multiple-interrupt controller and presents an alternative to the 8259 series of interrupt controllers. The design suits μP systems that must service multiple interrupt sources but whose μP has only a single interrupt input and doesn't permit vectored interrupts.

Referring to **Fig 1,** you will see that the PLD accepts five interrupts—the high-priority interrupt, HI, and EX_0, EX_1, EX_2, and EX_3. The PLD also has two interrupt-enable inputs: EN HI enables HI, and EN EX enables the lower-priority interrupts, $EX_{0\text{-}3}$. All the interrupt registers can activate the PLD's IRQ output to interrupt the μP. The μP uses the $\overline{\text{IOR}}$ and $\overline{\text{CS}}$ signals to enable the individual interrupt-output lines and to clear the interrupt registers. EDN

To Vote For This Design, Circle No 748

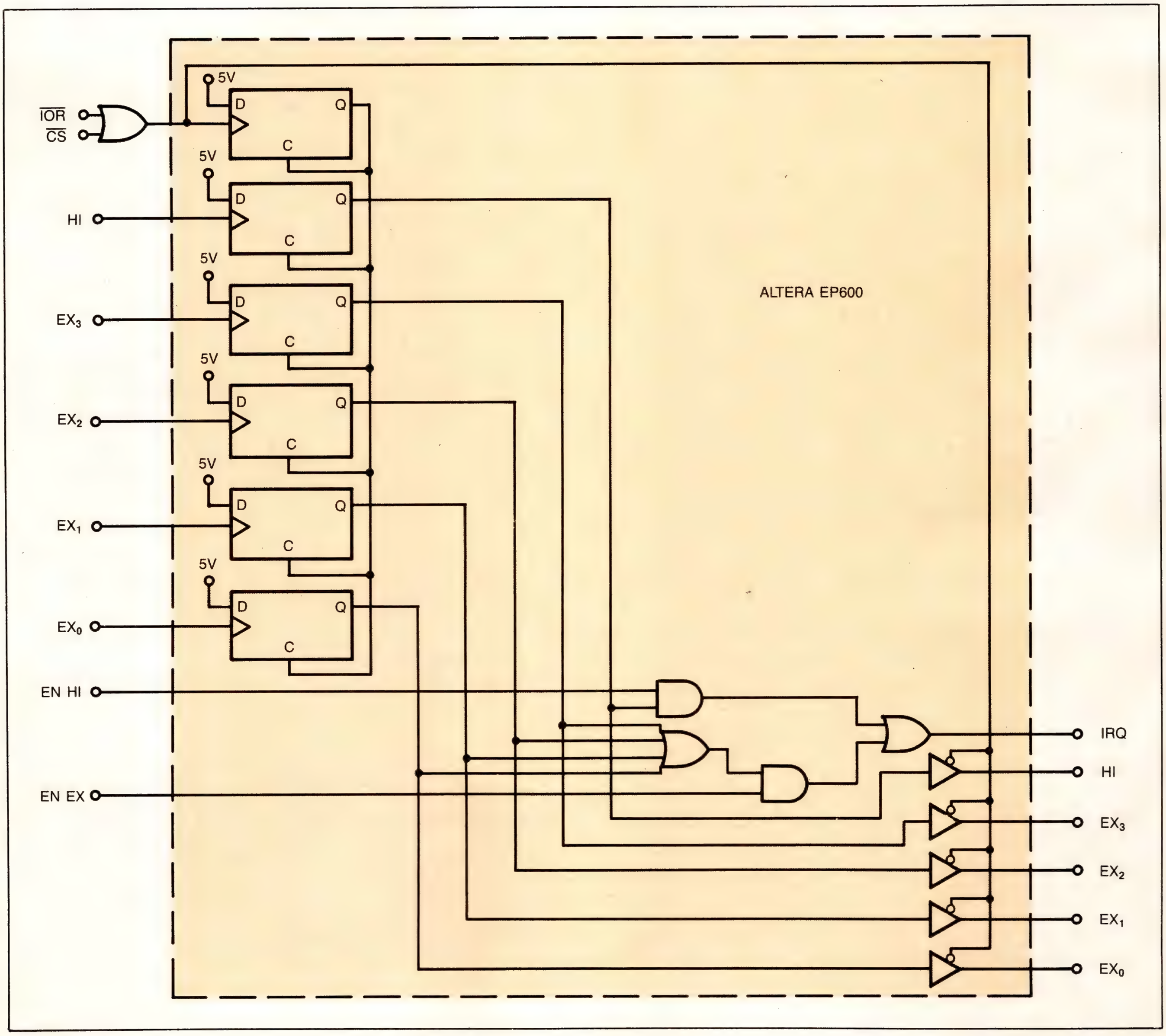


***Fig 1—This PLD provides** a simple alternative to 8259 interrupt controllers.*

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SPECIFICATIONS

Pin Model	**KSW-2-46**		**KSWA-2-46**	
Connector Version	**ZFSW-2-46**		**ZFSWA-2-46**	
FREQ. RANGE	dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (db)	typ	max	typ	max
dc-200MHz	0.9	1.1	0.8	1.1
200-1000MHz	1.0	1.3	0.9	1.3
1-4.6GHz	1.3	1.7	1.5	2.6
ISOLATION (dB)	typ	min	typ	min
dc-200MHz	60	50	60	50
200-1000MHz	45	40	50	40
1-4.6GHz	30	23	30	25
VSWR (typ) ON	1.3:1		1.3	
OFF	—		1.4	
SW. SPEED (nsec)				
rise or fall time	2(typ)		3(typ)	
MAX RF INPUT (bBm)				
up to 500MHz	+17		+17	
above 500MHz	+27		+27	
CONTROL VOLT.	-8V on, OV off		-8V on, OV off	
OPER/STOR TEMP.	-55° to +125°C		-55° to +125°C	
PRICE (10-24)	**$32.95**		**$48.95**	
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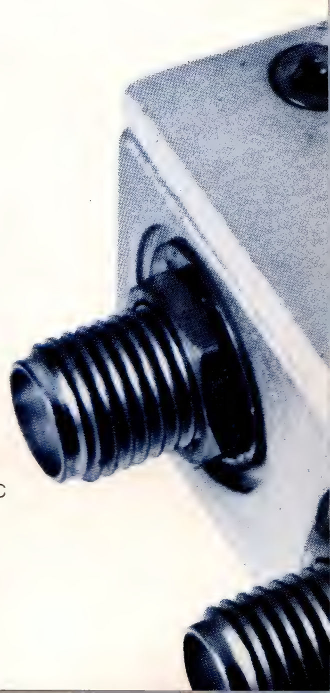

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CIRCLE NO 234

LISTING 1—PLD INTERRUPT CONTROLLER

```
/**  Inputs  **/

Pin 2       = ior_cs    ;      /* PC bus i/o read ORed with  !cs */
Pin 3       = ex3       ;      /* external interrupts            */
Pin 4       = ex2       ;      /*                                */
Pin 5       = ex1       ;      /*                                */
Pin 6       = ex0       ;      /*                                */
Pin 11      = hi_en     ;      /* enable for 1m628/629 interrupt */
Pin 14      = ex_en     ;      /* enable for external interrupts */
Pin 23      = hi        ;      /* 1m628/629 interrupt            */

/**  Outputs  **/

Pin 22      = d4        ;      /* status storage:                */
Pin 7       = d3        ;      /*    d4     = hi                 */
Pin 8       = d2        ;      /*    d3-d0 = ext4-1              */
Pin 9       = d1        ;      /*                                */
Pin 10      = d0        ;      /*                                */
Pin 21      = b4        ;      /* tri-state status outputs       */
Pin 20      = b3        ;      /*                                */
Pin 19      = b2        ;      /*                                */
Pin 18      = b1        ;      /*                                */
Pin 17      = b0        ;      /*                                */
Pin 16      = dr        ;      /* read/clear flip-flop           */
Pin 15      = irq       ;      /* interrupt request out          */

/** Declarations and Intermediate Variable Definitions **/

a = hi_en & d4;                /* gated hi interrupt             */
b = d3 # d2 # d1 # d0;         /* combined external interrupts   */
c = b & ex_en;                 /* gated combined external ints   */

/** Logic Equations **/

dr.d  = 'b'1;
dr.ck = ior_cs;                /* clear after read flip-flop     */
dr.ar = dr.dfb;

d4.d  = 'b'1;
d4.ck = hi;                    /* interrupt storage flip-flops   */
d4.ar = dr.dfb;

d3.d  = 'b'1;
d3.ck = ex3;
d3.ar = dr.dfb;

d2.d  = 'b'1;
d2.ck = ex2;
d2.ar = dr.dfb;

d1.d  = 'b'1;
d1.ck = ex1;
d1.ar = dr.dfb;

d0.d  = 'b'1;
d0.ck = ex0;
d0.ar = dr.dfb;

b4    = d4;                    /* tri-state status output        */
b4.oe = !ior_cs;

b3    = d3;
b3.oe = !ior_cs;

b2    = d2;
b2.oe = !ior_cs;

b1    = d1;
b1.oe = !ior_cs;

b0    = d0;
b0.oe = !ior_cs;

irq = a # c;                   /* interrupt request output       */
```

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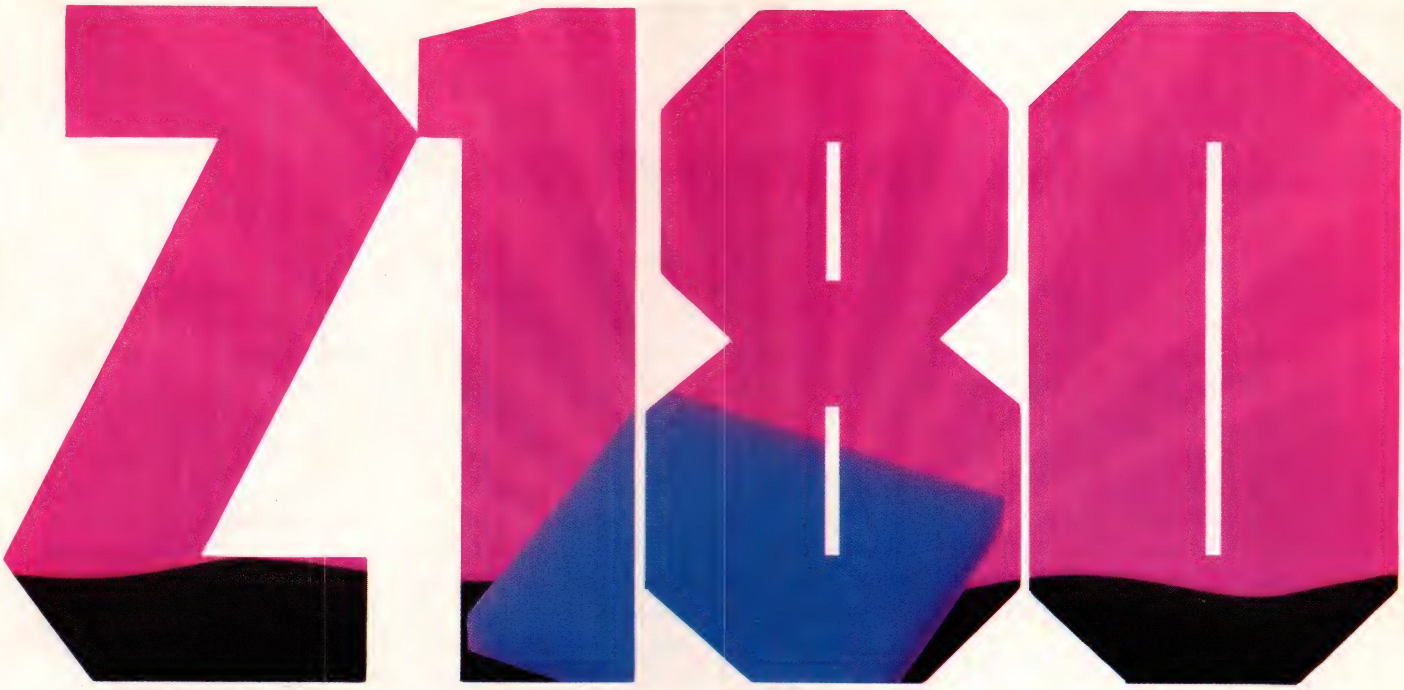

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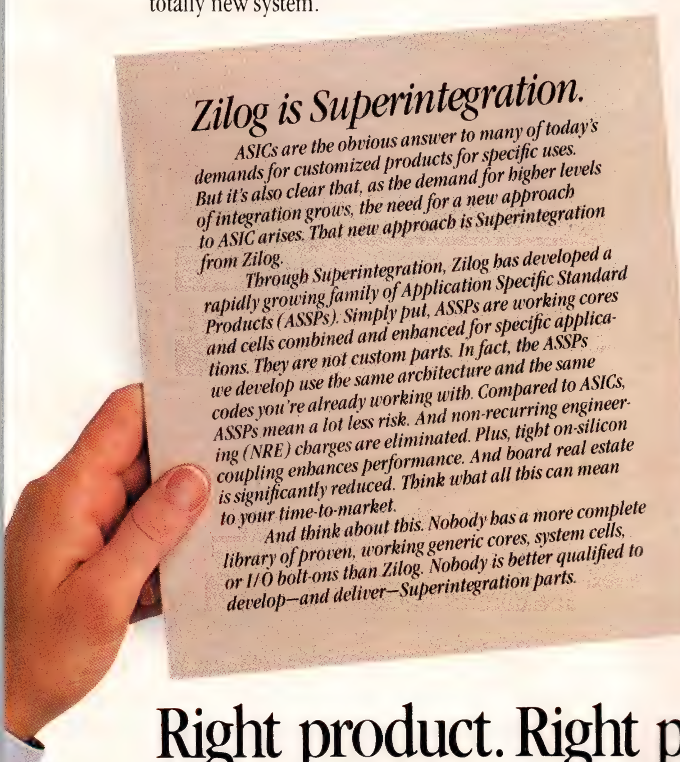

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Source follower linearizes photodiode

Joseph L Sousa
Hybrid Systems, Billerica, MA

A common method of transforming the output current of a photodiode into a voltage signal—paralleling the photodiode with a high-value load resistor (**Fig 1a**)—produces a nonlinear response. Also, the combination of the load's transresistance, R_T, and the photodiode's junction capacitance, C_J, slow the circuit's response time. **Fig 1b** shows virtually the same components as **Fig 1a** rearranged to maximize the inherent speed and linearity of the photodiode. The Hybrid Systems (Billerica, MA) SP4010 is a unity voltage-gain buffer with a JFET input, 60-MHz 3-dB bandwidth, and 18-bit (0.0004%) linearity over a ±10V input range.

In the circuit of **Fig 1b,** the photodiode sees a constant voltage across its terminals, which is essential for linear photodiode outputs. The optional zener diode, D_Z, sets a reverse bias at the photodiode for lower junction capacitance and higher speed (if you don't use D_Z, be sure to connect the feedback loop). An optional diode, D_{CLAMP}, limits the output in case of unexpected light bursts but results in increased dark-current leakage and lower speed. The buffered output of the circuit equals the photodiode current times the transresistance, R_T. **Fig 2** shows the circuit's response to a fast light pulse. EDN

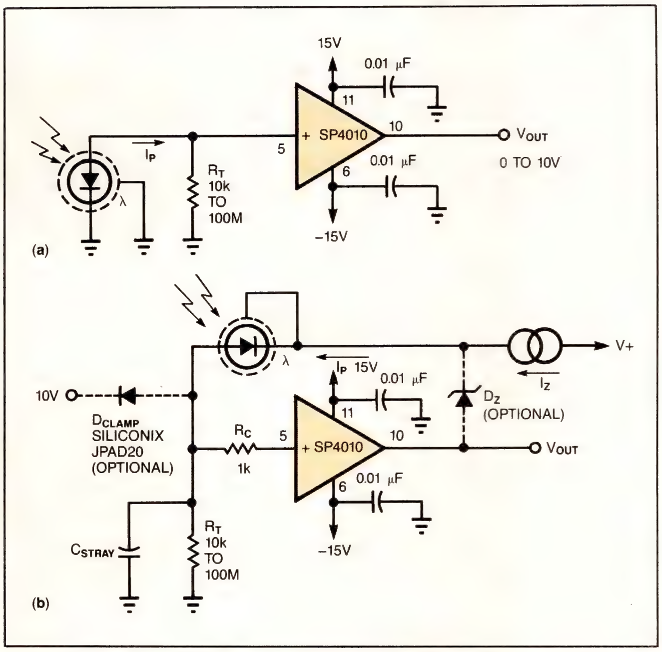

*Fig 1—**By rearranging the components in a,** the circuit in **b** improves the speed and linearity of the photodiode's response.*

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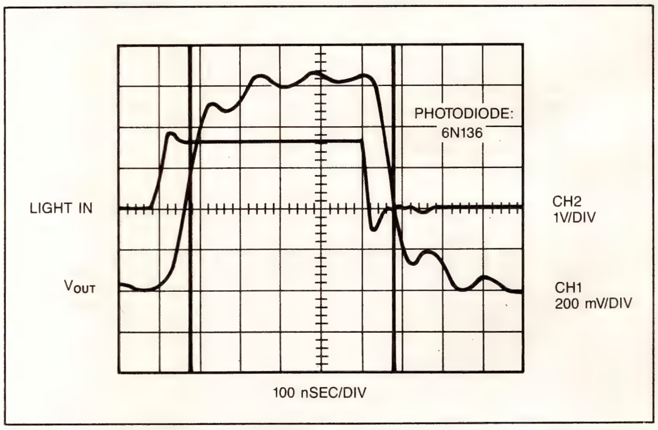

*Fig 2—**In Fig 1b's configuration,** the source-follower circuit provides a virtual short circuit at the photodiode to achieve high speed and 0.0004% linearity.*

Discrete-amplifier circuit sums signals

Michael Wyatt and R E Younski
Honeywell, Clearwater, FL

The simple discrete-amplifier design of **Fig 1** provides a high-speed summing node without resorting to an op amp. The circuit handles ±1V signals with less than 1% distortion, has a small-signal bandwith greater than 10 MHz, and consumes 13.7 mW. The measured output-signal swing is 6V p-p.

Transistor Q_1, operating as a common-base stage,

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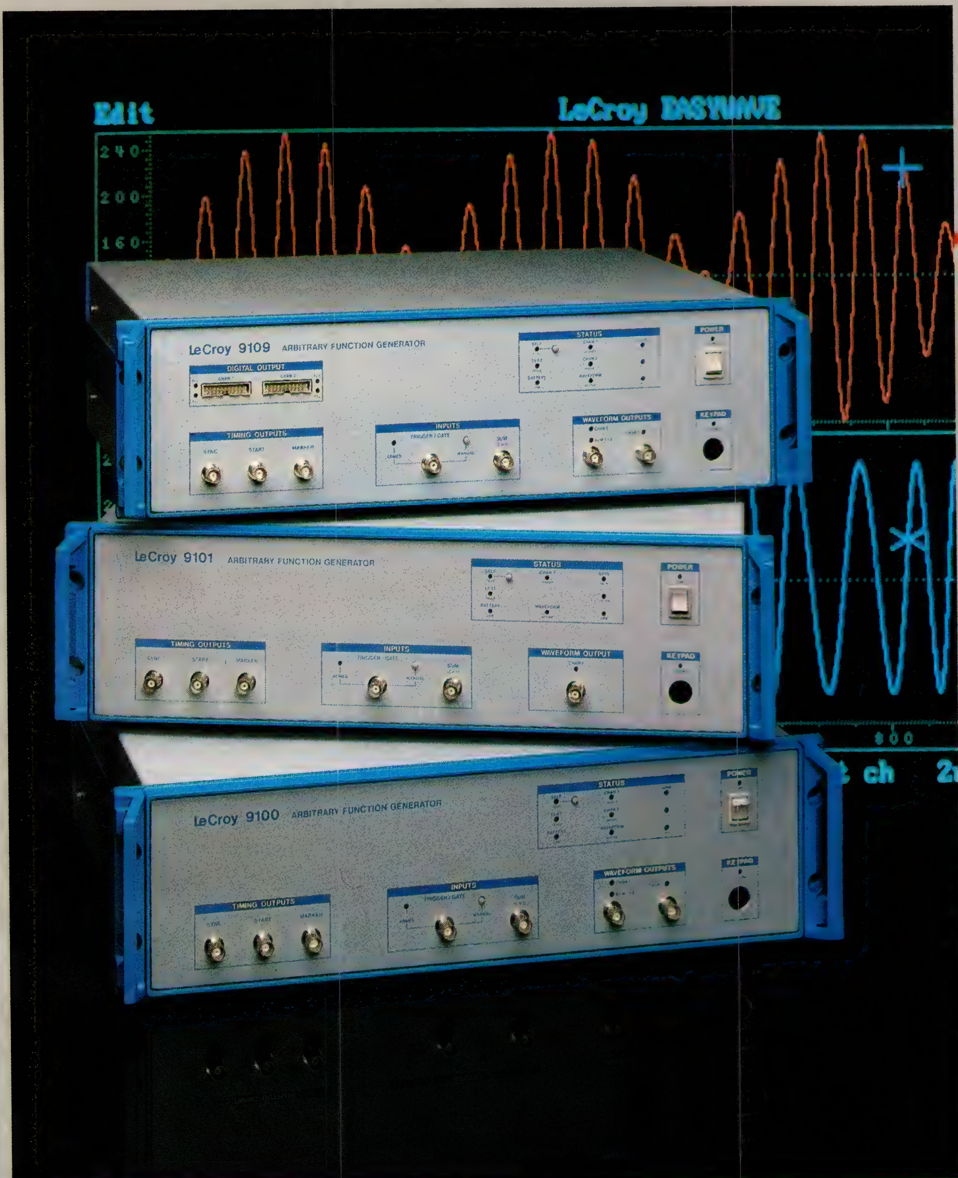

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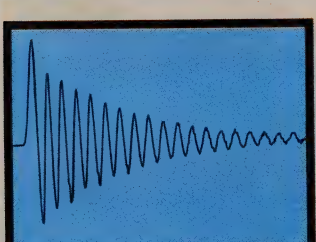
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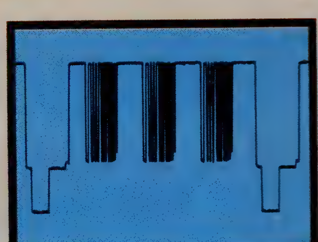
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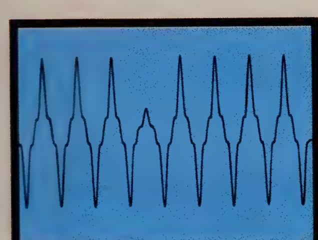
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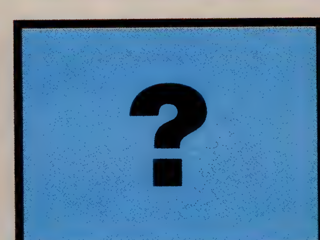
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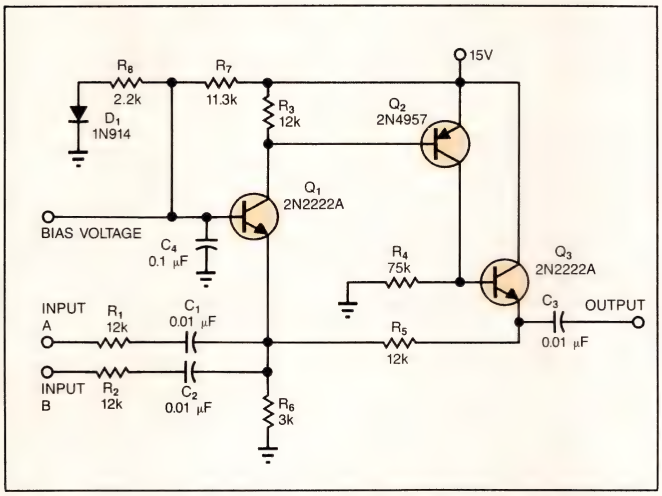

*Fig 1—**In contrast to designs** based on conventional op amps, this discrete summing-amplifier circuit doesn't suffer from a rapid fall-off in gain with increases in frequency.*

achieves low input impedance and wide bandwidth. Thanks to the low input impedance of the common-base configuration, Q_1's emitter appears as a virtual ac ground to both the input and the output signals without requiring the excessive negative feedback you would need with a conventional op amp.

Maintaining a near virtual ground at high frequencies is essential to ensure accurate summing. The open-loop gain of a conventional op amp falls off rapidly with increasing frequency. This fall-off restricts the effectiveness of the negative feedback. Limiting the feedback's effect will cause an op amp's virtual ground to increasingly deviate from true ground potential as frequency increases, thereby creating summing errors.

Q_2, a high-frequency pnp transistor, provides voltage gain and determines the high-frequency characteristics of the circuit. Because Miller capacitance limits the circuit's high-frequency gain, you should use a good-quality, high-frequency pnp device, such as a 2N4957, for Q_2. Q_3, an emitter follower, buffers Q_2 and supplies negative dc and ac feedback to Q_1 to maintain Q_1's operating point and to further reduce the virtual ac ground's impedance. You can substitute any general-purpose npn transitor for Q_1 or Q_3 because Q_2's pole dominates the circuit.

The summing gain is equal to $-R_5/R_1$ for input A and $-R_5/R_2$ for input B. You can add extra inputs as required. Resistors R_8 and R_7 and diode D_1 form a temperature-compensated dc-bias network that gives crude, but adequate, first-order compensation. The network causes Q_1 and Q_2 to operate with collector currents of 145 µA and causes Q_3 to operate with an emitter current of 620 µA. EDN

To Vote For This Design, Circle No 747

Pulse generator boasts very low duty cycle

Alex Ureche
Coopervision Surgical, Irvine, CA

Using a precision oscillator and a few CMOS counters, you can build a precise, very low duty-cycle pulse generator. You can add as many counters as you desire to make the period as long as you wish. The circuit in **Fig 1** will generate a pulse about 5 msec long every 24 hours—a 5.9^{-6}% duty cycle. EDN

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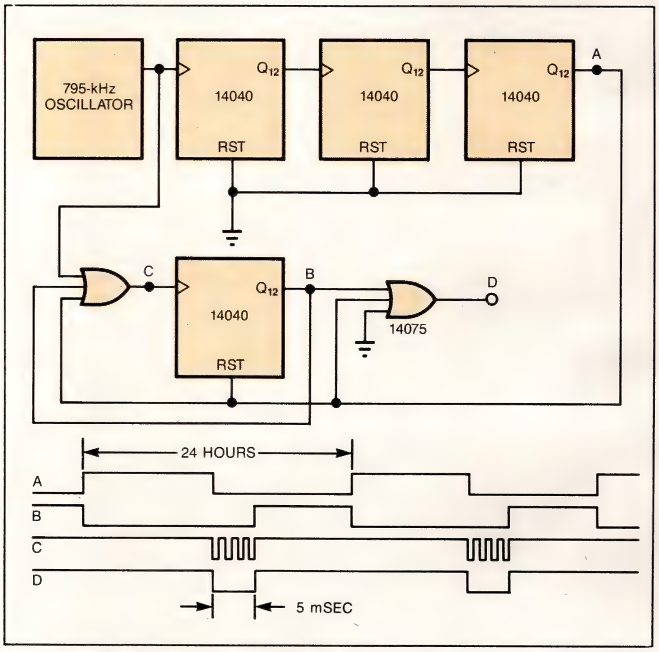

*Fig 1—**This low-duty-cycle pulse generator** produces one 5-msec pulse every 24 hours.*

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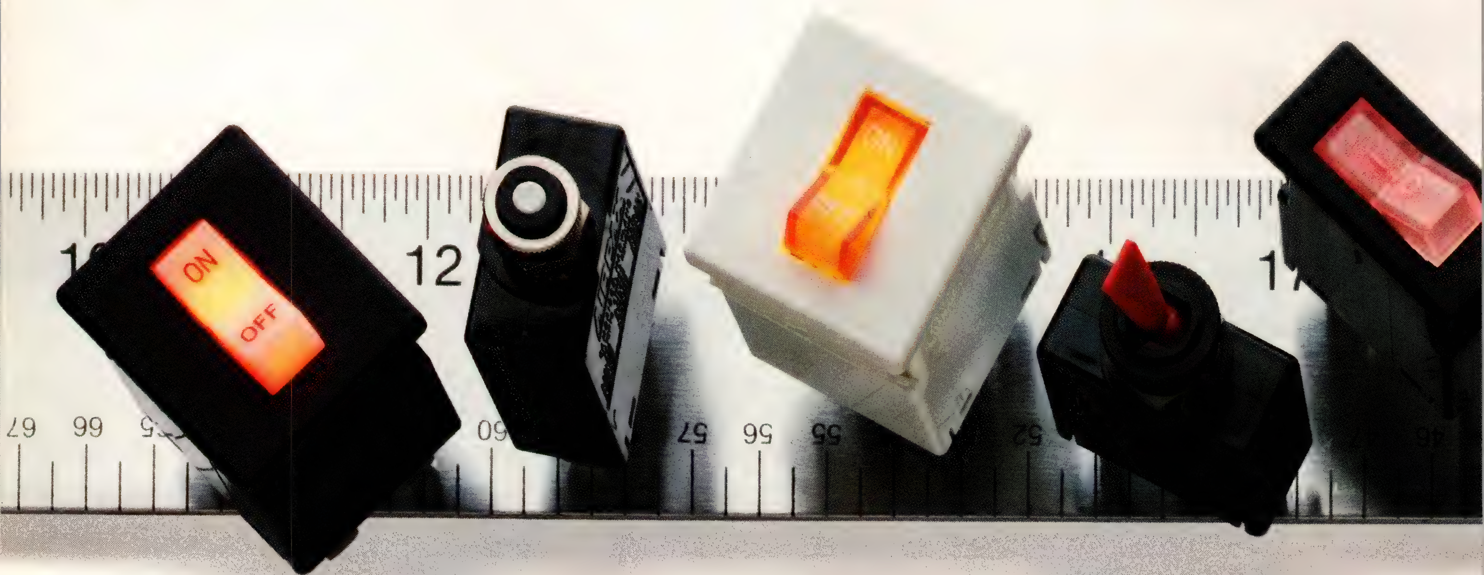

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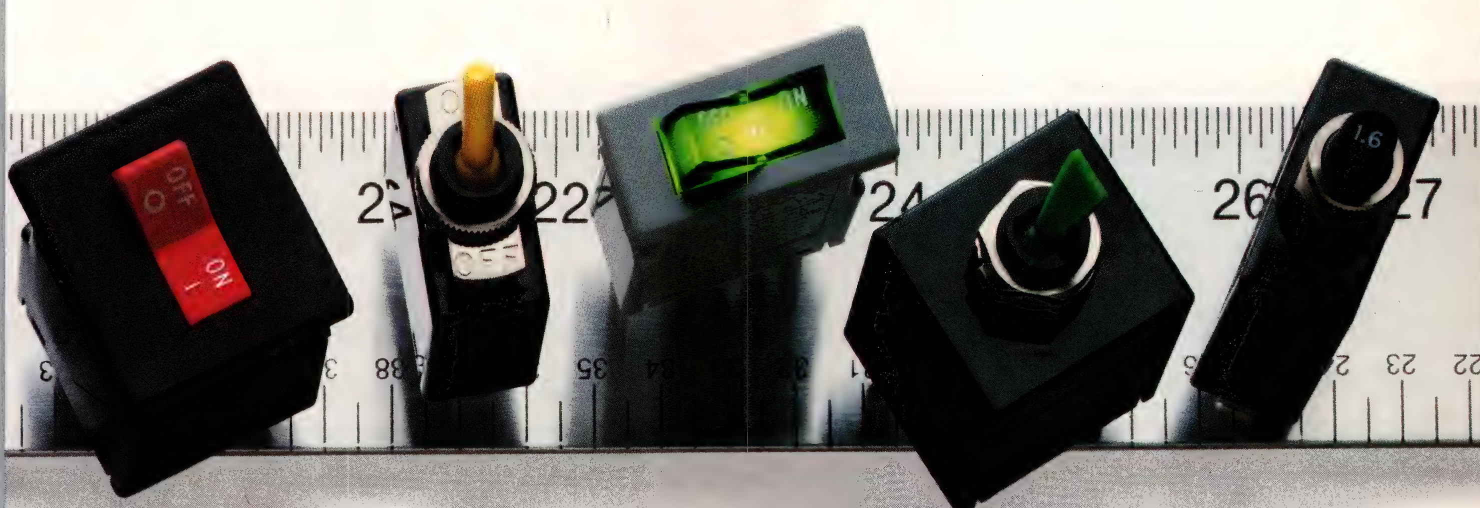

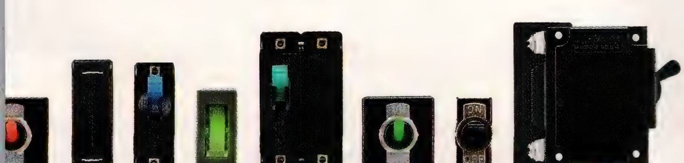

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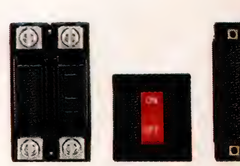

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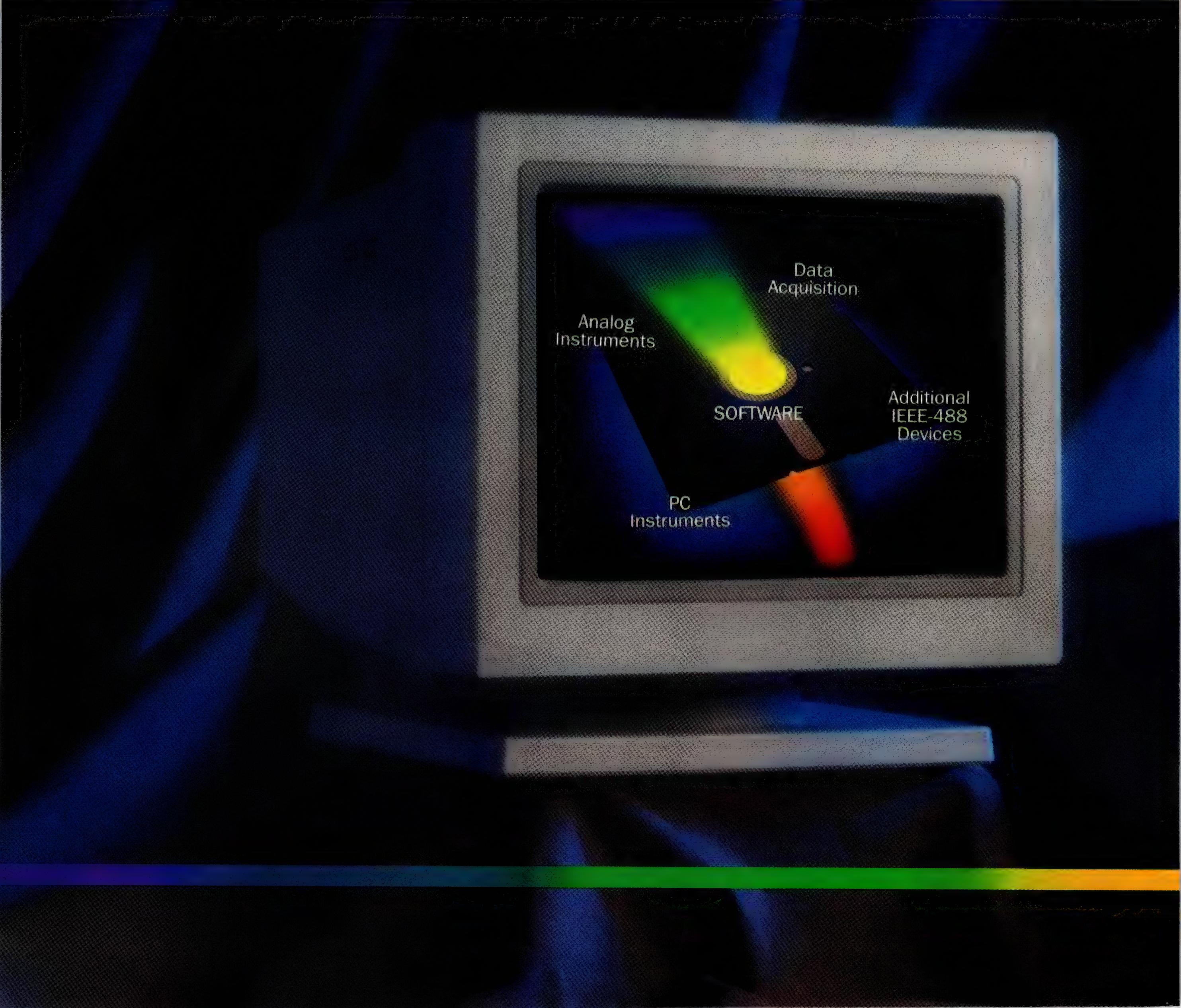

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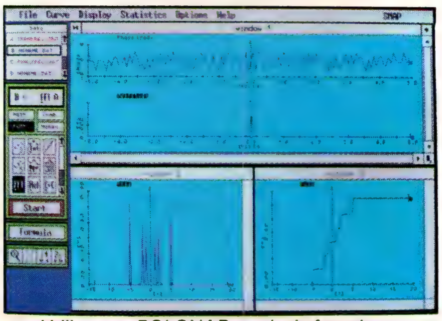

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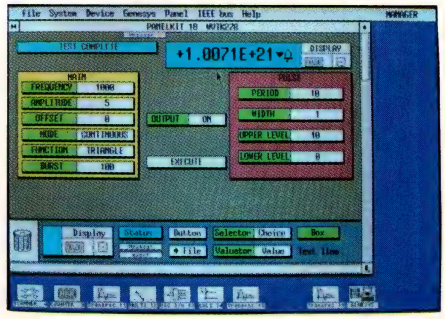

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- Robotics
- Machine Tool
- Imaging Systems
- Calibration Equipment
- Surveying Equipment

Very high resolution laser rotary encoders

MODEL	RESOLUTION (ppr)	MAXIMUM FREQUENCY RESPONSE (KHz)	MAXIMUM ANGULAR VELOCITY (rps)	SIGNAL OUTPUT			SIZE (mm x mm)
				Analog or Digital	Output Circuit	Absolute or Incremental	
K-1*	81,000	500	6.2 (372 rpm)	Analog	Op Amp + Serial Resistor (1 Vp-p)	Incremental	36 x 48
R-10	81,000	500	6.2 (372 rpm)	Digital	Open Collector	Incremental	36 x 48
R-1L	81,000	500	6.2 (372 rpm)	Digital	Line Driver (Balanced)	Incremental	36 x 58
R-2A*	Incremental 65,536 (2^{16}) Absolute 256 (2^{8})	500	7.6 (456 rpm)	Analog	Op Amp + Serial Resistor (1 Vp-p)	Absolute	56 x 80
R-2L	Incremental 65,536 (2^{16}) Absolute 256 (2^{8})	500	7.6 (456 rpm)	Digital	Line Driver (Balanced)	Absolute	56 x 80
M-1	50,000	2,000	40 (2400 rpm)	Digital	Line Driver (Balanced)	Incremental	56 x 70

* CI 16-1 (16x output pulse) Interpolator available with Analog Output units.

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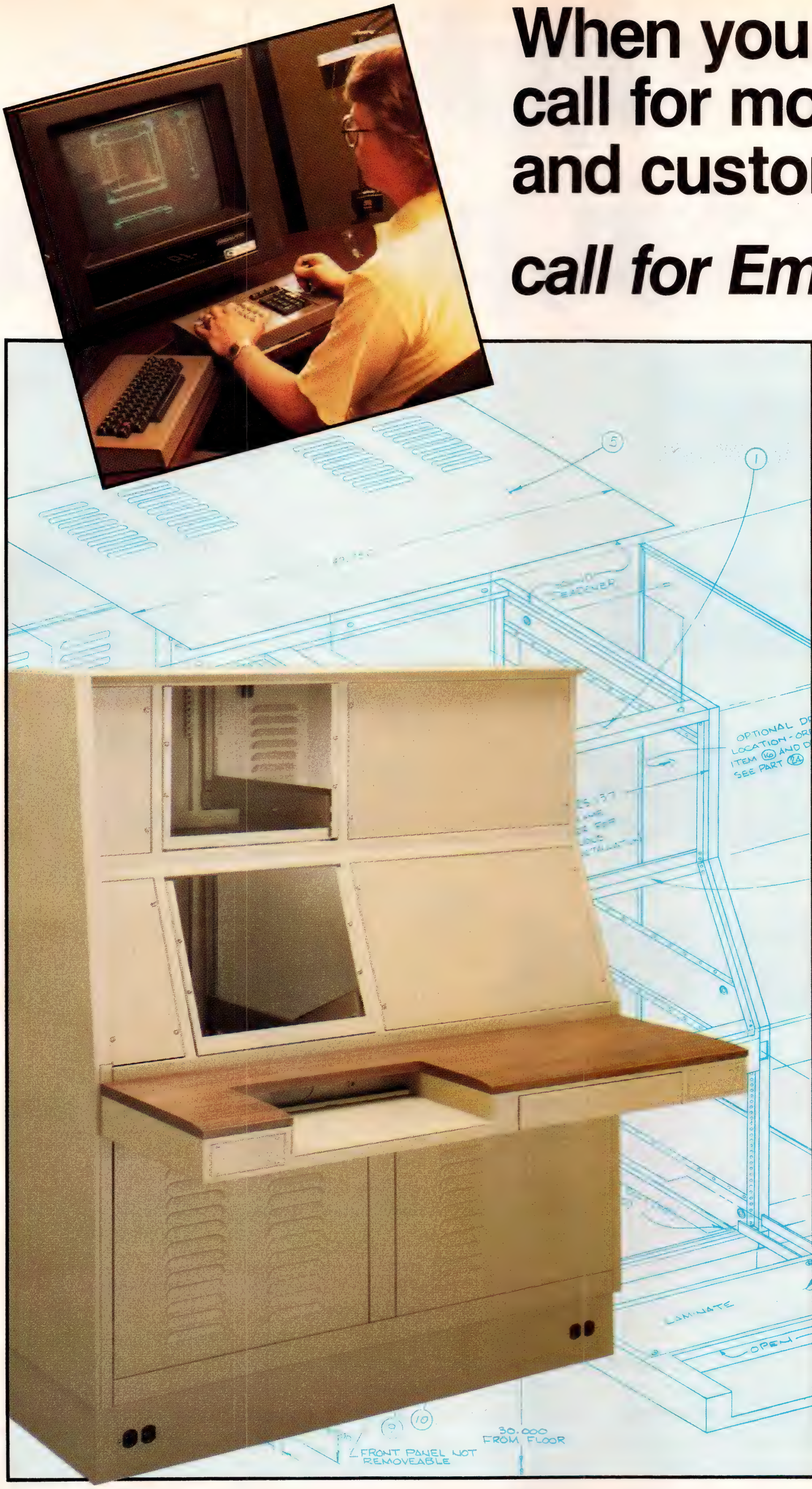
CIRCLE NO 240



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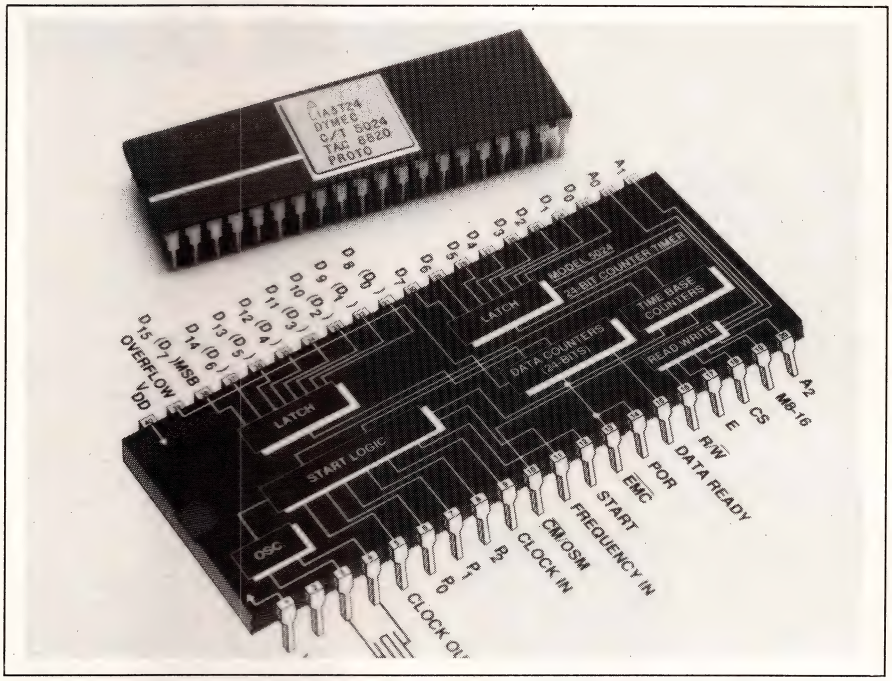
3M

INTEGRATED CIRCUITS

COUNTER/TIMER

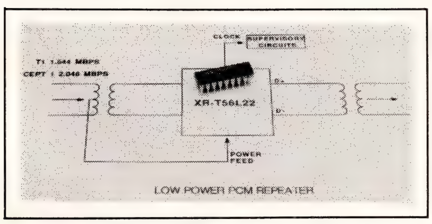
- *Operates to 50 MHz*
- *24-bit resolution*

Guaranteed not to miss a single count at 50-MHz inputs, the Model 5024 counter/timer consists of a counter with 24-bit resolution and a programmable time base. You can program by counting intervals from 100 nsec to 16 sec, and you can interface the counter data to either 8- or 16-bit µP data buses. The 5024 supports frequency-counting and period-averaging techniques, operating in both continuous and single-sampling mode. The 5024 includes a clock oscillator, a 24-bit counter with overflow flag, output, and programming data latches, and control logic. An internal multiplexer controls the switching and the clock inputs. The user need only supply a clock signal or crystal at any frequency to 20 MHz, and the input frequency to 50 MHz. The 5024 comes in a double-width 40-pin plastic DIP. $24 (100). Delivery, stock to eight weeks ARO.



Dymec Inc, 8 Lowell Ave, Winchester, MA 01890. Phone (800) 225-1151; in MA, (617) 729-7870. TWX 710-348-6596.

Circle No 351



PCM REPEATER

- *T1 and CEPT1 compatible*
- *Operates from a 5.1V supply*

Designed for digital PCM carrier systems operating at T1 and CEPT1 rates, the XR-T56L22 repeater IC provides all of the active circuitry needed for one side of a PCM repeater. Powered from a 5.1V supply, the IC requires 8.75 mA of current. The XR-T56L22 features an on-chip shunt regulator, an internal 90° phase shifter, dual-matched automatic line build-out ports, and a clock output. The low-power IC requires a minimum number of external components, thus permitting the same power supply to drive a greater number of parallel-connected repeaters. The clock output enables the design of a digital-code loopback circuit that meets the new Bellcore requirements. In plastic and ceramic DIPs, and surface-mount packages. $7.25 (1000).

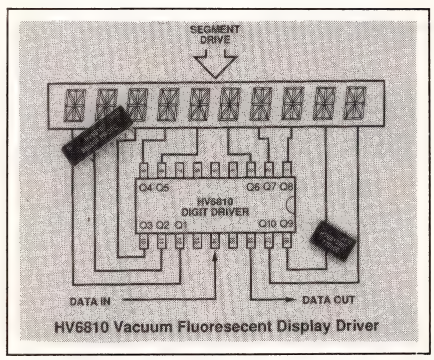
Exar Corp, Box 49007, San Jose, CA 95161. Phone (408) 434-6400. TWX 910-339-9233.

Circle No 352

DISPLAY DRIVER

- *Improved second source*
- *Pin-compatible with 4810 and 5810*

Designed for dot-matrix and vacuum-fluorescent displays, the HV6810 driver has a 10-channel, serial-to-parallel latched display. It's an improved second-source replacement for industry types 4810 and 5810. The HV6810 features an 80V (90V max) operating voltage and zero high-voltage standby power. Each output of the HV6810 can source 60 mA of current and has an active pull-down feature. The device also features a TTL-compatible logic section, 5V CMOS-compatible inputs, and a serial-data output that permits cascading of additional chips for use with large displays. DIP, $1.35; SOIC, $1.53 (100).



HV6810 Vacuum Fluorescent Display Driver

Supertex Inc, Box 3607, Sunnyvale, CA 94088. Phone (408) 744-0100. TWX 910-339-9388.

Circle No 353

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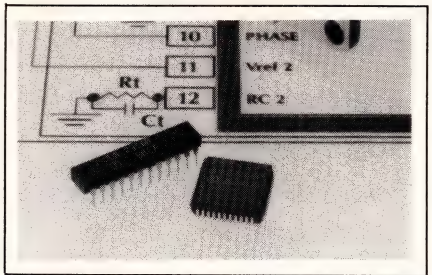


DUAL-MOTOR DRIVERS

- *Has two full-bridge drivers*
- *±750-mA continuous output current*

Designed to drive both windings of a bipolar stepper motor, the UDN2916B and UDN2916EB include two full-bridge drivers, each with its own PWM circuitry. Either IC can replace two PBL3717-type devices. The UDN2916 drivers feature a continuous output current rating of ±750 mA; they can handle ±1A peak at start-up. Each bridge includes both ground-clamp and flyback diodes for protection against inductive transients, as well as self-resetting thermal protection that disables the outputs whenever the chip temperature exceeds 160°C. Internally generated delays prevent crossover currents when the circuit switches. A PWM loop accepts 2-bit logic inputs for digital selection of motor-winding current. UDN2916B, in a 24-pin DIP, $2.09; UDN2916EB, in a 44-pin PLCC, $2.41 (1000). Delivery, 8 to 12 weeks ARO.

Sprague Electric Co, Semiconductor Group, Box 2036, Worcester, MA 01613. Phone (508) 853-5000. TWX 710-340-6304.

Circle No 354

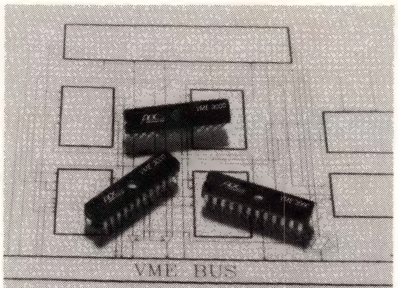
SCSI CONTROLLER

- *Fabricated in low-power CMOS*
- *Compatible with NMOS version*

Designed as a plug-in replacement for the NCR 53C80, the Am53C80 is a functionally-compatible replacement for the Am5380 NMOS type. At 105 mW, the power consumption of the Am53C80 is about 60% less than the NMOS version. Like the Am5380, the Am53C80 provides an asynchronous interface with data-transfer rates to 1.5M bytes/sec. The IC supports arbitration and includes parity generation with optional checking. High-current outputs provide direct connection to the SCSI bus. The Am53C80 communicates with the system CPU as a peripheral device. By reading from or writing to the appropriate registers on the SCSI controller, the CPU can initiate any bus activity, addressing both standard and memory-mapped I/O functions. In 48-pin DIPs and 44-pin PLCCs. $9.50 (100).

Advanced Micro Devices, Box 3453, Sunnyvale, CA 94088. Phone (408) 732-2400.

Circle No 355



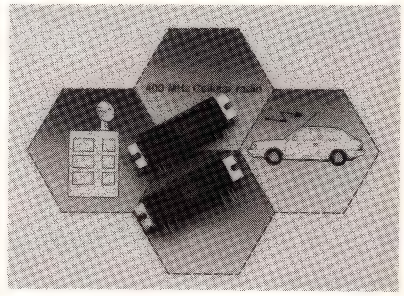
VME BUS INTERRUPT IC

- *Provides protocol logic*
- *Includes 48-mA drivers*

Built from programmable logic technology, the VME-3000 CMOS IC includes the protocol logic, 48-mA drivers, and input buffers needed to generate a single-level interrupt request on the VME Bus and respond to an interrupt request. The VME-3000 generates a VME Bus interrupt request signal (IRQ) and responds to an interrupt cycle when it receives an IACKIN signal from the system master. The VME-3000 then asserts either IACKOUT or INTACK, depending on the interrupt cycle selection. You can use the VME-3000 with the company's VME-2000 slave and VME-1200 master interface chips or with any VME-compatible master and slave modules. The chip is packaged in a 24-pin DIP. $26 (samples).

PLX Technology, 520 Weddell Dr, Suite 3, Sunnyvale, CA 94089. Phone (408) 747-1711.

Circle No 356



RF POWER MODULES

- *Operate at 400 MHz*
- *Have 20W of output power*

Designed for cellular radio applications, the BGY49A and BGY49B power modules operate from 12.5V battery supplies and feature 20W output power over the 400- to 470-MHz frequency range. Both devices offer an output power control range of more than 30 dB, a maximum drive power requirement of 150 mW, and an efficiency of greater than 35%. The modules differ only in operating frequency. The BGY49A operates from 400 to 440 MHz; the BGY49B operates from 440 to 470 MHz. The 20W output level ensures 15W at the antenna—a requirement of 400-MHz systems. The modules can withstand a VSWR of 50:1 for short-period overload conditions at the maximum rated output power. Samples are available from stock; production

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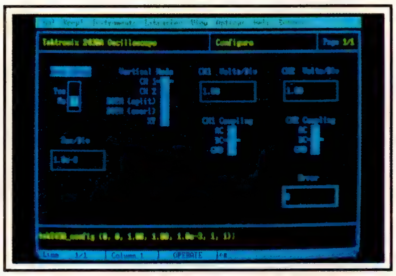
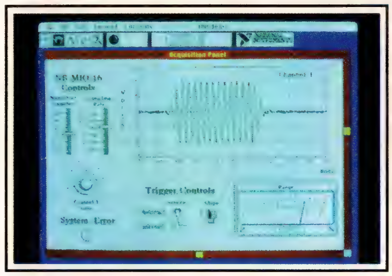
Integrated libraries for GPIB, RS-232, A/D-D/A-DIO plug-in cards, and modular instruments.



Intuitive character-based function panels that automatically generate source code.

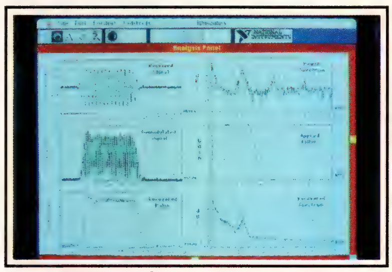


Front panel user interface with virtual instrument block diagram programming.

Analysis

Extensive libraries for data reduction, digital signal processing, and statistical analysis.

Over 100 analysis functions plus all the built-in functions of your language.



Over 250 icons for computation and analysis.

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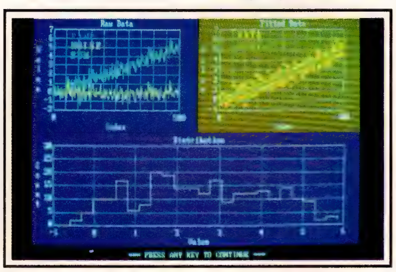
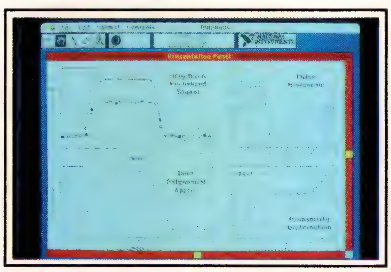
Flexible high-performance graphics and report generation.



Extensive graphics support for CGA, EGA, MCGA, VGA, and Hercules.



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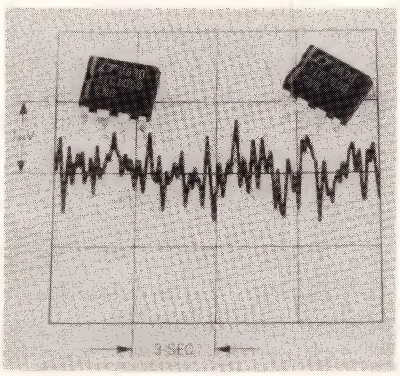
Philips Components Division, Box 523, 5600 AM Eindhoven, The Netherlands. Phone 3140-757189. TLX 51573. FAX (3140) 757319.

Circle No 357

Amperex Electronic Corp, Box 560, Hicksville, NY 11802. Phone (516) 931-6200.

Circle No 358



OP AMP

- *Chopper stabilized*
- *Includes S/H capacitors*

According to the manufacturer, the LTC1050 is the first chopper-stabilized op amp to include S/H capacitors on chip without degrading device performance. The LTC1050 features overload recovery times from positive and negative saturation conditions of 1.5 and 3 msec, respectively. Other features include a maximum offset voltage of 5 μV, a dc to 10-Hz input noise voltage of 1.8 μV p-p, and a typical voltage gain of 160 dB. The LTC1050 achieves a slew rate of 4V/μsec and a gain-bandwidth product of 2.5 MHz with only 900 μA of supply current. The LTC1050 is available in both military and commercial versions. Packages include an 8-pin plastic DIP, a ceramic DIP, and SO packages. Commercial plastic versions, $2.25 (100).

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 432-1900. FAX 408-434-0507.

Circle No 359

HIGH-SPEED FIFOs

- *Feature 15-nsec access times*
- *Available in two organizations*

The SSL7201 and SSL7202 are mid-density FIFOs with 15-nsec access times. Featuring dual-port static RAM (SRAM) architectures, the 7201 has a 512-word × 9-bit organization, and the 7202 has a 1024-word × 9-bit organization. According to the manufacturer, both parts are the fastest available in these densities and organizations. Both parts are pin-compatible with industry standards with the same part numbers. They also handle byte parity, an increasingly popular feature in high-end 32-bit CISC and RISC systems. The devices are available in performance grades of

15, 20, 25 and 30 nsec, and in a choice of 28-pin DIP or 32-pad CLCC and PLCC packages. $40.50 to $114.66 (100).

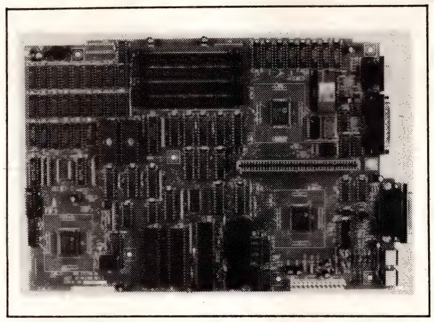
Saratoga Semiconductor, 10500 Ridgeview Court, Cupertino, CA 95014. Phone (408) 864-0500. FAX 408-446-4416.

Circle No 360

PS/2-COMPATIBLE ICs

- *Emulate IBM PS/2 Model 30*
- *3-chip controller plus VGA chip*

Emulating the IBM PS/2 Model 30, the 3-chip set includes the VL82C031 system controller, the VL82C032 I/O controller, and the VL82C033 disk controller. A fourth chip, the VL82C037 video-graphics controller, is compatible with other PS/2 models, as well as the IBM PC/AT and PC/XT. The dual-speed 8-or 10-MHz VL82C031 controls memory, parity, address paths,



data paths, and four DMA channels. The VL82C032 controls the keyboard and pointing device, two serial channels, disk storage, and display functions. The VL82C033 contains an analog data separator, a phase comparator, filters, and other elements for floppy-disk control. The VL82C037 provides support for 800 × 600-pixel displays having as many as 16 colors. 3-chip set, $92.60; VGA chip, $38.60 (1000).

VLSI Technology, 8375 South River Parkway, Tempe, AZ 85284. Phone (602) 752-8574.

Circle No 361

FIBER-OPTIC CHIPS

- *Fabricated in GaAs*
- *Chip set includes seven devices*

Designed for digital transmission over fiber-optic links, this chip set contains a transimpedance amplifier, an AGC amplifier, a laser driver, a decision circuit, a multiplexer, a demultiplexer, and a clock-recovery circuit. Fabricated in GaAs, the chip set has a data-rate capability from 2G to 3G bits/sec. The transimpedance amplifier has a sensitivity of −32 dBm at 2G bits/sec, the AGC amplifier has a gain of 40 dB max, and the laser driver features adjustable modulation current from 20 to 80 mA. Both the laser driver and the decision circuit have rise and fall times of <150 psec. The acquisition time for the clock-recovery circuit ranges from 75 to 150 μsec. The 4-channel-type multiplexer and demultiplexer also have rise and fall times of <150 psec. Transimpedance amplifier,

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CIRCLE NO 244

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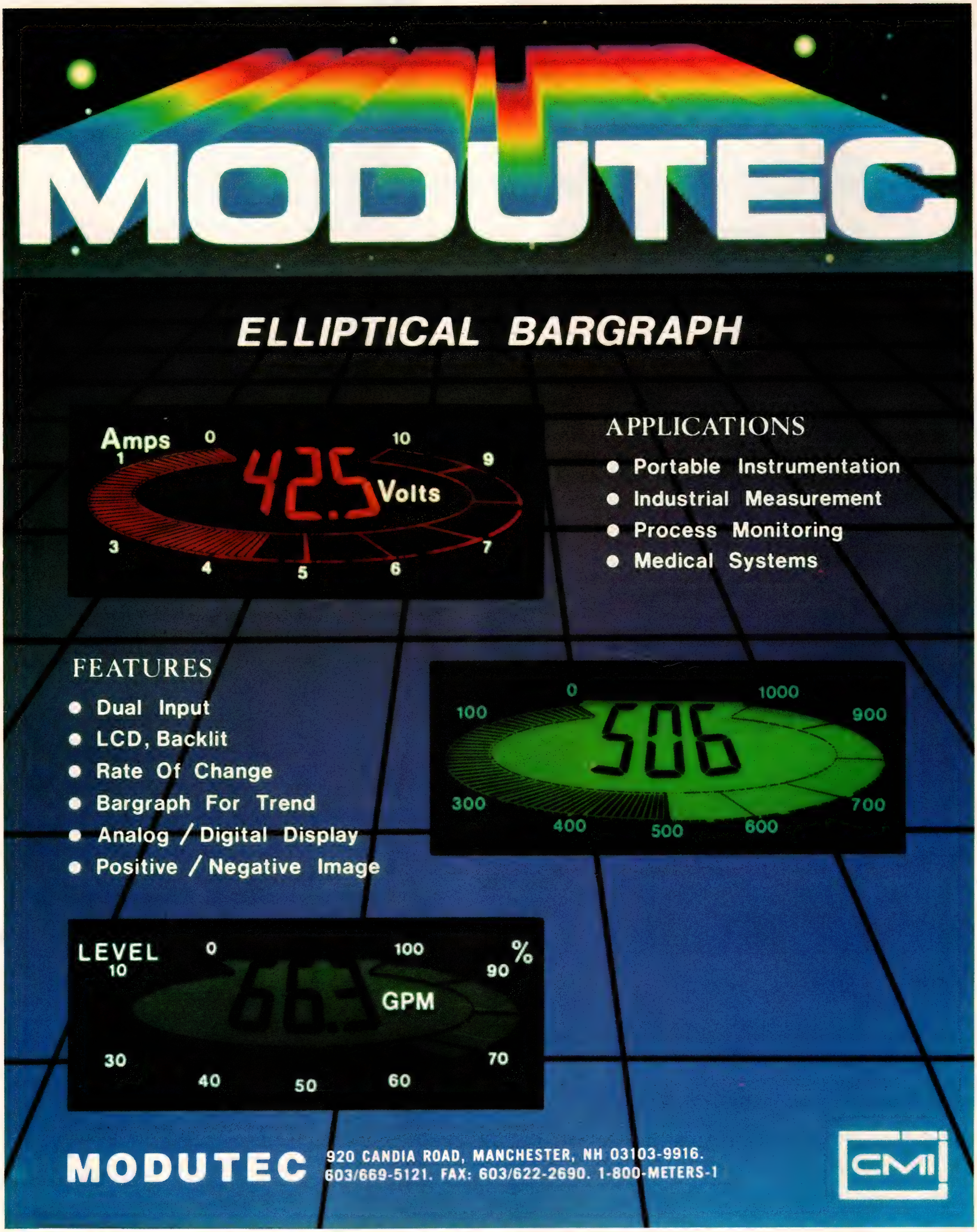


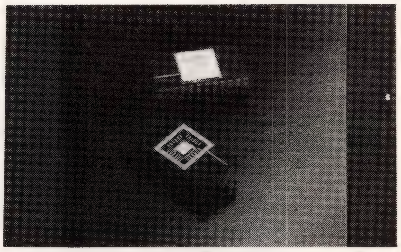
WESCON BOOTH NO. 2662

CIRCLE NO 245

\$40; AGC amplifier, \$35; decision circuit, \$50; and laser driver, \$60 (1000). The multiplexer, demultiplexer, and clock-recovery circuit will be available by mid-1989.

AT&T Microelectronics, 555 Union Blvd, Allentown, PA 18103. Phone (800) 372-2447.

Circle No 362



8-BIT FLASH ADC

- *20-MHz sampling rate*
- *10-MHz full-power bandwidth*

Fabricated in low-power CMOS, the ADC-208 flash A/D converter provides an 8-bit sampling rate of 20 MHz and effective bit rates to 30 MHz in the burst mode. The video flash converter operates from a 5V supply and consumes 500 mW of power. Other features include a one-shot-mode conversion time of 35 nsec and a mid-point tap for use with an external voltage source to improve integral linearity. The ADC-208 also provides latched 3-state outputs for μP interfacing. Packaged in a hermetic 24-pin ceramic DIP, the device is available in both commercial and military temperature ranges. \$50 to \$158 (100).

Datel Inc, 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. TWX 710-346-1953.

Circle No 363

S/H AMPLIFIER

- *500-nsec acquisition time*
- *Features 12-bit accuracy*

Fabricated with a dielectric isolation process, the SP5330 high-speed S/H amplifier achieves a 500-nsec acquisition time with 12-bit or 0.01% accuracy. The SP5330 includes a differential-input transconductance amplifier, a low-leakage analog switch, and an output integrator stage with an internal 90-pF hold capacitor. The chip, which is capable of high-speed data acquisition in both 10-bit (350 nsec) and 12-bit (500-nsec) systems, has a low droop-rate of 0.01 μV/μsec and a slew rate of 90V/μsec. The SP5330 is available in a 14-pin DIP and is TTL/CMOS compatible. Commercial versions, \$14.95; military versions (scheduled for the first quarter of 1989), \$49.90 (100).

Sipex Corp, 22 Linnell Circle, Suburban Industrial Park, Billerica, MA 01821. Phone (508) 667-8700.

Circle No 364

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CIRCLE NO 246

A/D CONVERTER

- *12-bit operation*
- *4-µsec conversion time*

The ADC6010 12-bit successive-approximation A/D converter has an internal S/H amplifier, a 3.3-MHz clock, and a 6.3V reference. The 4-µsec conversion time can be short-cycled to 2.8 µsec. The device features five user-selectable input ranges: 0 to 5V, 0 to 10V, ±2.5V, ±5V, and ±10V. Data is available in parallel or serial format with corresponding clock and data signals. The gain and offset are externally trimmable to zero, and full-scale accuracy is ±0.012% ±½ LSB. The power consumption is 1.2W typ. The ADC6010 is packaged in a hermetic 32-pin DIP and is available in commercial and military versions. From $93 (100).

Advanced Analog, 2270 Martin Ave, Santa Clara, CA 95050. Phone (408) 988-4930. TWX 910-338-2213.

Circle No 365

DTMF TRANSCEIVER

- *5V CMOS technology*
- *Generates and decodes 16 digits*

The SSI-75T2091 dual-tone multiple-frequency (DTMF) transceiver provides tone generation and detection, call-progress detection, and early-tone detection on a single chip. The device can both generate and decode all 16 standard tone digits. When detecting the presence of signals in the 305- to 640-Hz band, the SSI-75T2091 offers call-progress detection, which can discern busy signals, ring signals, and dial tones. The early-detect feature can detect incoming DTMF tones before the timing validation occurs. The only external components required by the SSI-75T2091 are a 3.58-MHz crystal and a 1-MΩ resistor to provide the time base for digital functions and the switched-capacitor filters in the device. 28-pin DIP, $10.92; 28-pin PLCC, $11.46 (100).

Silicon Systems, 14351 Myford Rd, Tustin, CA 92680. Phone (714) 731-7110.

Circle No 366

EEPROMs

- *Accessed serially via an I²C Bus interface*
- *Have chip- and byte-erase modes*

The 512×8-bit SDA 2546 and 1024×8-bit SDA 2586 serially accessed EEPROMs feature an I²C Bus interface—a 2-line serial data/control interface—through which

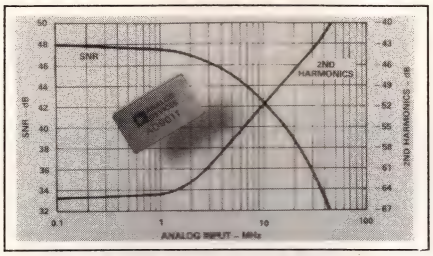
you can read or write data to or from the memory. You can reprogram individual words within the device by performing an erase cycle followed by a write cycle. On-chip circuitry completes the reprogramming operation, within 10 msec typ and 20 msec max. For words that are already in the erased condition, the programming time is automatically shortened. You can also erase the entire memory in a single erase operation. A flag bit in the device's status register allows you to determine when erase or reprogramming cycles are completed. The allowable number of reprogramming cycles per address location is in excess of 10^4, and the specified data-retention period is >10 years. Both devices operate from a single 5V supply and are housed in 8-pin DIPs. SDA2546 $2.90; SDA2586 $3.50 (10,000).

Siemens AG, Zentralstelle für Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

Circle No 367

Siemens Components Inc, 2191 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 980-4500.

Circle No 368



A/D CONVERTER

- *Offers 8-bit, 100-MHz performance*
- *Includes buffer and reference*

Combining a monolithic flash converter, a wideband buffer op amp, and a voltage reference, the hybrid AD9011 comes in a 24-pin metal DIP. User-selectable input pins provide gains of −4, −2 and −1 with corresponding input voltage spans of 0.5, 1, and 2V p-p. The on-board voltage reference delivers an external current to 12 mA and has a maximum voltage drift of 40 ppm/°C over the specified operating temperature range. With a full-scale step, the AD9011 recovers to 8-bit accuracy (±1LSB) in 11 nsec. Over the 80-MHz input bandwidth, gross error codes occur less than once in every 10^{12} conversions. With a 9.3-MHz input signal, the signal-to-noise ratio is 43 dB, and maximum in-band harmonics are −46 dB. The AD9011 operates from +5 and −5.2V supplies and is available in commercial and military temperature ranges. From $180 (100).

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 935-5565. TLX 924491. TWX 710-394-6577.

Circle No 369

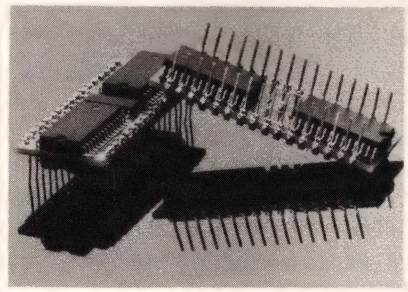
DRIVER/RECEIVER ICs

- *Conform to RS-232C protocols*
- *Operate from a 5V supply*

The uPD4711 and uPD4712 CMOS line driver/receiver chips conform to all standard RS-232C protocols. The ICs incorporate dc-dc converters that allow them to operate from a 5V supply. The connection of four external capacitors provides voltages of 10V or −10V from the single source. The 4711 integrates two sets of driver/receivers on a single chip; the 4712 provides four sets. The chips also include an internal power-on/off reset function, which prevents system malfunction when power to the ICs is turned on or off. 4711CX 20-pin DIP and 4711GS 28-pin surface-mount package, $4.50 to $5; 4712CY 28-pin DIP and 4712GT 28-pin surface-mount package, $6.50 to $7 (100).

NEC Electronics Inc, Box 7241, Mountain View, CA 94039. Phone (415) 960-6000. TWX 910-379-6985.

Circle No 370



1M-BIT STATIC RAM

- *Has byte-wide format*
- *Includes high-speed decoder*

The MS12808 1M-bit static RAM is organized in a 128k×8-bit byte-wide format. The module contains four 32k×8-bit SRAMs, a high-speed CMOS decoder, and a decoupling capacitor. The MS12808 conforms to the JEDEC byte-wide pinout and fits into a standard 32-pin, 600-mil-wide socket. The module is available with access-time ratings of 100, 120, and 150 nsec. 100-nsec version, $145; 120-nsec version, $120; 150-nsec version, $90 (1-25).

Micro Electronic Technologies Inc, 35 South St, Hopkinton, MA 01748. Phone (508) 435-9057.

Circle No 371

HYBRID MEMORY

- *Allows custom memory configurations on a PGA*
- *Suitable for high-reliability applications*

Constructed using LCC memory devices mounted on a ceramic pin-grid array (PGA), Puma II memories offer a 50% space saving when compared to conventional DIP memories. The ceramic PGA, which also carries decoupling capacitors for the memory devices, provides a large thermal mass for effective heat sinking, thus improving device

The Sine of a Good Generator

Purity • Precision • Speed

- typically 0,0006% (–105 dB) distortion in the audio range
- ±0,1192 mHz frequency accuracy throughout the 0,2 Hz to 200 kHz range
- precision attenuator with ±0,026 dB (±0,3%) accuracy across the entire 100 μV to 5 V range
- very fast response time for *all* functions via IEEE-488 interface
- heterodyne synthesis gives "instantaneous" settling (<0,1 ms) of frequency and amplitude
- memory sweep feature with pre-defined amplitude weighting
- two models: Sine Generator Type 1051 and Sine/Noise Generator Type 1049

Brüel & Kjær

Brüel & Kjaer Instruments, Inc. 185 Forest Street · Marlborough, MA 01752 USA · Telephone 617/481-7000

WORLD HEADQUARTERS: DK-2850 Nærum · Denmark · Telephone: +45 2 80 05 00 · Telex: 37316 bruka dk

Australia (02) 450-2066 · Austria 02235/7550*0 · Belgium 02 · 242-97 45 · Brazil 246 8149 · Canada (514) 695-8225 · Finland (90) 80 17 044 · France (1) 64 57 20 10
Federal Republic of Germany (04106) 4055 · Great Britain (01) 954-2366 · Holland 03 402-39 994 · Hong Kong 5-487486 · Italy (02) 52 44 141
Japan 03-356-1711 · Republic of Korea 02-793-6886 · Norway 02-78 70 96 · Singapore 225 8533 · Spain (91) 268 10 00 · Sweden (08) 711 27 30 · Switzerland (042) 65 11 61
Taiwan (02) 713 9303 · USA (617) 481-7000 · Local representatives and service organisations world-wide

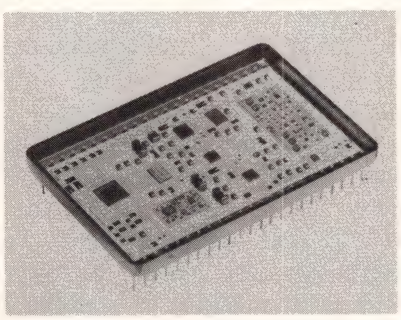
88-059

CIRCLE NO 248

reliability. As a result, the memories are suitable for use in military, aerospace, and similar high-reliability applications. Puma II memories can incorporate static RAMs or EEPROMs with capacities ranging from 2k×8bit to 128k×8bit and UV erasable EPROMs with capacities between 8k×8bit and 64k×8bit. You can mix memory types on a single PGA and configure the memory devices to provide 8-, 16-, or 32-bit data widths. The 66-pin PGA measures 1.12 in. square. A military-grade memory comprises four 32k×8-bit static RAMs, screened to MIL-STD-883C requirements. £250 (100).

Hybrid Memory Products Ltd, Elm Rd, W Chirton Industrial Estate, North Shields, Tyne and Wear NE29 8SE, UK. Phone (09125) 80690. TLX 53206. FAX 091-259-0997.

Circle No 372



12-BIT HYBRID ADC

- *Has 10-MHz speed*
- *Includes track-and-hold circuit*

The ADC-00110 hybrid IC features a 12-bit, 10-MHz digitizing capability. Contained in its 46-pin package are a track-and-hold circuit, an A/D converter, data registers, a 3-state output buffer, and timing circuits. The ADC-00110 interfaces to most commonly used CPUs. Because the timing is self-contained, the hybrid IC requires only an encoding command to start its conversion cycle. Both TTL- and ECL-compatible models are available. Specifications include a signal-to-noise ratio of 66 dB and a linearity of 0.025%. The device is available with an operating temperature range of −55 to 125°C and MIL-STD-883 screening. From $1500. Delivery, stock to 12 weeks ARO.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600. TLX 510-228-7324.

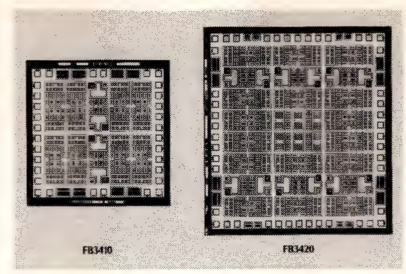
Circle No 373

LINEAR ARRAY

- *36V dual-layer-metal process*
- *Has a mini-tile architecture*

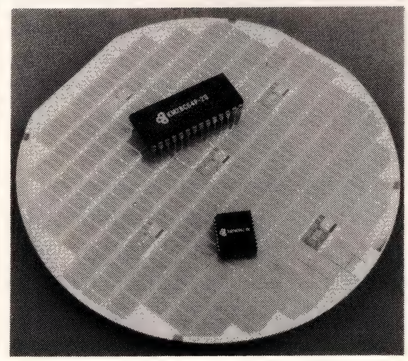
The 36V-rated FB3400 family of analog arrays combines the company's mini-tile architecture with the ability to handle traditional ±15V swings. The double-layer-metal process simplifies the interconnection of complex designs.

Three are presently available. The FB3420 and FB3430 include additional capacitors to ease the design of op-amp filters. The FB3410 replaces the extra capacitors with transistors for use with comparator designs, or discrete transistor re-lplacements. The FB3400 family consists of five types of mini-tiles, which you can use to implement functional equivalents of a wide variety of analog circuits such as op amps, comparators, voltage references, and video amplifiers. Typical NRE (nonrecurring engineering) charges, $30,000. Delivery, 12 to 14 weeks ARO.



Micro Linear Corp, 2092 Concourse Dr, San Jose, CA 95131. Phone (408) 433-5200.

Circle No 374



EEPROMs

- *64k-bit devices*
- *200- and 250-nsec access times*

The KM28C64 and KM28C65 64k-bit EEPROMs are available in access times of 200 and 250 nsec, as well as in slower speed ratings. The chips are organized into 8,192 8-bit words and feature a 28-pin, byte-wide JEDEC standard pinout. The EEPROMs also feature a 32-byte page mode, making it possible to rewrite each chip in only 1.3 sec max. Data is modified using simple TTL-level signals and a 5V power supply. An internally self-timed write cycle latches both address and data to provide a free system bus during the 5-msec/page write period. Endurance ratings specify 10,000 erase/write cycles and data retention for more than 10 years. The devices are available in 28-pin DIPs and 32-pin PLCCs. From $9 (100).

Samsung Semiconductor, 3725 N First St, San Jose, CA 95134. Phone (408) 434-5561. TLX 339544.

Circle No 375

CIRCLE NO 250

0 to 60 in 5 seconds

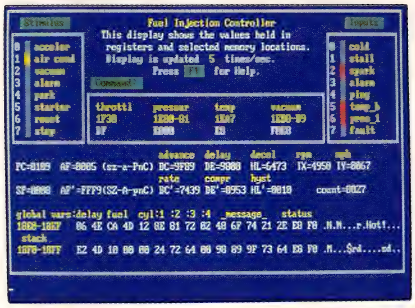
with new UniLab 8620 analyzer-emulator.

▪ 64Kbytes from hard disk in 5 seconds. That's moving. But today you've got to be fast just to stay in the race for better microprocessor designs.

▪ The secret is a new, high-speed parallel interface: the Orion bus. Which zips data between your PC/AT and the 8620 analyzer-emulator, breaking the RS-232 bottleneck.

▪ The 8620 with O-bus gives you complete program diagnosis — and solutions — in real time. For more than 150 different microprocessors. Using **the same command set** environment.

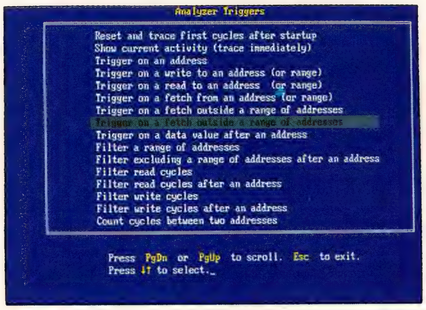
▪ A generous 2730 trace-cycle buffer with selective filtering lets you cut through the clutter and display just the traces you wish. And you get 1μsec resolution in program time measurement. Plus continuous InSight monitoring of your program's key functions as they are performed.



InSight Display. InSight blends analyzer-emulator techniques to give you continuous, real time monitoring of key processor functions. And still services user interrupts. It displays changing register contents, I/O lines, ports, user-defined memory windows. With your own labels.

▪ On top of that, you get UniLab's trademark ability to debug by symptom, not just by breakpoint and single step. And, to help you complete the job on time, on the spot, a stimulus generator and EPROM programmer are included.

▪ Ease of use, another Orion trademark, is also built in. So you have all the familiar features and formats you're used to working with. It doesn't matter if your project is a single chip controller or complex 16-bit



Analyzer Triggers. Commonly used triggers can be selected quickly from a list of standard and user-defined triggers.

microprocessor, the 8620 is the top price/performance analyzer-emulator that does it all. At just $4380. With processor Personality Paks typically $550 each.

▪ UniLab 8620. Fast-lane debugging that gets you to market quicker.

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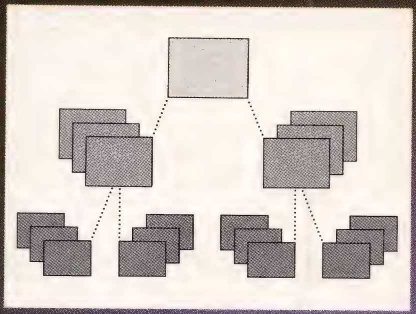
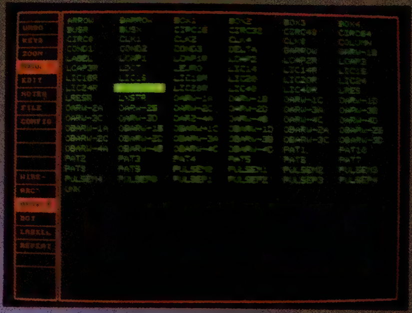
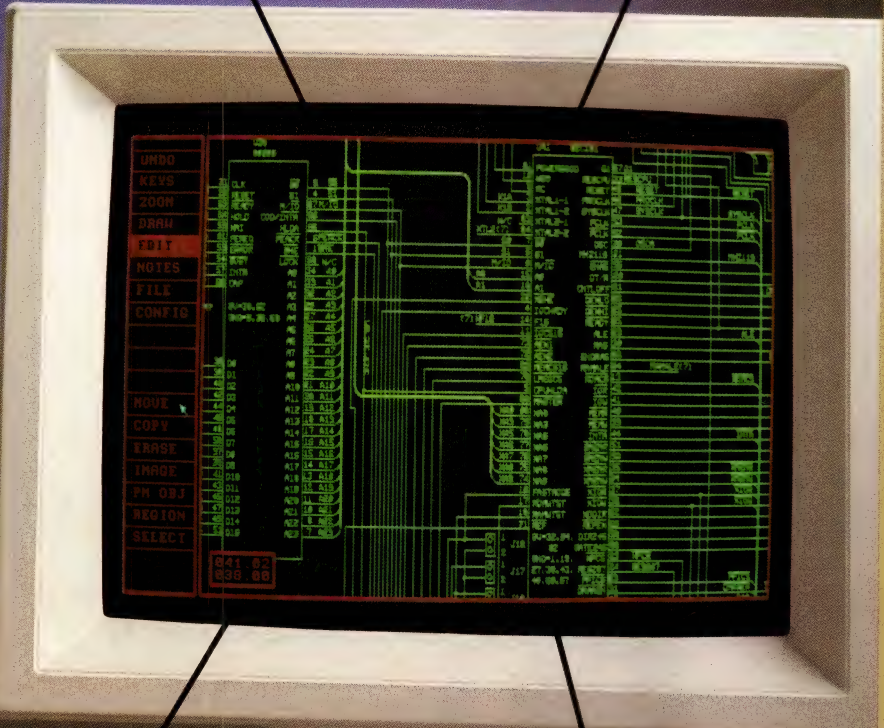
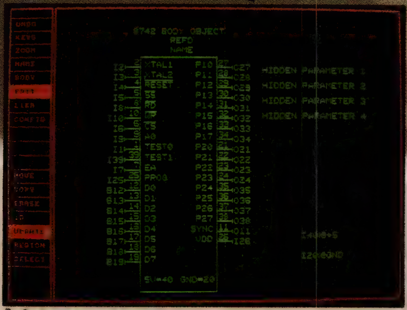


SCHEMA II+ supports true hierarchical design of unlimited levels up to 99 pages per drawing block

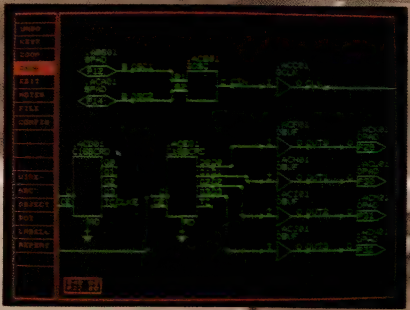


True interactive parts browsing simplifies component inspection and selection





Full Graphical Object Editor resides with the Schematic Editor for quick component creation



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PC I/O BREAKTHROUGHS

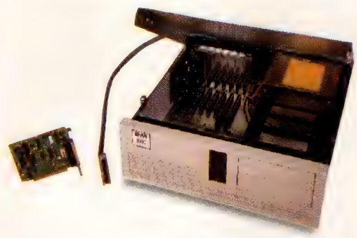
NEW

Direct-to-Disk 190KB/s Data Transfer

PCI-20096S series software drivers transfer huge amounts of data both to and from disk. Archives data for event analysis, environmental monitoring, etc. Operates with hard disk, RAM disks, floppy disks and tape drives. Available for BASIC, C and TURBO PASCAL.

NEW

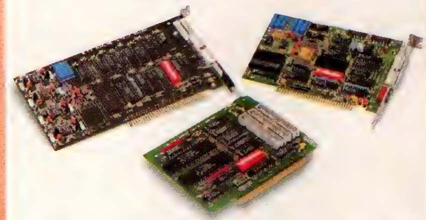
PC Expander Holds 7 Boards



The PC Expander (PCI-20055H series) features easy-access 7-slot board expansion capacity with fan-cooled 200W power supply. Permits up to 600 channel data acquisition systems. Accepts other PC compatible expansion boards. PCI-20063A-1 host interface board required.

NEW

Analog & Digital SuperBoards



Unequalled cost/performance plus FREE Basic Software drivers with:

- PCI-20093W-1 Analog Output Board with up to 31K ch/sec. 8 channels, V or I output.
- PCI-20089W-1 16/8 channel Analog Input Board with 32KHz sample rate and programmable gain.
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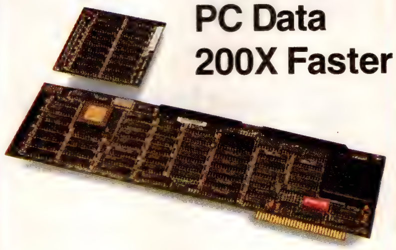
NEW

Real-Time Industrial Control & Monitoring

LT/Control software (PCI-20097S-1) provides process control, data logging and process monitoring. Provides for full-color animated, customized process-flow diagrams in real-time. Open loop and closed loop (PID) control algorithms included. No programming skills needed.

NEW

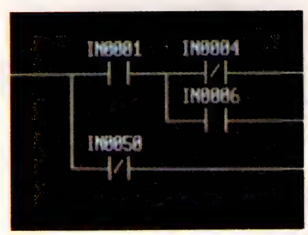
DSP Professional System Processes PC Data 200X Faster



Supercharged digital signal processing based on the industry standard TI TM320C25 processor. Up to 96KWords of on-board high speed memory with zero wait states. Powerful I/O options include analog I/O, digital I/O counters and timers. Extensive DSP software available.

NEW

Relay Ladder Logic Software



Process monitoring and control PCI-20073S-1 software converts your PC into a high-performance Programmable Logic Controller. Features Relay Screen Editor and single-key selection and entry of conventional Relay Ladder Symbols. Also includes Math Functions, Logic and Jumps, Password Security and more.

Never before have PC data acquisition, test, measurement and control products offered so much performance for so little money. Plus, each member of this all new hardware and software line-up is fully compatible with Burr-Brown's extensive PCI-20000 family, offering you the ultimate in flexibility and expandability. When it comes to PC data acquisition, Burr-Brown is the price/performance leader. Send for your *free* PC Instrumentation Handbook and you'll understand why. Call **602/746-1111** or write Burr-Brown, 1141 West Grant Road, MS131, Tucson, AZ 85705.

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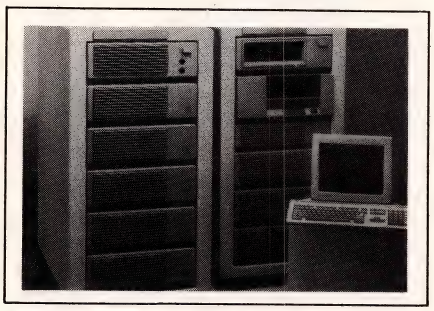

MULTIUSER SYSTEM

- *Dynamically balances the load of as many as 256 users*
- *16-slot Nubus version operates with up to eight 68020 CPUs*

The System 1500 expanded line of multiprocessor systems for multiuser environments consists of four models: the 1510, 1530, 1540, and 1580. Models 1510, 1530, and 1540 are all designed around a 7-slot Nubus, and the RAMs in each of the four models come with with error checking and correction. The entry-level Model 1510 for 30 to 50 users has one 68020 µP board with 10M bytes of RAM. The 1510 also has a 182M-byte hard-disk drive, a 60M-byte tape drive, a SCSI controller, and a model 924 terminal. The Model 1530 and 1540 are similar with the following exceptions. The model 1530 for 50 to 80 users can have as many as three CPU boards with 12M bytes of RAM and a 380M-byte hard-disk drive. The Model 1540 for 80 to 128 users has as many as four CPU boards with 20M bytes of RAM, a 1G-byte hard-disk drive, and a 2G-byte tape drive. The 1580 has a 16-slot Nubus that can accommodate eight CPU boards with 20M bytes of RAM. Designed for 128 to 256 users, the 1580 has a 1G-byte hard-disk drive and a 2G-byte tape drive. The 1510, $39,995; the other three models, with two CPU boards: 1530, $80,995; 1540, $121,995; 1580, $172,995.

Texas Instruments Inc, Data Systems Group, Box 181153, DSG-233, Austin, TX 78718. Phone (800) 527-3500.

Circle No 380

MOTHER BOARD

- *Allows you to build IBM PC/AT-compatible computers*
- *Has seven expansion slots*

Based on Zymos' Poach chip set, the MM286AT mother board allows you to build an IBM PC/AT-compatible computer around it. It runs an 80286 µP that you can clock at 8 or 10 MHz, and the board also has provision for an 80287 math coprocessor. It's supplied with 512k

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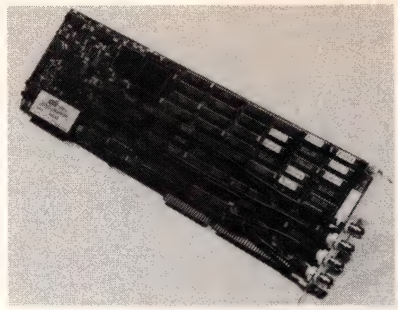
bytes of RAM that you can expand onboard to 1M byte. In addition, the board includes a floppy-disk controller, two RS-232C I/O ports, and a Centronics-compatible printer port. There are also seven expansion-slot connectors, five of which are configured to accept AT boards; the other two accept boards that are compatible with the IBM PC/XT. The Award BIOS is available for the board. Approximately £500.

Micro-Marketing Electronics Ltd, Unit 4, Soho Mills Industrial Estate, Wooburn Green, High Wycombe, Buckinghamshire HP10 0PF, UK. Phone (0628) 529222. TLX 848080. FAX (0628) 810141.

Circle No 381



A/D BOARD

- *IBM/AT-style plug-in board that digitizes data at 100 MHz*
- *Has a 2-channel analog input bandwidth of 50 MHz*

The STR*8100 is an A/D board for IBM PC, PC/XT, PC/AT and 386 compatible computers. The single plug-in board contains an 8-bit flash converter that digitizes transient data at rates from 780 kHz to 100 MHz. An equivalent time-sampling mode digitizes data at a rate as high as 800 MHz. The board's 2-channel analog front end has a 50-MHz bandwidth. You can address its 64k-byte static RAM buffer on 16k-byte boundaries. Memory segmentation lets you collect short data blocks in 4-byte increments. You can trigger externally or via software for pre- or post-triggering modes with delays from 0 to 256k samples. A post-processor finds the peak amplitude and the peak's time-of-arrival within a software-defined window. The board comes with a 2-channel, real-time digital-oscilloscope display program and a 1-year warranty. $4400.

Sonotek Inc, 8700 Morrissette Dr, Springfield, VA 22152. Phone (703) 440-0222. TWX 910-250-5257. FAX 703-440-9512.

Circle No 382

DEVELOPMENT BOARD

- *For TI's TMS320C30 floating-point DSP chip*
- *PC/AT board and daughter board act as a coprocessor*

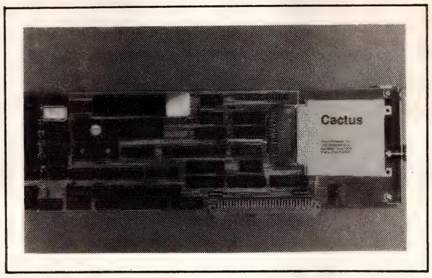
The Banshee System is an IBM PC/AT plug-in board for developing software for TI's TMS320C30 float-

CIRCLE NO 256

ing-point DSP chip. The board offers two types of memory options. It can hold 32k to 512k bytes of 35-nsec dual-access memory that the host can access by stealing cycles from the DSP chip. The DSP chip can access the memory with zero wait states. The other option is 8k bytes of 90-nsec dual-port memory that the host and the DSP chip can access with no wait states. The board communicates with the PC/AT host through the memories, a data-exchange register, or the host's DMA channel. An optional 16-bit A/D and D/A daughter board plugs directly into the AT-type board for I/O communications. Board with 128k bytes of dual-access memory, software package, without the TMS320C30 chip, $4995; daughter board, $795.

Atlanta Signal Processors Inc, 770 Spring St, Atlanta, GA 30308. Phone (404) 892-7265.

Circle No 383



LAN ADAPTER CARD

- *Provides communications at 2M bps for Macintosh II computers*
- *Occupies a single backplane slot*

The BroadTalk LAN board is a broadband LAN adapter board for the Macintosh II computer. The board uses a 2M-bps modem operating in a standard video channel for the broadband cable. The following inbound-to-outbound channel assignments are currently available: T14 to J, T14 to N, 2′ to O, and 3′ to P. The card uses 168.25 MHz as an offset frequency to translate channel T14 to J and a 192.25-MHz offset frequency for the other channel translations. The board occupies one backplane slot and uses Ethernet-packet-format driver software. You can change the board to an Ethernet adapter operating at a 10M-bps data rate by changing the modem to an Ethernet adapter module. Board with the broadband modem, $895; board with the Ethernet adapter module, $745. Delivery, 60 days ARO.

Cactus Computer Inc, 1120 Metrocrest Dr, Carrollton, TX 75006. Phone (214) 416-0525.

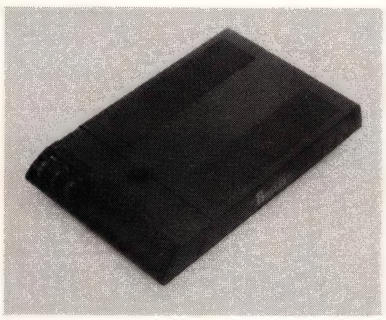
Circle No 384

9600-BPS MODEM

- *Complies with CCITT V.29, V.27, and Bell 212A standards*
- *The dialing protocol is the Hayes AT command set*

The E9612 9600-bps, stand-alone modem complies with the CCITT V.29, V.27, and the Bell 212A/103 standards and has automatic fall-

back and fall-forward modes. Operating in the asynchronous mode, the modem uses the company's speedy protocol (ESP) to achieve an effective throughput as high as 19.2k bps. It also operates with the Microcom networking protocol, class 5. The modem includes operational automatic dial-and-answer and manual originate-and-answer modes. It performs both tone and pulse dialing using the expanded Hayes AT command set with programmable S-Registers. Other features include a call-progress code



display, a stored dialing number with as many as 40 characters, and battery-backed memory, which preserves modem configurations and dialing settings. $1195.

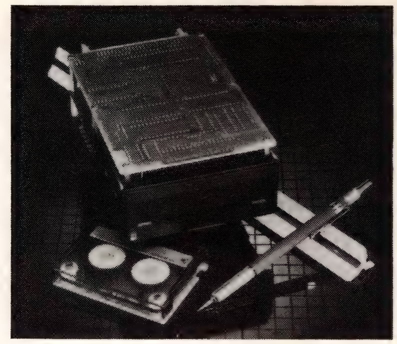
E-Tech Inc, 3333 Bowers Ave, #165, Santa Clara, CA 95054. Phone (408) 982-0270. FAX 408-982-0272.

Circle No 385

CARTRIDGE DRIVES

- *Records 86M bytes on a DC2000-type mini cartridge*
- *Average file-access time of 8 sec using the SCSI command set*

The MCD Series II cartridge-tape drive in a 3.5-in. form factor uses an extension of the QIC-100 data format to record 86M bytes on a high-density DC2000-type data cartridge. It records data at 16,000 bpi on 32 serpentine tracks using a group-code recording (GCR) scheme. The drive has an average



file-access time of 8 sec using the SCSI random-access common-command set and a 48k-byte data buffer. It performs read/write operations at 90 ips and has a rewind and search speed of 100 ips. The data transfer rate is 98.5k bytes/sec for fully corrected data with burst rates as high as 750k bytes/sec. The drive achieves a bit error rate of 1 in 10^{12} bits through the company's Heroic data recovery scheme, a 40-bit cyclic redundancy check for error detection, and an exclusive-OR

ECC with 50% data redundancy. The MTBF rating is 40,000 hours at 25% duty cycle, and the drive comes with a 12-month warranty. $480 (500).

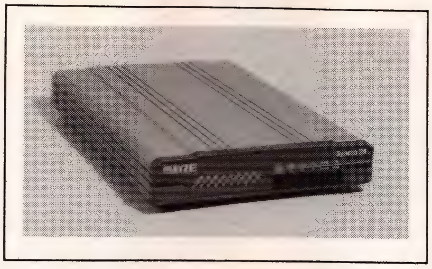
3M, Magnetic Media Div, 3M Center, St Paul, MN 55144. Phone (612) 733-7297.

Circle No 386

MODEM

- *Operates synchronously or asynchronously at 1200 or 2400 bps*
- *Stores 12 standard and 4 user-definable modem setups*

The Syncro-24 V.26/V.26-bis modem operates synchronously or asynchronously at bit rates of 1200 or 2400 bps, in full-duplex mode over 4-wire leased lines, or in half-duplex mode over 2-wire lines. Over leased lines, its 10-msec synchronization time suits it for both multidrop and point-to-point applications. The modem is software pro-



grammable using the industry standard AT prefixed commands. In addition, you can select one of 12 standard or four user-definable modem configurations, using front-panel pushbuttons. A separate command port allows you to perform modem configuration, autodialing, and call-monitoring operations without disturbing the data channel. The autodialer, which uses AT prefixed commands or the V.25-bis asynchronous/synchronous protocol, can store 20 telephone numbers. You can select and dial stored numbers from the modem's front panel or activate the selected number via the V.24 DTR (data terminal ready) signal. The Syncro-24 is available as a stand-alone unit or as a card for the company's Network-16 communications rack. Stand-alone unit, £445; modem card, £395.

Mayze Systems Ltd, Delta 900, Great Western Way, Swindon, Wiltshire SN5 7XQ, UK. Phone (0793) 511789. TLX 445707. FAX (0793) 511683.

Circle No 387

MOTHER BOARD

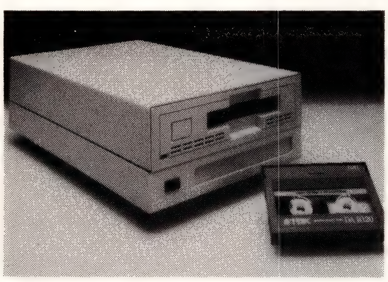
- *Transforms an IBM PC/XT into a 20-MHz 80386*
- *Has four 16-bit, three 8-bit, and one 32-bit slots*

According to the manufacturer, the SX386 rev 5 system mother board can transform IBM PC/XTs and compatible computers into 20-MHz, zero-wait-state systems. Besides its 20-MHz 80386 CPU, the board has 1M byte of 32-bit surface-mount dy-

namic RAM modules (expandable to 16M bytes) and a 20-MHz memory bus with 32-bit addressing; it can also support an 80387 math coprocessor. Its eight expansion slots are divided into four 16-bit, three 8-bit, and one 32-bit slots. The board runs with Unix, Xenix, PC-MOS 386, and other operating systems designed for the 80386 CPU. The system and the EGA BIOS can operate from the 32-bit memory. In addition, the board allows PC/XT users to run the OS/2 operating system and maintain their present investment in XT software and peripherals. Mother board with 1M byte of RAM, $1900; 16-bit disk controller, $170.

Dyna Computers, 3081 N First St, San Jose, CA 95134. Phone (408) 943-0100. FAX 408-943-0642.

Circle No 388



TAPE BACKUP

- *System features 600M-byte storage capacity*
- *Uses DAT format with error-correction extensions*

The QA-600 tape backup system based on the digital audio-tape (DAT) cassette format features 600M bytes of storage capacity and runs on SY-TOS tape operating-system software. The system's software format uses the standard DAT physical format with added error-correction-code extensions to correct as many as six consecutive bad tracks. The software format resembles the QIC standard, thus allowing it to take advantage of tape-drive software for DOS, XENIX, OS/2, and Novell operating systems. The drive comes in a 5¼-in. form factor, which can be an add-on for the IBM PC/AT and PS/2 computers or as an internal unit for IBM PC/AT compatibles. $2000.

Alliance Technology Inc, 510 Lawrence Expressway, Suite 210, Sunnyvale, CA 94086. Phone (408) 727-6200.

Circle No 389

I/O BOARD

- *Analog and digital I/O for single-height VME Bus systems*
- *Allows you to implement self-test and calibration routines*

To provide both analog and digital I/O facilities, the VDAD single-height VME Bus board has 12-bit A/D and D/A converters and 12 TTL-compatible bidirectional digi-

tal I/O lines. The A/D converter has 16 input channels and operates at conversion times between 7 and 25 μsec. You can initiate A/D conversions via software commands, an external trigger input, or an on-board 24-bit timer. The D/A converter has four output channels and a control register that has a read-back capability. Two handshake lines, associated with the digital I/O lines, allow you to generate system interrupts on external events. The board includes signal-switching facilities that allow you to implement self-test and A/D calibration routines. It interfaces to a range of signal-conditioning modules. The VDAD board is available partially populated, minus the A/D or D/A converter. From DM 950 to DM 1900 (OEM qty).

Pep Modular Computers GmbH, Am Klosterwald 4, 8950 Kaufbeuren, West Germany. Phone (08341) 81001. TLX 541233. FAX (08341) 40422.

Circle No 390

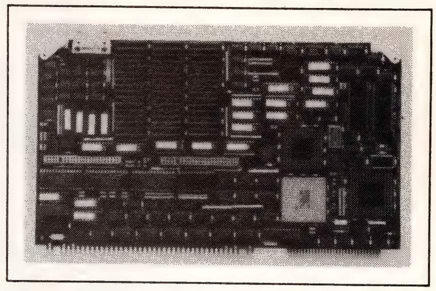
Pep Modular Computers Inc, Carnegie Office Park, 600 N Bell Ave, Pittsburgh, PA 15106. Phone (412) 279-6661. TLX 6711521.

Circle No 391

MULTIBUS I SBC

- *Has a 20-MHz 80386 CPU and 1M or 4M bytes of dynamic RAM*
- *Uses 4 double-word interleaved memory banks*

Software- and hardware-compatible with Intel's 386/3X Series Multibus I boards, the CD21/8386 single-board computer features a 20-MHz 80386 CPU and 1M or 4M bytes of dual-port dynamic RAM. It employs 4 double-word interleaved banks of RAM to reduce wait states and eliminate the need for cache memories. The board also contains sockets for an 82380 DMA controller, an 80387, and a Weitek 1167 math coprocessor. You can use either or both the 80387 and the Weitek coprocessors. The board can communicate with external devices through an RS-232C port or two SBX connectors. It contains all the Multibus interface logic required to operate in a multimaster system. A software monitor performs system tests, bootstrap-loads the operating system, and performs debug functions. Since the board can accept 256k-, 1M-, or 4M-byte dynamic RAMs, it can have as much as 16M bytes of memory. 4M-byte version, $5900. (100)



Central Data, 1602 Newton Dr,


UL TYPE CL2
UL TYPE CL 2
UL TYPE FPL

Champaign, IL 61821. Phone (800) 482-0315; in IL, (217) 359-8010. FAX 217-359-6904. TWX 910-245-0787.

Circle No 392

ACQUISITION SYSTEM

- *Has a 12-bit A/D converter for the Macintosh II and SE*
- *Also has two 12-bit D/A converters and 16 digital I/O channels*

The MBC-625 data-acquisition system for the Macintosh II and SE computers consists of a Nubus plug-in board that can accept daughter boards and an expansion system for the Macintosh SE. The system provides 16 single-ended or 8 differential input channels, a programmable gain instrumentation amplifier, a 12-bit A/D converter, two 12-bit D/A converters, 16 digital I/O channels, and three counter/timer channels. The A/D converter has an accuracy of 0.02% for a ±10V full-scale input voltage and has a conversion time of 5 μsec. The system throughput is 142 kHz. The plug-in board accepts as many as three plug-in boards for further system expansion. The SE expansion system consists of an enclosure with the plug-in board, a separate enclosure for the power supply, and a bus-extender board and interface. Data-acquisition plug-in board, $1290. SE expansion system, $1890.

MetraByte Corp, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. TLX 503989.

Circle No 393

CPU CARD

- *Features NEC's 16-bit, V25 μP for the STD Bus*
- *Has two serial ports, 32k bytes of RAM, and 24 digital I/O lines*

The 9510 multifunction CPU card for the STD Bus features an 8-MHz, 16-bit V25 μP from NEC that's code compatible with Intel's 8088 μP. Other features include two RS-232C ports, 24 digital I/O ports that can drive an optical-module rack, an iSBX expansion port, an alphanumeric display port, and a matrix-type keypad port. The card has 32k bytes of RAM for program and data storage, with space available for an additional 128k bytes. Other options include a 16-bit real-time clock and a floppy-disk controller. A built-in disk operating system reads and writes MS-DOS formatted disks if you opt for the disk controller. The card comes with STD Basic III installed in 32k bytes of ROM. STD Basic's Call statement lets you run assembly language and compiled C programs. $545.

Octagon Systems Corp, 6510 W 91st Ave, Westminster, CO 80030. Phone (303) 426-8540. FAX 303-426-8126.

Circle No 394

Who offers you the broadest line of power semiconductors... Darlington, FETMOD™, MOSBIP,™ SCR/diode modules, rectifiers and thyristors?

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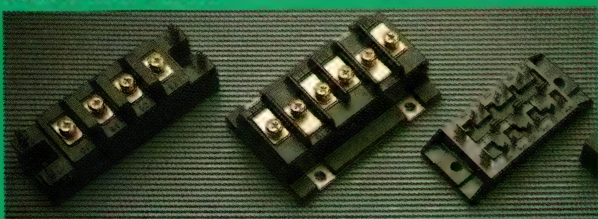
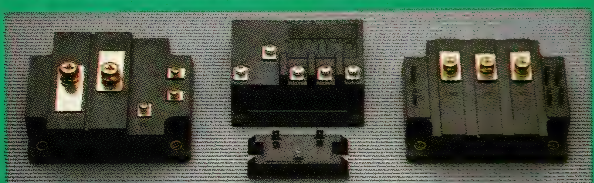
Powerex gives you what no one else does. Our one-source convenience and compatibility eliminate multi-source doubt. Our off-the-shelf availability means just-in-time delivery, instead of back-order delays or high inventory costs. We'll provide engineer-to-engineer phone conversations for an unbiased view of application needs and alternative component solutions. Best of all, POWEREX gives you leading-edge technology, rather than last-generation obsolescence. Take a look.

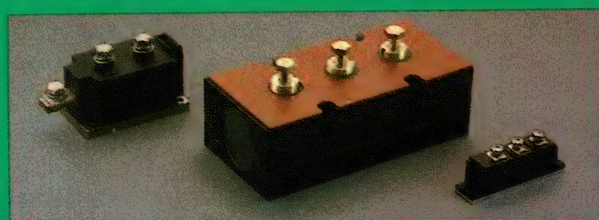


Only POWEREX offers you such a broad line of advanced power semconductor modules, including next generation FETMOD and cascade or cascode MOSBIP, rated at 8-300 A, 50-1,000 V for applications up to 100 kHz.

Only POWEREX offers you a complete line of low-power triacs and SCRs as part of the broadest line of power semiconductors available.



Only POWEREX offers you more advanced Darlington modules, including Application Specific (ASM™) modules: Single device, Phase-Leg, H-Bridge, Three Phase, Chopper and Common Emitter, 5-600 A, with $V_{CEV(SUS)}$ from 200 to 1400 V.



Only POWEREX can provide a modular solution for all the key power components from logic interface devices, input rectifiers and DC regulating components to the output power stage. POWEREX now offers the world's widest array of input power stage thyristor and diode modules. Ratings of 20-800 A, with V_{DRM}/V_{RRM} from 400 to 3000 V. Circuit configurations include Single device, Phase-Leg, Three Phase Bridge and Center Tap in common cathode or common anode configuration.

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Only POWEREX offers you all this. For product literature, call POWEREX at 1-800-451-1415, Ext. 300. (In New York, 315-457-9334.) For application assistance, call 412-925-7272, or write POWEREX, Inc., Hillis Street, Youngwood, PA 15697.

POWEREX

Joint Venture Corporation of Westinghouse, GE and Mitsubishi.

CIRCLE NO 260

Not too long ago, when people were predicting that new technologies would lead to the demise of the rotary switch, Grayhill responded by starting to re-design it for today's and tomorrow's needs. Here's what we're doing–

Process-compatible designs.

Today's technology demands process-sealing so your switches withstand wave soldering and cleaning processes. We offer process-sealed PC mount switches, single or multi-deck, with a growing range of choices of position, angle of throw, rating, circuitry and features.

More than just run of the MIL.

We've torture-tested and QPL-d them to provide the industry's broadest selection qualified to MIL-S-3786/04/13/20/35/39! Military versions are available for every major Grayhill series, ½" and 1", single and multi-deck.

Keep the quality, cut the cost.

Extensive re-tooling and retro-fitting of "old" products–extensive review of materials and methods–extensive analysis of real-world applications–allowed us to reduce cost without compromising performance. For example, we've developed still higher reliability switches with lower cost materials, where long shelf life and low cycle life are required.

Shorter lead times.

Using interlocking parts instead of insert molding is just one way we've cut the production cycle on custom switches. Your custom switches come more quickly, your standard switches virtually immediately (from local distributor stocks if you prefer).

We keep advancing the state-of-the-art.

Our rotary line is never static... see box for the latest forward development in rotary switch technology.

Grayhill makes rotary switches right and makes them easy to buy.

Technical specifications in the switch specifier's bible, the Grayhill Engineering Catalog, are detailed enough to guide you completely. Application assistance is as near as your phone, and delivery as near as your closest distributor. Call today for complete data on rotary switches for the nineties and beyond–from Grayhill!

New! Rotary encoder switch replaces dedicated keyboards and touchscreens

Combine with software as display source input to move a cursor or icon. Add push-button switch on same shaft to enter data.

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CIRCLE NO 261

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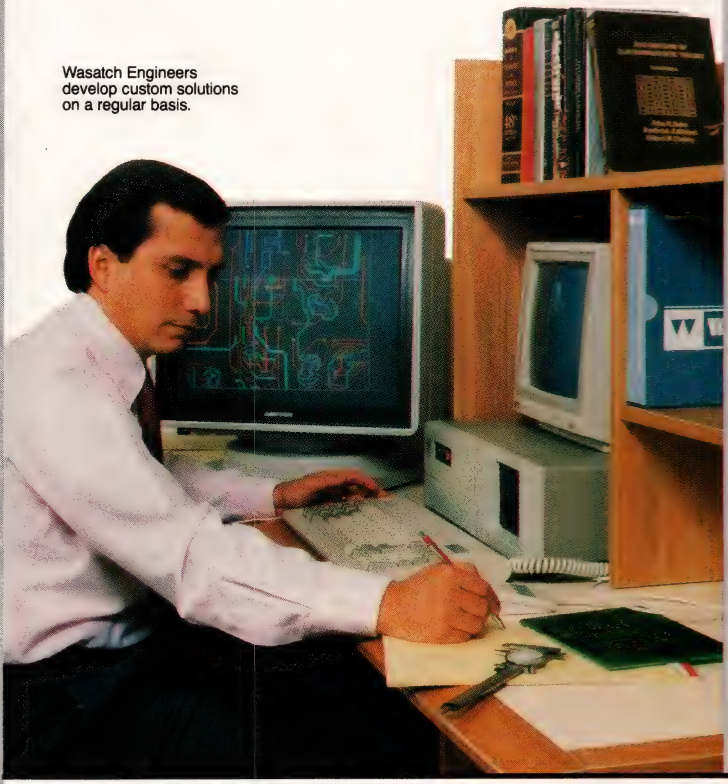

Wasatch Engineers develop custom solutions on a regular basis.

***Need A Custom Unit?...* No Problem.**

On a regular basis, Wasatch Engineers work directly with the customer to turn standard power supplies into prototypes for specific applications. And if a specific "off-the-shelf" unit cannot be modified, we'll design an entirely new unit at a very reasonable cost. So give us your idea, and watch us develop a prototype.

***Need Quick Turnaround?...* No Problem.**

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Wasatch is a company small enough to meet your needs, yet large enough to stay cost competitive. It's difficult to find a vendor that offers more power supply for your dollar.

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ACL from Philips. It's logical.

Using advances in fabrication technology, moving from six to three to one micron effective gate lengths, Philips CMOS logic now operates at speeds offered by the most advanced bipolar families, yet with all CMOS benefits.

That's Advanced CMOS Logic (ACL) from Philips. With an average gate propagation delay of 3 ns (150 MHz operation) and 24 mA output sink/source capability, Philips ACL allows designers to implement CMOS benefits across the whole speed spectrum of logic circuitry.

New pinning for a new technology.

Traditional IC pinouts, with supply pins at diagonally opposite corners, are a remnant from the days of single-sided print boards. They are inherently unsuitable for Advanced CMOS Logic, producing supply and ground noise resulting in reduction of system noise margins, loss of stored data and lower system speed. Philips ACL has multiple supply pins at the centre of each side of the package, the input pins on one side of the package, the output pins on the other side and control pins at the corners.

The result is improved system reliability, simplified design and reduced board area.

All Philips ACL ICs (74 AC/ACT 11XXX family) are available not only in 300 mil wide DIL packages but also in SO packages, so you can use surface mounting techniques to increase pcb packing density even further.

If you'd like full information on this important logic development, just contact your nearest Philips office.

For Advanced CMOS Logic, the name is Philips.

Philips Components, Marketing Communications, Building BA, P.O. Box 218, 5600 MD Eindhoven, The Netherlands. Telex: 35000 phtc nl/nl jevmc

PHILIPS

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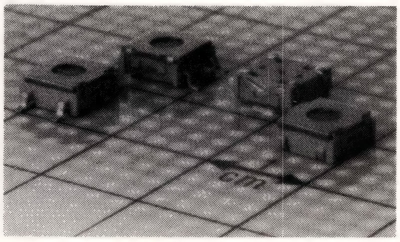


SWITCHES

- *Available with either gull-wing or J-wing terminals*
- *Compatible with all standard soldering processes*

Measuring less than 0.25 in. sq, KSC Series surface-mountable switches are available with either gull- or J-wing terminals. The single-pole, NO, pushbutton switches have actuation forces of 160 or 300g. The 160g model features a 500,000 cycle lifetime, and the 300g product features tactile feedback. The units' trapped-button design ensures that the solder joint does not fracture. KSC switches are constructed of high-temperature plastics and are fully sealed to withstand vapor-phase, infrared, and double-wave reflow soldering processes, as well as immersion cleaning operations. The switches comply with all surface-mount specifications and packaging standards. They come in thermoformed reels of 1000. The gull-wing units are packaged on 0.63-in.-wide tape; the J-wing units are packaged in 0.472-in.-wide tape. These dimensions meet the EIA and IEC requirements and are thus compatible with most pick-and-place equipment. $0.23 to $0.28 (OEM qty).

ITT Schadow Inc, 8081 Wallace Rd, Eden Prairie, MN 55344. Phone (612) 934-4400. TWX 910-576-2469. TLX 290556.

Circle No 445

SUBSTRATE

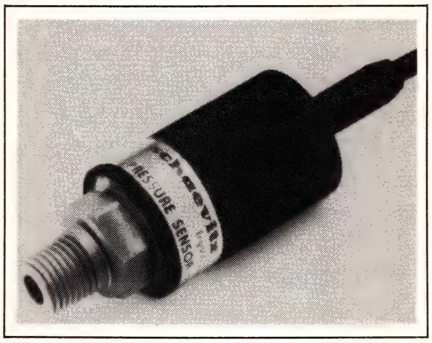
- *Solves the thermal problems of power hybrids*
- *Eliminates external heat sinks*

Designed for surface-mount applications, TI Strate is a thermally conductive substrate material that solves the severe thermal dissipation problem of power hybrids. It is constructed of a 0.62-in. metal core, aluminum base plate; a 1-oz top layer of electrically conductive copper; and a dielectric layer. The 2- to 3-mil layer of thermally conductive dielectric material provides a low thermal resistance from the

chip or package to the heat sink. A 2×2-in. substrate exhibits a 0.5 to 0.7°C/W thermal resistance while maintaining a 3-kV min breakdown strength. This conductivity is 5 to 10× greater than that of standard Kapton or FR4 substrate materials. The material also eliminates the need for external heat sinks, thereby easing the processing cycle. $0.50 to $1/in.^{2}

Texas Instruments, 34 Forest St, MS 4-9, Attleboro, MA 02703. Phone (508) 699-3800.

Circle No 446



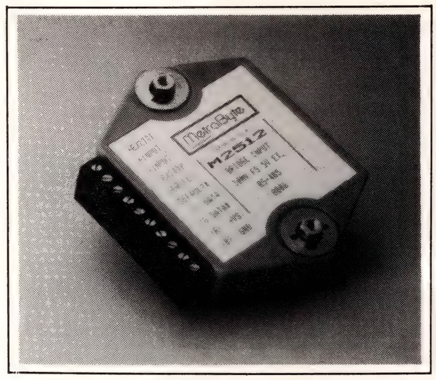
TRANSDUCERS

- *Designed for general-purpose industrial applications*
- *Possess a 10,000-psi measurement capability*

P1021 Series transducers accommodate industrial applications where solid-state devices cannot cope with the environment. An all-welded construction and a 5× overpressure protection enable the sensors to withstand high levels of shock and vibration. Available in vent-gauge, sealed-gauge, and absolute operational modes, the units range from 75 to 10,000 psi. All devices offer a combined nonlinearity and hysteresis spec equal to ±0.18% of the full-range output. The total thermal error-band accuracy measures ±1.2% of the full-range output. From $330 and $375 for gauge and absolute versions, respectively.

Schaevitz Engineering, Route 130 & Union Ave, Pennsauken, NJ 08110. Phone (609) 662-8000. FAX (609) 662-6281.

Circle No 447



CONDITIONERS

- *Provide a computer interface for a range of real-world circuits*
- *Offer both current- and voltage-input capability*

M2000 Series user-programmable data-acquisition and -control modules provide a computer interface for a range of real-world circuits. Thirty models are available for measuring voltage, current, frequency, events, and bridge circuits. All models are programmable, allowing users to scale output data in any engineeering units desired. Voltage-input models feature an input capability ranging from ±0.1 to ±10V dc. Resolution is 0.01% of FS. Current-input models have a ±10- to ±1000-mA and a 4- to 20-mA capability. Bridge- and event-input modules have input ranges of ±30 to ±100 mV and 0.0001 to 30 sec, respectively. Output data travels via standard RS-232C and RS-485 serial communication protocols. Selectable baud rates range from 300 to 38400 bps. $275 to $350.

MetraByte Corp, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. TLX 503989.

Circle No 448

SWITCHMODE SUPPLY

- *Delivers 1.5-kW output power*
- *Has power-factor correction circuitry*

The SMS-1500-00-00 single-output switchmode power supply can deliver 5V at 300A. To achieve greater output power or fail-safe operation,

110 MHz @34¢/MHz

Breakneck Performance at Breakthrough Prices

Anyone designing a 25 MHz to 40 MHz microcomputer is familiar with the three trade-offs of support logic: speed, affordability and availability.

Until now, nobody's ever solved all three at once.

The problem is that support logic has to run twice as fast as the CPU. Or the whole system slows down by a full third. Or more.

So a 33 MHz CPU needs a 66 MHz 22V10. But that doesn't exist in silicon. And CPUs just keep getting faster.

Performance	GA22V10-7	GA22V10-10
t_{PD}	7.5 ns	10.0 ns
t_s	3.0 ns	3.6 ns
t_{CO}	6.0 ns	7.5 ns
f_{MAX}	110 MHz	90 MHz
Volume Price	$37.00	$31.00

Problem solved: Gazelle's new 110 MHz GA22V10s. At great prices. In quantity.

The result?

Swifter 68030s. Extraordinary 80386s. Accelerated 88000s. Full-speed SPARC.™ Red-hot RISC. All priced competitively.

The reason?

Gazelle's GA22V10s are TTL-compatible GaAs—100% pin and function compatible with silicon. At just 34¢/MHz, they deliver the price advantage of silicon 22V10s. But at 110 MHz, they're more than twice as fast. And fast enough to outrun the fastest CPUs.

But inexpensive enough to outsmart the toughest competition.

gazelle

(408) 982-0900

Call for an information kit. Or send your name and address to Gazelle, Dept. B, 2300 Owen St., Santa Clara, CA 95054.

the power supply can be optionally fitted with active current-sharing circuitry that allows you to parallel as many as five units together. The output is fully floating, and you can adjust it in the 4.5 to 5.5V range by means of an internal potentiometer. The load regulation is better than 0.4% for a load change of 300 to 1500W, and the line regulation is less than 0.2% for a change in input voltage of 265 to 195V. The supply also features an electronic power-factor correction system that virtually eliminates quadrature current components being drawn from the line input. The output is protected against over-current and over-voltage conditions, and the power supply is protected against excessive temperature build-up. The supply has flag outputs to indicate fully operational and power-fail conditions. It also has a remote shutdown facility. The supply meets IEC, VDE, CAS, UL, and BS safety requirements, as well as international EMC requirements. Approximately $1400.

Weir Electronics Ltd, Durban Rd, Bognor Regis, Sussex PO22 9RW, UK. Phone (0243) 865991. TLX 86543. FAX (0243) 868613.

Circle No 449

Weir Inc, 418 3rd Street, Annapolis, MD 21403. Phone (301) 268-0122. FAX 301-268-7909.

Circle No 450

INDUCTORS

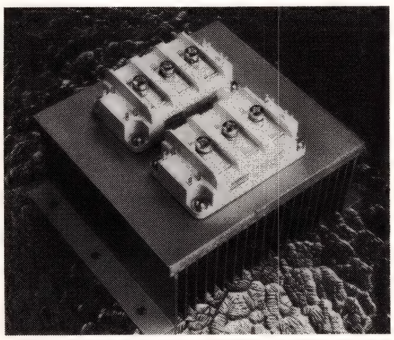
- *Features a ferrite shield*
- *Inductance values range from 1 to 1000 μH*

CS 2014 chip inductors are available with inductance values of 1 to 1000 μH. Minimum Q is 50. The inductors' magnetic shield is 100% ferrite and provides a coupling rate of only 3%. Standard tolerance is ±10% for inductance values above 10 μH. Below 10 μH, standard tolerance is ±20%, but ±10% is available by special order. Measuring $0.199 \times 0.144 \times 0.125$ in., the induc-

tors are compatible with automatic insertion equipment and accommodate both flow and reflow soldering operations. The inductors are available in both bulk and tape-and-reel packaging. From $0.50. Delivery, stock to six weeks ARO.

ICS Manufacturing Inc, 11661-F Martens River Circle, Fountain Valley, CA 92708. Phone (800) 642-2645; in CA, (800) 247-7864. FAX 714-540-8326.

Circle No 451



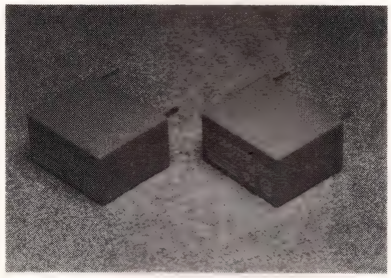
HEAT SINKS

- *Meet natural-convection and forced-air needs*
- *Accommodate all standard power modules*

Series 6760 heat sinks are designed to provide low thermal resistance in both natural-convection and forced-air applications. The units feature aluminum fins that are bonded to the mounting surface with epoxy. Available in nine standard sizes, the heat sinks' mounting-hole patterns accommodate all standard power modules. Forced-air models are designed to accept standard muffin fans with a 4.12-in.-square mounting-hole pattern. Mounting surfaces range from 7×4.78 to 16×10.78 in., and thermal resistance values range from 0.024 to 0.08°C/W. Natural-convection models are 3.13-in. high and available in 7- and 12-in. lengths. The heat sinks have a 7.375-in. wide mounting surface and are available with or without mounting flanges. Thermal resistance ranges from 0.22 to 0.3°C/W. $39.37 (100) for the 7-in. natural-convection model. Delivery, eight to 12 weeks ARO.

Aavid Engineering Inc, Box 400, Laconia, NH 03247. Phone (603) 528-3400.

Circle No 452



POWER RELAY

- *Withstands a 5000V surge*
- *Features a 1200-VA switching capacity*

Capable of withstanding a 5000V surge, the OJE miniature power relay features 10A contacts in a package measuring only 0.579×0.4×0.717 in. The relay can switch as much as 10A at 3 to 48V dc over an operating range of −30 to +80°C. Its maximum switching capacity is 1200 VA or 240W dc, and the contacts are available in 1A or 1B arrangements. Units are available with either standard or sensitive coils—450 and 200 mW, respectively. Its lifetime is estimated at 100,000 operations min at the rated load. The relay is UL recognized and CSA approved. $1.76 (1000) for a standard Form 1A version. Delivery, stock to 12 weeks ARO.

Original Electric Mfg Co Inc, 123 Linclon Blvd, Middlesex, NJ 08846. Phone (201) 271-5770.

Circle No 453

TRANSFORMERS

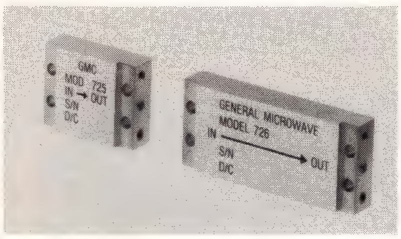
- *Available in 16-pin DIPs*
- *Plug-compatible with existing standards*

LT60XX Series pulse transformers are housed in standard 16-pin DIPs and deliver a 2000V min line oscillation for Ethernet/Cheapernet applications. Able to withstand auto-insertion techniques, the units are

plug-compatible with existing IEEE 802.3 industry standards. Other features include a 50V peak pulse-voltage rating, a 75-mW dissipation rating, and a 250-mW average power rating. Standard inductance values range from 35 to 250 μH. $3.25 (1000).

Valor Electronics Inc, 6275 Nancy Ridge Dr, San Diego, CA 92121. Phone (619) 458-1471. TLX 653406. FAX 619-458-0875.

Circle No 454



LIMITERS

- *Handle 100W peak input power*
- *Meet MIL-STD-883 requirements*

The units in this family of 1- to 18-GHz limiters are designed for low- and medium-power applications. Model 725 provides limiting for cw and peak powers of 3 and 100W max, respectively. The Model 726 is rated for input power levels of 10W cw and 200W peak. Maximum leakage power is 100 mW. Insertion loss and VSWR range from 0.7 to 2.0 dB and 1.75:1 to 2.0:1, respectively. All models are designed to meet the requirements of MIL-STD-883. They are supplied in hermetically sealed packages with removable SMA connectors and operate over a −65 to +125°C range. From $300.

General Microwave Corp, 5500 New Horizons Blvd, Amityville, NY 11701. Phone (516) 226-8900.

Circle No 455

PROTECTORS

- *Provide primary and secondary data-line protection*
- *Compatible with most computers and peripherals*

The CPP52-SP and CPP52-PP assemblies are specifically designed to provide transient protection for RS-232C I/O ports fed from data lines in a protected environment. The CPP52-SP protects all 25 pins on the data-line connector and is compatible with every model of computer and peripheral on the market. The assembly provides secondary protection in an environment where all lines are contained within one building. The CPP52-PP is available in three versions: 8, 16, and 25 pin. All accommodate long-line applications where RS-232C lines run between buildings or are otherwise exposed to a harsh transient environment. The assemblies are easy to install. CPP52-SP, $44; CPP52-PP, $107.

General Semiconductor Industries Inc, 2001 W 10th Pl, Tempe. AZ 85281. Phone (602) 968-3101. FAX (602) 966-6396.

Circle No 456

PRESSURE SENSORS

- *Feature full signal conditioning*
- *Offer 0.2% full-scale accuracy*

The 142SC100D and the 142SC150D pressure sensors measure differential pressures from 0 to 100 and 0 to 150 psi, respectively. Both devices feature full signal conditioning circuitry. They offer typical accuracies of 0.2% full-scale output. Offset is specified at 1.00±0.05V, and the factory-set full-scale output span is 5±0.5V. All products are specified at a supply voltage of 8V, but you can use any voltage between 7 and 16V, since the output voltage is ra-

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CIRCLE NO 268

Plug-in power for VME!

Here's a fully featured 400-watt, triple-output power system that's configured for *direct connection* to the motherboard in your VME bus system. It's a standard MOSFET switcher that includes all the features you've come to expect from NCR Power Systems.

Switching frequency is 80 kHz, and the unit has protection against overvoltage, overcurrent, and input surges. It meets the stringent safety and EMI requirements established by UL, CSA and TUV (VDE). Packaging complies with the Eurocard standards defined in DIN-41494 and IEC-297 for plug-in attachment to the motherboard. Precise (±0.4%) line and load regulation and 75% efficiency make the unit ideal for data communications and processing applications.

Standard units can be modified by NCR for precise conformance to customer requirements.

For detailed specifications and price quotation, contact NCR Power Systems, 3200 Lake Emma Road, Lake Mary, FL 32746-3393; Telephone 800/327-7612 or in Florida, call 407/323-9250.

NCR

CIRCLE NO 270

WESCON: Booths #2815 & 16

tiometric to the supply voltage. The transducers have a −40 to +85°C operating range; compensation limits temperature errors to ±1% over −18 to +63°C. Both sensors are housed in a thermoplastic nylon case. $48 (100).

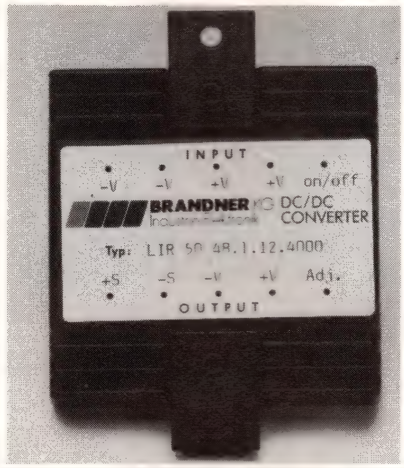
Sensym Inc, 1255 Reamwood Ave, Sunnyvale, CA 94089. Phone (408) 744-1500.

Circle No 457

DC/DC CONVERTERS

- *Operate over a large input voltage range*
- *Provide 40 or 50W output power*

LIR-series encapsulated DC/DC converters tolerate more than ±25% changes in input voltage without performance degradation. They are available for operation from input voltage ranges of 18V to 36V (24V nominal), 36V to 72V (48V/60V nominal), and 72V to 144V (110V nominal). The supplies,



which measure 76.2×76.2×17-mm (3×3×0.67-in.), are available with total output power ratings of 40 or 50W. They are available with single, dual, or triple outputs at 5, 12, 15 or 24V. All the outputs are fully regulated and can operate at ambient temperatures as high as 65°C without derating. All the outputs are short-circuit protected and start up correctly under full-load conditions. They are available with solder-pin, screw-fit, or push-fit connectors. The 40W versions are priced at around £73 to £81 (100). The 50W versions cost around £80 to £90 (100).

Brandner Vertriebs GmbH, Siemensstrasse 26, 8755 Alzenau, West Germany. Phone (06023) 330105. TLX 4188593. FAX 060234609.

Circle No 458

POWER SUPPLIES

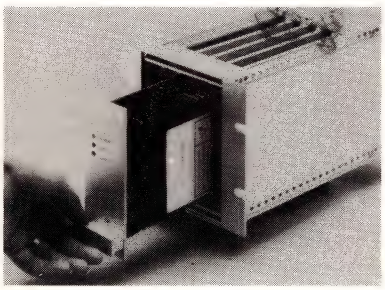
- *Designed for Eurocard/VME applications*
- *Feature a 75% efficiency*

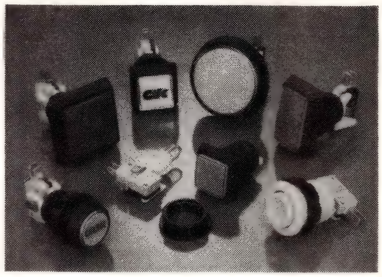
HSU Series switching power supplies are designed to mount in standard Eurocard/VME racks. The 3U package is available in 6TE, 8TE, and 10TE widths. The single-, dual-, and triple-output models in the line output 45 to 100W with output voltages ranging from 5 to 24V

dc. The switching frequency is 100 kHz and the efficiency 75%. The supplies operate from inputs of 90 to 132 or 180 to 264V ac. Line regulation is 0.4%, and load regulation ranges from 1 to 5%. Maximum noise and ripple are 2%, and transient response is less than 0.5 msec following a 50% load change. The standard operating range is 0 to 50°C. $102 to $139 (100).

Total Power International Inc, 418 Bridge St, Lowell, MA 01850. Phone (508) 453-7272. TLX 948617

Circle No 459





SWITCHES

- *Are UL recognized and CSA certified*
- *Feature 100,000-cycle lifetimes*

Available in seven illuminated and nonilluminated styles, Q Series pushbuttons feature snap-action switches. The units have a spdt contact configurations and are UL recognized and CSA approved. The contacts are rated for 21A max at 250V ac, 1 HP at 125V ac, and 2 HP at 250V ac. Full-load electrical life is 100,000 cycles. Other specifications include a $10^9\Omega$ min insulation resistance and a 1500V rms dielectric strength at sea level. Both 0.187- and 0.250-in. quick-connect terminal styles are available. Wedge-base T-3¼ incandescent lamps are supplied with either 6, 14, or 28V ratings. Lamp terminals have 0.25-in. quick-connect terminals. From $4.80 (1000). Delivery, four to six weeks ARO.

C&K Components Inc, 15 Riverdale Ave, Newton, MA 02158. Phone (617) 964-6400.

Circle No 460

ENCODERS

- *Are sealed against harsh environments*
- *Operate from a single supply*

Model H20 optical encoders are designed for the process control and factory automation industries. They feature an all-aluminum, 2-in. diameter package that includes an 80-lb load bearing. The package is fully sealed against oil and water splash.

PAPST

Choosing the right fan for your application is easy, when you choose PAPST. Simply because PAPST offers the broadest line of AC and DC tubeaxial fans in the world.

We also offer you some of the newest and most innovative. Like our new 48-volt DC MULTIFAN, our new sleeve bearing 80mm DC MULTIFAN, 6-inch DC fans with speed sensing or alarm circuitry, and our latest 25mm SLIM LINE series of AC fans.

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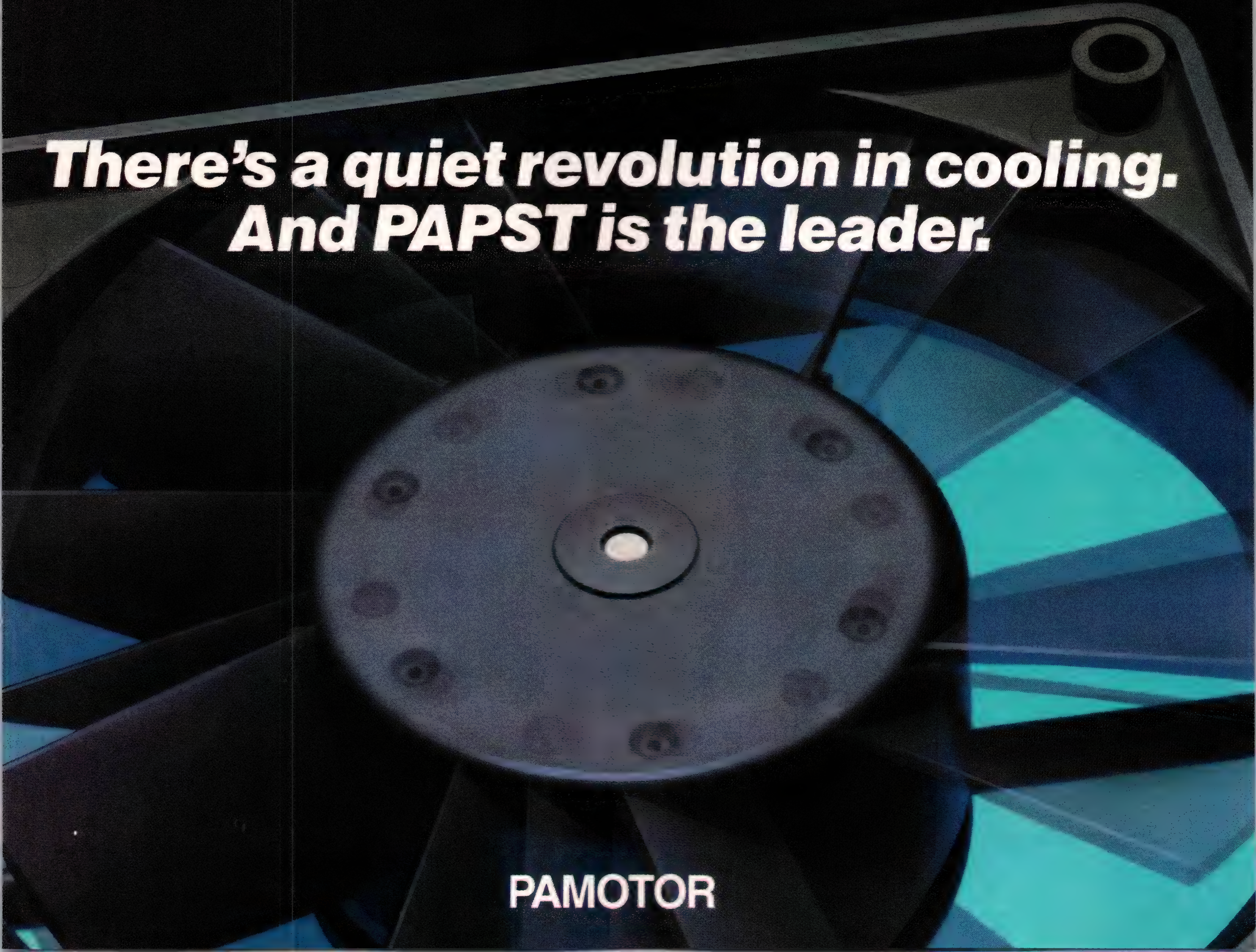
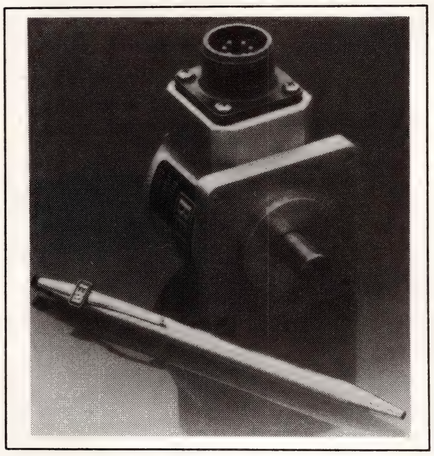
Newport, RI 02840. (401) 849-8810
Telex 952092 1-800-551-6245
(Continental USA except for MA)
1-800-262-5226 (MA only)

CIRCLE NO 271

There's a quiet revolution in cooling. And PAPST is the leader.



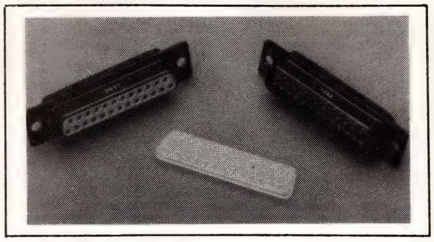
PAMOTOR



An unbreakable code disk provides as many as 600 cycles per turn (2400 counts per turn) on two quadrature channels. The encoders feature a single LED source and operate from a supply level of 5 to 24V dc. Zero index outputs are available as an option. Other options include hollow- and through-shaft versions, tethered mounting arrangements, sealed cable or environmental connectors, and a variety of mounting configurations. $100 (OEM qty).

BEI Motion Systems Co, 7230 Hollister Ave, Goleta, CA 93117. Phone (805) 968-0782. TLX 888069. FAX 805-968-3154.

Circle No 461



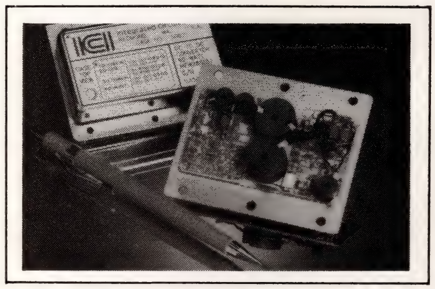
CONNECTORS

- *Feature a watertight design*
- *Available in five sizes*

These D subminiature connectors have protected, sliding spring-wire socket contacts that are pre-bent and fixed to the carrier. These features allow them to expand independently, resulting in long lifetimes. The connectors are available in 9-, 15-, 25-, 37-, and 50-position versions. Each accommodates a mix of power-, signal-, and coaxial-type contacts. The steel housing is corrosion resistant and the surface is galvanized and chromated in black. The body's polyester FR insulation material is equipped with silicon sealing plates. The contacts are plated in accordance with MIL-G-45204. From $15.40 for 9-position units. Delivery, four to six weeks ARO.

Carrot Components Corp, 750 W Ventura Blvd, Camarillo, CA 93010. Phone (805) 484-0540. TLX 181095. TWX 910-336-1237. FAX 805-987-5062.

Circle No 462



DC/DC CONVERTERS

- *Offer as many as three outputs*
- *Feature hermetically sealed metal packages*

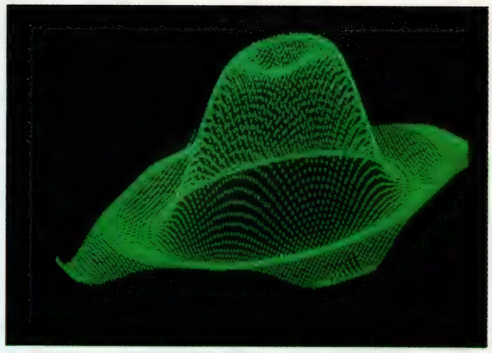
MFW Series 70W dc/dc converters are available in single-, dual-, and triple-output versions. They accept inputs of 19 to 40V (28V nominal) and provide outputs of 3.5, 5, 12, and 15V. All converters are offered in hermetically sealed metal packages that measure 1.77×3.08×0.55 in.—resulting in a 23W/in.^{3} power density. The operating range spans −55 to +85°C. Additional features include full input/output isolation, internal filtering, short-circuit protection, external synchronization capability, and an inhibit function. Environmental screening to MIL-STD-883 is available as an option. $695 to $795 (100). Delivery, stock to 12 weeks ARO.

Integrated Circuits Inc, Box 97005, Redmond, WA 98073. Phone (206) 882-3100. TWX 910-443-2302.

Circle No 463

VF Technology... The Bright Decision

Futaba, a world leading manufacturer of vacuum fluorescent displays, offers a wide assortment of *display tubes* in many sizes and formats. Also, Futaba offers *display modules* with all the electronics required to refresh the display and easily interface with host system.



GRAPHIC DISPLAY

Both front glass phosphor, which provides maximum viewing angle and uniform surface appearance, and conventional back glass phosphor, with optimum brightness and software dimming capabilities, are available. All Futaba graphics modules offer complete drive electronics, bit mapped control with a DC/DC converter. All active components are surface mounted onto a single board.

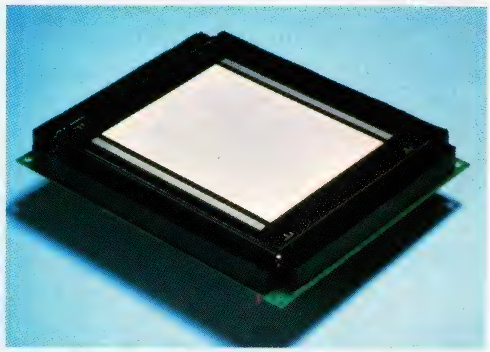
DOT MATRIX MODULES

Utilizing Futaba's dot matrix displays, a completely intelligent line of "dot modules" is available. Each includes all drive, power supply and microprocessor components surface mounted onto a single board. Surface mounted technology results in higher reliability and allows for a smaller overall package and lower cost. All dot modules require only a 5V DC power source and can accept parallel or 8 possible serial baud rates.

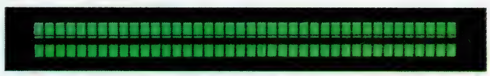
GRAPHIC DISPLAYS/MODULES

Futaba Display	Futaba Module	Pixels (Row X Char.)	Brightness (FT-L)	Module Dimensions (in.)
GP1013A	GP1013A02	64X34	200	3.35X2.95X0.7
GP1005B	GP1005B03	128X64	400	7.28X3.35X1.77
GP1010B	GP1010B01	176X16	200	7.32X2.16X1.70
GP1009B	GP1009B03	240X64	200	6.2X2.76X1.57
GP1006B	GP1006B04	256X64	200	9.84X3.35X1.77
GP1002C	GP1002C02	320X240	100*	7.10X6.30X1.60
GP1018A	GP1018A01	400X240	40	7.10X6.30X1.61
GP1004C	GP1004C03	640X400	30	9.65X7.3X1.85
GP1019A	GP1019A03	640X400	35	7.10X6.70X2.56

*Different Versions Available



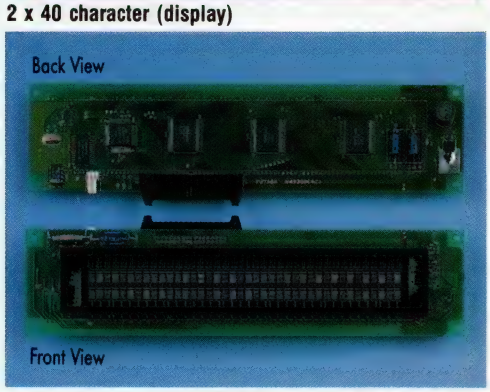
Compact, flat panel graphic displays and modules present clean, sharp images, whether for text or full graphics application.



2 x 40 character (display)

DOT MATRIX/CHARACTER DISPLAY MODULES

Futaba Display	Futaba Module	Char. X Row	Dot Format	Char. Ht. (in.)	Module Dimensions (in.)
16LD03G	M16LD03B	16X1	5X7	0.433	8.90X1.95X.98
16SY03Z	M16SY03B	16X1	14 SEGMENT ALPHANUMERIC	0.200	4.92X1.32X.83
20SD01Z	M20SD01	20X1	5X7	0.200	6.3X1.97X.75
20SD42Z	M20SD42	20X1	5X12	0.344	7.1X2.16X.88
40SD02Z	M40SD02	40X1	5X7	0.200	9.45X2.16X.88
40SD42Z	M40SD42	40X1	5X12	0.344	9.45X2.16X.88
202SD03Z	M202SD03	20X2	5X7	0.200	6.7X2.56X.90
402SD04Z	M402SD04	40X2	5X7	0.200	10.43X2.56X.90
MANY OTHER DISPLAYS	NEW MODULES AVAILABLE SOON				



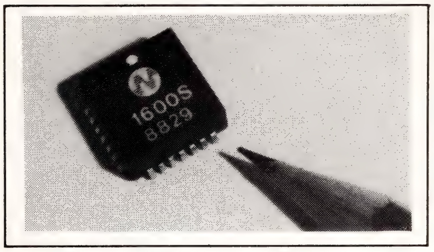
2 x 40 character (module)

Pattern flexibility and pleasing appearance are offered by Futaba in dot displays and modules.

Futaba also offers a complete catalog of alphanumeric, segmented displays.

Futaba supports its products with design engineering and system integration assistance. Call or write today.

FUTABA
Corporation of America
Electronic Components Division
711 E. State Parkway
Schaumburg, IL 60173
Telephone: (312) 884-1444
FAX: (312) 884-1635



BUS ISOLATORS

- *Provide pulse transformer isolation for LANs and buses*
- *Available in surface-mount packages*

Suitable for surface mounting, 1600 Series bus isolators for Cheapernet, token-ring, and other networks are packaged in 28-pin J-lead plastic leaded-chip carriers. They are available with isolation voltage ratings of 500 or 2000V rms. In conjunction with suitable interface chip sets, you can use the isolators to implement CSMA/CD (carrier sense multiple access with collision detection) and IEEE-802.5 network nodes. The isolators for CSMA/CD networks provide isolation for the TX and RX data channels and for the CD (collision detect) channel. The isolator for IEEE-802.5 networks is a dual-channel device. In addition, a 4-channel isolator can isolate data buses, thus offering a low-cost alternative to optocouplers. £5 (100).

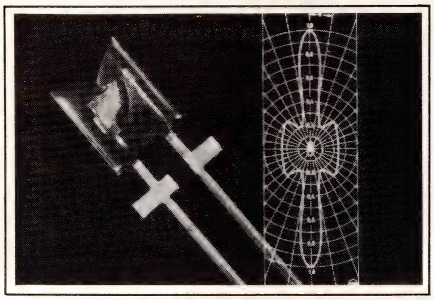
Newport Components Ltd, Tanners Dr, Blakelands North, Milton Keynes MK14 5NA, UK. Phone (0908) 615232. TLX 825621. FAX (0908) 617545.

Circle No 464

IR LED

- *Produces two separate beams*
- *Operates at a wavelength of 950 nm*

The SFH435 infra-red LED emits two diametrically opposed beams from a single GaAs chip, making it suitable for applications that would normally require two separate devices—for example, end-of-tape de-



tection in video recorders. The two beams have a half-angle of 8° and a peak emission wavelength of 950 nm. The LED is housed in a 6.4×2.5-mm oval-shaped package and produces an output power of 8 mW/sterad at a forward current of 100 mA. DM 0.90 (1000).

Siemens AG, Zentralstelle für Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

Circle No 465

Siemens Components Inc, Optoelectronics Div, 19000 Homestead Rd, Cupertino, CA 95014. Phone (408) 257-7910. TWX 910-338-0022.

Circle No 466

OPTOCOUPLER

- *Needs no power supply*
- *Operates over −40 to +100°C*

The PVI5100 optocoupler produces its output from an internal photovoltaic generator (PVG). Input current causes an optical emission from an LED to strike the PVG, thereby producing the output signal. It provides a 5V/10-μA output with a 10-mA input. The units will accept steady-state inputs of 2 to 50 mA as well as pulse inputs up to 1A. The units operate over a −40 to +100°C range. Turn-on times with loads of 10 and 1 MΩ equal 10 and 15 μsec, respectively. Corresponding turn-off times are 400 and 100 μsec. Maximum I/O capacitance equals 1 pF, and dielectric isolation specs at 2500V rms. $2.37 (1000). Delivery, four to six weeks ARO.

International Rectifier, 233 Kansas St, El Segundo, CA 90245. Phone (213) 607-8869.

Circle No 467

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toughest microcircuit prob
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NAVY
763

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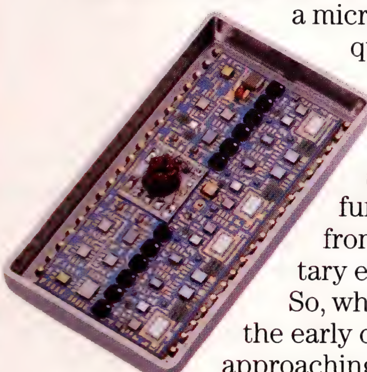
Our products range from custom hi-rel hybrid microcircuits, to Standard Electronic Modules (SEMs) in high-density configurations, to miniaturized subsystems for military and space applications. We have in-house hybrid and monolithic design, manufacturing, and technology expertise to convert the toughest requirements into high-performance microcircuits.

And we've used our experience to build a host of standard circuits. These pre-engineered "off-the-shelf" packages include MIL-STD-1553 standard data bus products, and MIL-STD-1397 interfaces.

One new standard product is the CT2100, a microprocessor controlled, quad solid state relay, with 1500 volt isolation. The circuit incorporates fully isolated switch status and built-in test functions, and operates from -55 to + 125°C in military environments.



So, whether your project is in the early design stage or is approaching production, call on CTI. Solutions to some of your requirements may have to be invented. Others may already be on our shelves. We offer you the advantage of either—or both. Call or write us today.

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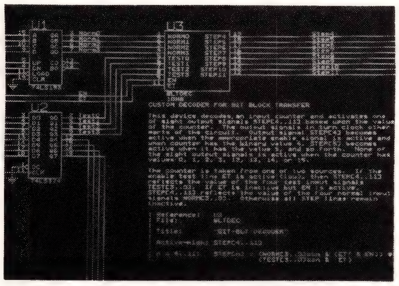
CIRCLE NO 278

NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS



PLD SOFTWARE

- *Generates JEDEC file for device programming*
- *Automatically creates combinational logic test patterns*

OrCAD/PLD allows you to store equations, state-machine procedures, and text describing the logic in a specific device next to its symbol on the schematic. If you make subsequent design changes to the PLD's internal logic, the changes will be reflected in the documentation next to the device symbol on the schematic. You can define the logic, using a proprietary form of indexed equations that reduces large and complex Boolean equations to a single line. The PLD expands the indexed equation into Boolean logic, then optimizes it for the device. You can also use a procedural programming language for state machines, truth tables, Boolean equations, and schematic symbols to define the PLD. The OrCAD/MOD optional utility for the company's digital simulation software can read JEDEC files and thereby create simulation models of the PLD. You can then exercise the PLDs with the other components in your circuit to produce a timing-based, board-level simulation. The software comes with more than 200 full-specification timing models, but also allows you to develop your own models if needed. $495 each.

OrCAD Systems Corp, 1049 SW Baseline St, Suite 500, Hillsboro, OR 97123. Phone (503) 640-9488.

Circle No 397

PC-BOARD DESIGN

- *High-speed graphics*
- *Draws smooth curve traces of arbitrary shapes*

Master Designer II release 4 has added features to address the needs of analog designers. In addition to using a display-list processing technique to speed graphics processing, you can specify components lying on a critical path and component grouping information, which must

be maintained through the layout process. You can create smooth curve traces, and curved and irregularly shaped power and ground planes. Release 4 also provides a feature known as polygon pouring, which lets you create shielding ground planes automatically by filling areas between existing signal traces with copper. Another feature called trace plowing allows you to run a trace through a previously defined polygon, while the program automatically creates the required trace spacing. You can also nest your curve traces with the trace-hugging feature. Jumpers are available as components to allow you to jump traces on single-sided or very complex boards while maintaining connectivity. Automatic stringer generation simplifies routing to SMT components. Release 4 includes interactive pc-board layout and schematic-capture software with full forward and backward annotation, a 6000-component library, and a bidirectional graphics-to-ASCII interface called PDIF (P-CAD Design Interchange Format). $8495.

Personal CAD Systems, 1290 Parkmoor Ave, San Jose, CA 95126. Phone (408) 971-1300.

Circle No 398

REAL-TIME 68030 OS

- *Features prioritized tasks and fast context switching*
- *Provides direct access to interrupts*

Regulus/68030 is a real-time, Unix-compatible operating system for computers based on the Motorola 68030 32-bit μP. The OS supports all system calls and kernel features of Unix System V; the real-time features include prioritized tasks, fast context switching, efficient intertask communications, contiguous files, and direct access to interrupts. Typical real-time latency is 380 μsec on a 20-MHz 68030 with no wait states; the latency includes the disabling and servicing of an interrupt, task scheduling, and task switching. Object-code license fee, $7500 (10).

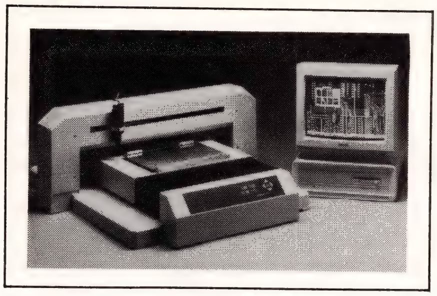
Alcyon Corp, 6888 Nancy Ridge Dr, San Diego, CA 92121. Phone (619) 587-1155. FAX 619-587-9968.

Circle No 399

PC-BOARD CAD

- *Allows you to design, etch, and drill your own pc boards*
- *Includes automatic via generation and an autorouter*

The Versatron-2000 pc-board CAD system not only allows you to design double-sided pc boards, but it also allows you to etch and drill your own prototype boards. The CAD system is based on a dedicated 16-bit color graphics computer with 1.2M bytes of RAM. It features



high-speed redrawing of any part of the layout, labeling of component pads, dynamic rubber-banding, and automatic generation of vias when you move tracks from one side of the board to the other. The system also has a multipass autorouter that in many cases is capable of 100% routing. You drive the system using a mouse and pop-up screen menus. To increase speed, the system runs entirely in RAM, only requiring disk storage to access component libraries and to store completed layouts. In addition to generating normal hard-copy plots, the system plotter can also plot the track layout directly onto a copper-clad pc board ready for etching. By replacing the plotting head with the drill head supplied, you can also drill the pc board. Hardware and software, £5750.

Versatronics Ltd, Mardy Rd, Cardiff CF3 8EQ, UK. Phone (0222) 770488. FAX (0222) 779295.

Circle No 400

MULTITASKING OS

- *Runs on 80386-based computers*
- *Upgraded version is compatible with DOS 4.0*

VM/386 Professional Multitasker is an operating system that runs on 80386-based computers and provides multitasking facilities. It creates a separate memory partition for each task and within that partition creates a virtual 8086-like machine to run the task. You can assign partitions that are larger than 32M bytes in size. This upgraded version is compatible with DOS 4.0 and remains compatible with DOS version 3. Other new features include support for DMA operations, allowing Bernoulli boxes and other fast I/O devices to work with VM/386; support for networking hardware from vendors such as IBM, 3COM, and Novell; and improved interrupt handling and asynchronous communications facilities. The operating system provides a separate copy of DOS, AUTOEXEC.BAT, and CONFIG.SYS for each virtual machine, so that each one can have different characteristics and start-up conditions. You can define a "hot key" that will let you switch from one application to another with a single keystroke. $245.

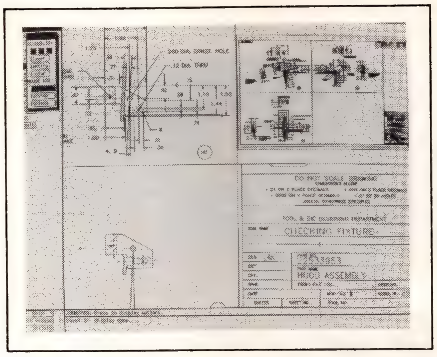
IGC, 4800 Great America Pkwy, Santa Clara, CA 95054. Phone (408) 986-8373. TLX 510-601-7773. FAX 408-986-1431.

Circle No 401

PAPERLESS BLUEPRINT

- *Provides write-protected access to design information*
- *Accepts and outputs in standard formats*

PreView allows you to communicate your design to all members of the product-process team, while maintaining document control. The team can view all sources of design information, including scanned images from paper-based drawings and documentation, CAD drawings, and 3-D models on PCs under MS-DOS or on Sun or Apollo workstations under Unix. The software lets you or your team create new views, zoom in or out, and mirror and rotate to generate different perspectives of the design. Your team can



make notations about dimensions, specifications, or questionable areas, then return a "marked up" electronic version for your review. You receive a "clear overlay" that you can view on top of the CAD database. You can also use the software to overlay two revisions of a drawing to compare them and graphically determine what changes have been made. The software accepts CAD data in either the IGES (International Graphics Exchange Specification) or standard plot file format, and it supports the MIL-D-28000 engineering-drafting application subset of IGES. PreView allows you to produce data in several different plotter and printer formats including HPGL, CGM, and PostScript, and the files are compatible with many desktop publishing packages. From $2595.

Rosetta Technologies Inc, 1225 NW Murray Rd, Portland, OR 97229. Phone (503) 626-2288. FAX 503-643-6760.

Circle No 402

DEVELOPMENT TOOL

- *Integrated development and debug tools*
- *Runs on DEC VAX and Apple Macs*

ToolWare is a completely integrated software-development and -debugging package for the 68000 μP family that runs on VAX and Macintosh hardware. The software includes a cross C compiler, an assembler/linker, and a source level debugger with a MakeFile feature that allows for quick code compila-

tion. The package gives you the ability to develop applications for the 68000, 68008, 68010, and 68020 µPs. Mac version, $2800; VAX version, $11,200.

Motorola Inc, Microprocessor Products Group, 6501 William Cannon Dr W, Austin, TX 78735. Phone (512) 440-2839.

Circle No 403

TERMINAL EMULATOR

- *Emulates multiple RTs to MIL-STD-1553A or B specs*
- *Provides BUS-65517 control from Microsoft C*

The BUS-69007 software package allows the vendor's BUS-65517 (a plug-in card for the IBM PC family) to emulate as many as 31 Remote Terminals (RTs) that meet the stringent status-response timing requirements imposed by MIL-STD-1553A or B. You can use a selection of error-injection capabilities for any of the RTs. The BUS-69007 software supports 1553A protocol applications where one or more RTs must be simulated. The BUS-69008 software upgrade allows you to bypass the menu-driven software and control the BUS-65517 card directly through a library of Microsoft C subroutines. These subroutines support 1553B applications in real time to enhance simulation and real-system emulation. You can read and modify parameters, such as data words and RT status bits, in real time without impacting message transfers over the 1553B bus. $2500 for 69007; $3000 for 69008.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600. TWX 510-228-7324.

Circle No 404

NETWORK SOFTWARE

- *Provides VME Bus systems with access to Arcnet LANs*
- *Operates at file-transfer or data-packet levels*

The NFM/ARC and VBF/ARC software drivers simplify the integration of Arcnet LAN communication facilities into VME Bus systems that run the OS-9 operating system. The software drivers operate with the company's VME Bus Arcnet interface cards. The NFM/ARC package links with Microware's OS-9/NET network-file manager to provide transparent access to remote systems. As a result, files held on remote systems appear as if they are held on a local disk. The package includes the same functions as the OS-9 disk-file manager. Operating at a lower level, the VBF/ARC software allows you to use standard OS-9 operating system calls to transfer single data packets across an Arcnet LAN and to achieve bulk data-transfer rates as high as 800k bps. The driver is supplied with Vivaway's VBF variable-

block file-manager software to provide multi-channel access to the network. NFM/ARC £85; VBF/ARC £75.

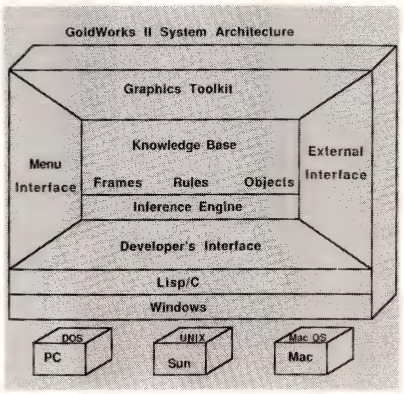
Comendec Ltd, Aston Science Park, Love Lane, Aston Triangle, Birmingham B7 4BJ, UK. Phone 021-359-0981. TLX 33435. FAX 021-359-0433.

Circle No 405

EXPERT SYSTEM TOOL

- *Runs on PCs and MAC II and Sun workstations*
- *Rule editor allows you to enter rules without syntax skill*

Goldworks II expert-system-building tool combines windows with dynamic graphics to let you build end-user interfaces without programming. Its features include a knowledge-representation system; an easy-to-use menu interface; interfaces to many conventional applications such as spreadsheets and da-



tabases; interfaces to other programming languages; and portability to PCs, Macintosh IIs, and Sun workstations. The program combines frames for representing problems, forward and backward chaining rules for reasoning, and object-oriented programming for simplifying the solution of large problems. Written in both LISP and C, Goldworks II can take advantage of the strengths of both languages. With LISP, you get the ability to use variables in your rules, an unlimited number of values in slots, an unlimited number of rules and frames, and true message passing. C offers you window systems. Goldworks II provides both a Graphics Layout Tool, which allows developers to build graphics end-user interfaces without programming, and Browsers, which provides a graphical representation of the expert system as it is being built. IBM PC/AT system requirements for Goldworks II include 5M bytes of extended memory, 15M bytes of free disk space, 640K bytes of base memory, an EGA display adapter and monitor, Microsoft Windows version 2.03 or higher, and MS-DOS version 3.0 or higher. $7500.

Gold Hill Computers Inc, 26 Landsdowne St, Cambridge, MA 02139. Phone (617) 621-3300.

Circle No 406

MAC CAD

- *Lets you transfer 2-D designs to 3-D format*
- *Gives you direct access to the Macintosh Toolbox*

VersaCAD/Macintosh version 2.0 contains substantial improvements over earlier releases of this CAD program for the Macintosh. A 3-D visualization feature allows you to transfer two-dimensional designs to 3-D format; you can then display the design using any mix of wire-frame, isometric, perspective, or hidden-line views. If you change one of these views, the program automatically updates the other views to reflect the changes. Light-source color shading provides surface-modelled renditions. The package includes three Hypercard stacks: a parametric-design stack that lets you define relationships between different views and assemblies of your design, a database stack that lets you include descriptive information about any design object, and a drawing-manager stack that produces a catalog of all the designs you have completed with the aid of VersaCAD/Macintosh. The PICT import/export feature lets you transfer designs between VersaCAD and other Macintosh applications. You can also perform the transfer by means of other standards such as IGES, DXF, and ASCII file formats. $1995.

Versacad Corp, 2124 Main St, Huntington Beach, CA 92648. Phone (714) 960-7720.

Circle No 407

TEXT PROCESSOR

- *Allows you to format raw text files*
- *Oprates under the OS-9 operating system*

Modelled on AT&T's NROFF/Unix, the TP text processor operates on 68000-family computers that run Microware's OS-9 multiuser, multitasking, real-time operating system. The package allows you to convert raw text files into formatted text suitable for output to hardcopy devices, such as daisy-wheel, dot-matrix, and laser printers, as well as photocomposers. Text-processing commands let you perform a variety of operations, including page fitting; line justification; and margin, paragraph, and title definition. The package also has more advanced text-processing commands. You can also combine commands to form command macros. $600.

EKF-Elektronik GmbH, Weidekampstrasse 1a, 4700 Hamm 1, West Germany. Phone (02381) 12630. TLX 828621. FAX (02381) 15067.

Circle No 408

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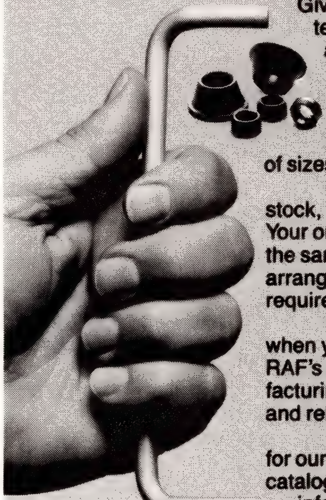

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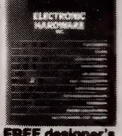

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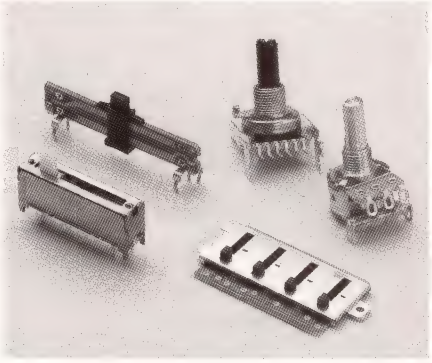

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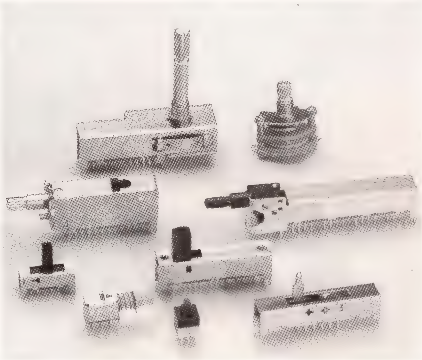


CIRCLE NO 40

OBJECT-ORIENTED C

- *Includes function and method prototyping*
- *Provides enhanced error-handling capabilities*

Objective-C version 4.0 is an object-oriented superset of the C programming language that provides type checking under programmer control and gives you fine-grained control of run-time optimization. By using Objective-C and its run time support environment, you can improve productivity and design large software systems. The support environment includes the Objective-C Compiler version 4.0, which generates C code, supports ANSI C extensions, and enables function and method prototyping; the Objective-C Interpreter version 2.0, which allows you to preprocess, compile, link, and interpret source code; ICpak 101, a set of classes that implement basic data structures; and ICpak 201, a tool kit that creates user interfaces. Versions of Objective-C are available for Sun and Apollo workstations, DEC VAX, Hewlett Packard 9000 series 200/300, and IBM PC/AT and compatibles. Prices start at $495 for the PC/AT version.

The Stepstone Corp, 75 Glen Rd, Sandy Hook, CT 06482. Phone (203) 426-1875. TLX 506127 FAX 203-270-0106.

Circle No 409

FORTRAN TOOL

- *Restructures old Fortran programs*
- *Makes programs easier to read and maintain*

SPAG, a "spaghetti-code unscrambler" that reads and analyzes old Fortran source code, produces a restructured version that's easier to read, understand, and maintain than the original version. SPAG reorders blocks of statements and produces neatly structured and indented output; it also removes almost all GOTOs and statement labels. This procedure does not change the meaning of the code or the order in which tasks are executed, but does change the manner in which the program's internal logic is represented by the source code. Associated tools are the CRAM documenter; the CMAKE tool for system building, similar to the Unix **make**; and QMERGE, a version-control tool. Versions are available for mainframes, workstations, and IBM PCs and compatibles. SPAG PC version, $1200, IBM mainframe version, $12,800; complete tool set, $1500 to $15,000.

OTG Systems Inc, Box 5250, Scranton, PA 18505. Phone (717) 343-8200.

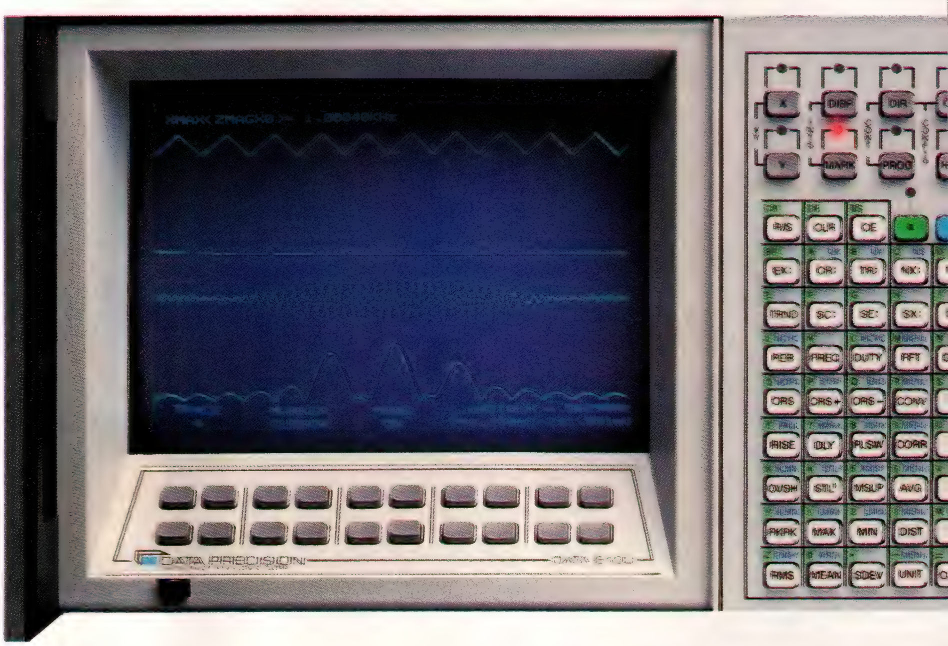
Circle No 410

FIND THE SOLUTION TO YOUR CHALLENGING SIGNAL ANALYSIS PROBLEM HERE.

(Or challenge us to come up with a solution for you).

THE INSTRUMENTS:

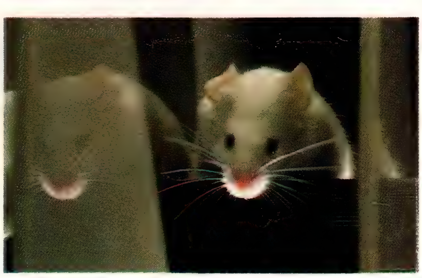
The DATA 6100 permits complex signal analysis with or without computers. You get simple one-key access to 50+ processing functions, settling time to within 0.01% of final value in less than 10 ns, rise times as fast as 350 ps and resolution to 16 bits at 100 GHz effective sampling rate. **The MODEL 2020** generates waveforms in real time, lets you add noise, glitches, simulate phase shifts or degraded rise times with front panel entry, and features a 512K output memory.



THE SUB SOLUTION:

With the 650-1 Plug-In Digitizer's true 16-bit/1 MHz resolution, the DATA 6100 can determine "Who goes there?" in the undersea environment, easily differentiating seemingly identical screw and engine noises. With more than 50 resident functions and 32,000 data point storage, analysis and retrieval of key sensor data are greatly simplified.

THE BIOMEDICAL SOLUTION:



Studies of the effect of psychotropic drugs on brain electrical activity may lead to greater understanding of the etiology of mental disorders. The DATA 6100 acquires signals from 0.5 to 100 mV with durations of fractions of a millisecond in this advanced research program. In other applications, the Model 2020's direct entry, real-time waveform generation and modification enhances analysis.

THE VIBRATION SOLUTION:

The DATA 6100's extensive frequency and time-domain capabilities excel in industrial vibration analysis, such as the automatic testing of transmissions, alternators, and fuel pumps. For example, 6 FFT input types and 18 result options speed electric fuel pump fault detection through signature analysis.

THE DISK DRIVE SOLUTION:

Disk drive performance parameters such as position error signal (PES) symmetry and seek-time errors can be rapidly and cost-effectively tested with the DATA 6100 and the 620-1 plug-in. Testing PES resonance and PES spike is equally fast and efficient. The 6100's programmability and powerful algorithms provide single-key results.

Sub photo/General Dynamics

CIRCLE NO 283

YOUR SOLUTION:

We'd like to show you how the DATA 6100/Model 2020 can meet your specific requirements. Complete and mail the coupon today for comprehensive technical data and demonstration to **Analogic, MLS-5E7, 8 Centennial Drive, Peabody, MA 01961** or call 1-800-343-8150.

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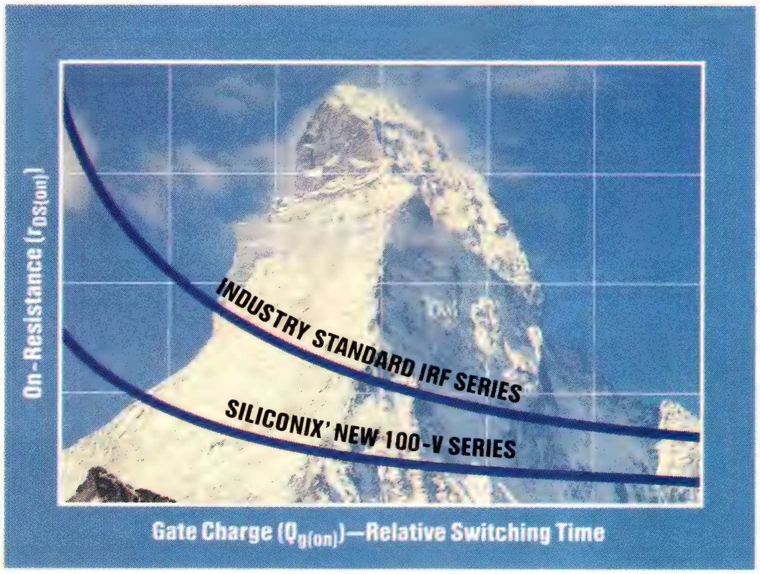

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SMP40N10	TO-220	40 mΩ	40 A	40 A
SMP30N10	TO-220	60 mΩ	30 A	30 A

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CIRCLE NO 288

TEST & MEASUREMENT INSTRUMENTS

PROGRAMMERS

- *Program pc-board-mounted devices in circuit*
- *Handle many MOS and CMOS PROMs, µPs, and PLDs*

The Boardsite 4100 and 4400 are, respectively, desktop and portable in-circuit programmers that program MOS and CMOS PROMs, EPROMs, EEPROMs, µPs, microcontrollers, and PLDs. Unlike most device programmers, these units program devices that are already mounted on pc boards. In-circuit programming, a requirement in many military applications, is more economical than traditional approaches in many commercial applications because it reduces handling of devices and the possibility of costly errors. Both instruments use an external IBM PC or compatible computer that you supply. The programmers include a high-speed expansion bus that forms the PC interface. In a departure from earlier in-circuit programmers, the vendor has devised a fixturing scheme for user pc boards that eliminates custom-designed adapters and fixtures. The products also include menu-driven software that facilitates the process of profiling the boards to be programmed. BoardSite 4100, from $9500; BoardSite 4400, $14,500.

Data I/O Corp, Box 97046, Redmond, WA 98073. Phone (206) 881-6444. TLX 152167. FAX 206-882-1043.

Circle No 415

FREQUENCY SOURCE

- *Provides 12 frequencies for telecomms testing*
- *Has selectable signal levels*

Suited for use in telecommunications testing, the LU250 hand-held oscillator generates 12 crystal-controlled frequencies at six selectable signal levels. The standard frequencies generated are 0.3, 0.5, 0.8, 1.6, 2.0, 2.4, 2.6, 2.8, 3.0, 3.3,

2.280, and 2.713 kHz. You can select signal levels of 1, 0, −4, −10, −13, or −30 dB. The company also provides alternative signal levels by special order. The instrument's output incorporates a fuse-protected coupling transformer that provides a dc path to automatically hold the telephone line. The LU250 operates from a single 9V PP3 battery and comes with a carrying case and harness. £170.

Seaward Electronic Ltd, Bracken Hill, S W Industrial Estate, Peterlee, County Durham SR8 2JJ, UK. Phone (091) 5863511. TLX 537476. FAX 091-586-0227.

Circle No 416

83C451/751 EMULATORS

- *Perform real-time emulation to 12 and 16 MHz*
- *Serially link to IBM PCs and 100%-compatible hosts*

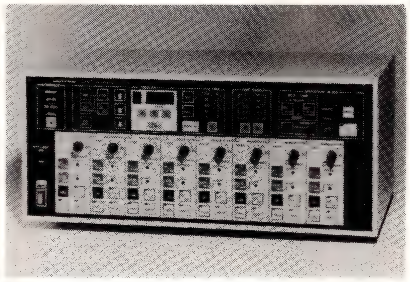
The MetaIce-83C451 and MetaIce-83C751 are in-circuit emulators (ICEs) that support the 83C451 and 83C751 microprocessors, as well as µPs for the 80C451, 87C451, and 87C751. The vendor is also adding emulators to the line that support the 80512, 80532, 80C552, and 80C652. The 83C451 and 83C751 emulators support µPs operating at clock rates to 12 MHz and to 16 MHz, respectively. Most of the models can break and trace on 16 trigger conditions. They all support full symbolic debugging with 4k frames of trace memory. Except for the -751 unit, emulation memory contains 64k bytes for the program and 64k bytes for external data. $3495 to $4995.

MetaLink Corp, Box 1329, Chandler, AZ 85244. Phone (800) 638-2423; in AZ, (602) 926-0797. TLX 4998050.

Circle No 417

TRANSIENT RECORDER

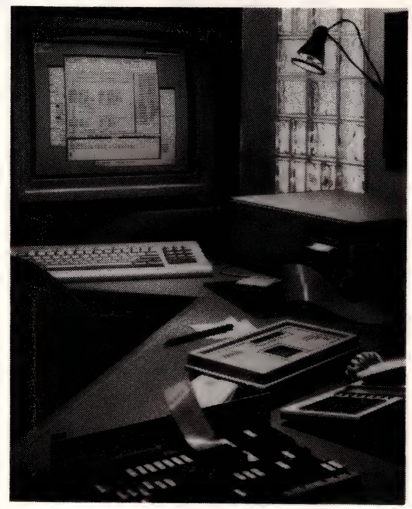
- *Has floating inputs for signals from 50 mV to 500V*
- *Stores 256k bytes/channel of 100-kHz data*



The 4400 Series data-memory system captures six or eight channels of analog-waveform data with 8-bit precision. In its standard configuration, it stores 64k samples of each channel's data, but you can expand the memory to 256k samples/channel. You can set the unit's sampling rate from 500 to 500,000 samples/sec on each channel, regardless of the number of channels in use. The output rate is a constant 500 samples/sec. The inputs are floating, and you can adjust their full-scale sensitivity from 50 mV to 500V. From $9250. Delivery, 60 days ARO.

Soltec, Sol Vista Pk, San Fernando, CA 91340. Phone (800) 423-2344; in CA, (818) 365-0800. FAX 818-365-7839.

Circle No 418



DEVELOPMENT TOOLS

- *Run on Sun workstations*
- *Debug µP systems at source and symbolic levels*

Validate/XEL is a source-level debugger; Validate/ES is a driver for symbolic debugging. Both of the tool sets, which are intended for debugging dedicated systems based on 16- and 32-bit Motorola µPs, support the vendor's ES 1800 in-circuit emulator and run on Sun Microsystems' Unix-based workstations. The hardware and the debugging tools optionally permit interfacing the emulator to the host computer via a SCSI bus that transfers data as much as 35 times faster than an RS-232C interface. The source-level debugger includes an optimizing C-

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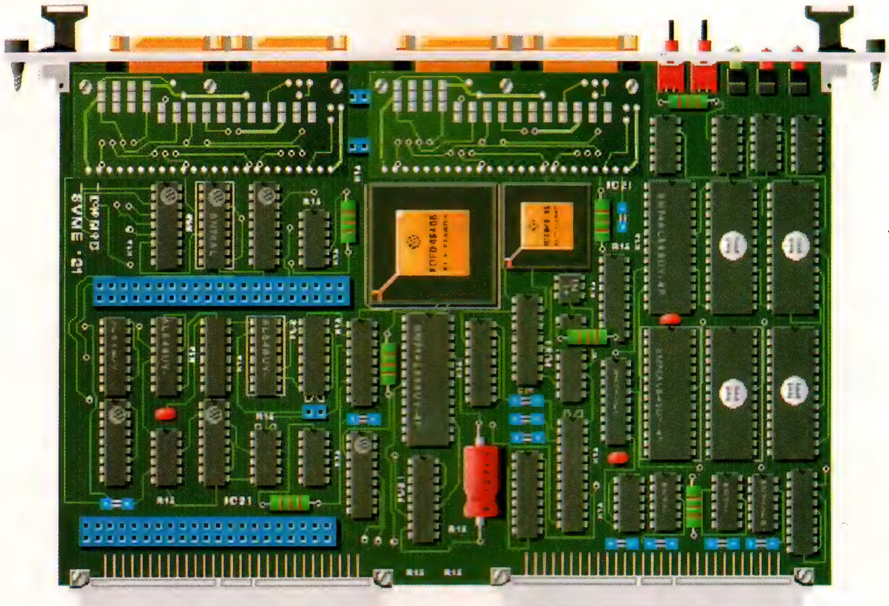

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CIRCLE NO 291

language cross-compiler. It also features emulator and simulator links that allow you to begin to debug microcode before the target hardware becomes available. Validate/XEL, from $7500; Validate/ES, $1500; SCSI option, $4500.

Applied Microsystems Corp, Box 97002, Redmond, WA 98073. Phone (800) 426-3925; in WA, (206) 882-2000. TLX 185196.

Circle No 419

WAVEFORM DIGITIZER

- *Samples two channels at once*
- *Buffers 32k or 64k 12-bit samples/channel*

The R1288 waveform digitizer is a 12-bit unit that, without multiplexing, samples two channels simultaneously at speeds from 1 to 1M samples/sec. You can control it completely via the IEEE-488 bus. It offers 32k- or 64k-byte buffers, single-ended or differential inputs, sensitivity from 10 mV to 250V p-p, and 100% pre- and post-triggering. The unit can be used with an external clock. $2995.

Rapid Systems Inc, 433 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. TLX 265017.

Circle No 420

SUPPLY TEST MODULES

- *Let you configure your own power-supply tester*
- *Use a library of over 100 test-software routines*

The Micro/OEM series of power test modules lets you configure power-supply test systems in accordance with your own requirements. The modules work with a library of over 100 test-software routines

and an automatic program generator. The software runs on IBM PCs and compatible computers. Included in the family of modules are a ripple-and-noise test unit that makes measurements to 50 MHz and a 150-MHz waveform analyzer. From $12,000. Delivery, six weeks ARO.

Intepro Systems Inc, 450 Bedford St, Lexington, MA 02173. Phone (617) 863-9500. FAX 617-861-1957.

Circle No 421

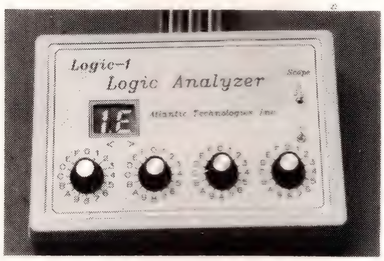
ARBITRARY GENERATORS

- *Generate analog waveforms from digital representation*
- *Have 64k and 128k point waveform memories*

The 9101 and 9109 are arbitrary waveform generators that generate analog waveforms from digital representations of the waveforms. The 9101 has a 200M-point/sec maximum clock rate, a 64k-point waveform memory, and 350k points of non-volatile storage. It can supply a maximum output of 10V p-p into 50Ω. The risetimes of output waveforms can be as short as 5 nsec. The 9109 has two channels and 128k points of waveform memory; it also has a pair of 8-bit output ports that display the digital representations of the output waveforms. Otherwise, the 9109's specs are similar to those of the 9101. A PC-based program called Easywave allows waveform creation and editing. 9101, $9900; 9109, $12,900.

LeCroy Corp, 700 Chestnut Ridge Rd, Chestnut Ridge, NY 10977. Phone (914) 578-6020. FAX 914-425-8967.

Circle No 422



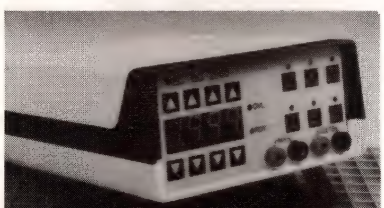
LOGIC ANALYZER

- *Displays 8-bit data*
- *Has 16 programmable trigger inputs*

The Logic 1 logic analyzer bridges the gap between simple logic probes and full-featured logic analyzers. The unit connects to the system under test, using a 34-wire cable terminated in snap-on clips. There are eight data inputs and 22 trigger inputs, 16 of which are programmable via four panel-mounted 16-position switches. When a trigger condition is satisfied, the unit displays the data at the data inputs as a pair of hexadecimal digits. An address locator lets you find problems such as infinite loops and incorrect jumps. $349.

Atlantic Technologies Inc, 600 Upland Rd, Upland, PA 19015. Phone (215) 499-7480.

Circle No 423



CALIBRATOR

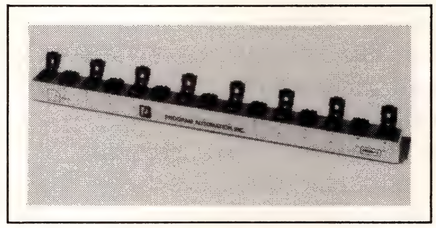
- *Offers six dc voltage and current ranges*
- *Maintains error of <0.025% of range*

The 4-lb, 7.5×5.5×2.75-in. BC-2000 voltage and current calibrator provides dc outputs with 3½-digit precision in six ranges: zero to 200 mV, 2V, 20V, 2 mA, 20 mA, and 200 mA. Maximum error is 0.025% of full-scale range on all ranges. An

LED display indicates the output value. Front-panel-mounted membrane switches let you select the range and control the output that appears on the front-panel-mounted banana jacks (one pair for voltage, another for current). Switches above and below each digit of the display let you increase or decrease the output by amounts that correspond to the digit weight. The calibrator receives power from the 115V ac line, with a 230V option available for European applications. $699.95.

Martel Electronics, 27 Roulston Rd, Windham, NH 03087. Phone (800) 821-0023; in NH, (603) 893-0886.

Circle No 424



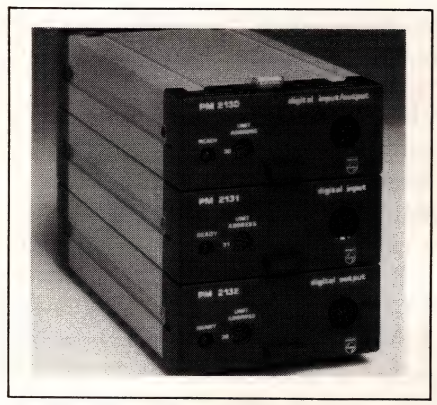
PLCC ADAPTER

- *Works with Data I/O Series 1000 programmers*
- *Allows simultaneous programming of 30 devices*

The Pasma 2 adapter lets you use Data I/O Corp's Series 1000 EPROM programmers, which normally work with DIP devices, to program LCC- and PLCC-packaged ICs in high volume. Each adapter accommodates 15 devices; two adapters can fit on the programmer. The adapter, which features pop-out ejectors, permits copying data from DIP to PLCC devices or between PLCC devices. $3800. Delivery, six weeks ARO.

Program Automation Inc, 22706 Aspan St, Suite 308, El Toro, CA 92630. Phone (714) 859-8200.

Circle No 425



GPIB I/O MODULES

- *Allow digital I/O in IEEE-488-based systems*
- *Provide optical isolation and signal latching*

The PM 2130, PM 2131, and PM 2132 are stackable, computer-controlled modules that facilitate interfacing digital input and output devices to IEEE-488-based systems. The PM 2130 offers eight input and eight output channels. The PM 2131

has 16 input channels and the PM 2132 has 16 output channels. You can set the inputs to latch data. Modules with input capability can compare their inputs to a reference data pattern that you program. If the data matches the reference pattern, the module will send a warning message to the IEEE-488 bus controller. The output lines are optically isolated and work with signal levels of either 0 to 5V or 0 to 30V; they are protected against short circuits and inductive spikes, and can control load currents as large as 100 mA. Each module, $575.

John Fluke Mfg Co Inc, Box C-9090, Everett, WA 98206. Phone (800) 443-5853, ext 77.

Circle No 426

Philips Test and Measurement, Building HKF, 5600 MD, Eindoven, The Netherlands. Phone local office.

Circle No 427

SCANNER CARD

- *Switches as many as 1000 analog-signal points*
- *Offers choice of mercury-wetted- or dry-reed relays*

The Model 7164 scanner cards contain 20 2-pole relays. The cards plug into the vendor's 705 and 706 analog-signal scanners and allow you to configure multiplexing systems with as many as 1000 differential points. You can select cards with dry-reed or mercury-wetted-reed (Hg) relays. Both types can handle a maximum signal level of 100V and can carry 1A. The dry-reed devices exhibit an initial contact resistance of 400 mΩ and have a rated life of 10^8 closures. The Hg devices maintain their 400 mΩ resistance over their rated life of 10^9 closures. Signals enter the cards via 50-pin D connectors. Dry-reed card, $395; Hg relay card, $650.

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139. Phone (216) 248-0400. TLX 985469.

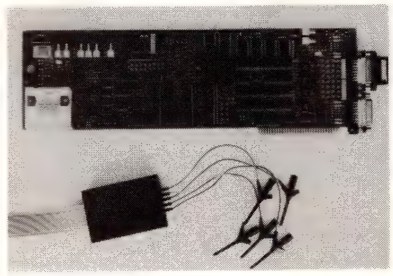
Circle No 428

LOGIC ANALYZER

- *Provides as many as 32 200-MHz logic timing channels*
- *Comprises add-in boards for an IBM PC*

The TA208 add-in board for IBM PC, PC/XT, PC/AT, and compatible computers converts the computer to a 200-MHz logic timing analyzer. Each board has eight input channels, and you can install as many as four boards in a single PC to produce a 32-channel analyzer. A coaxial connection between the

boards synchronizes their operation and allows a 32-channel setup to meet the single-board specification. The variable threshold input pods present a circuit load of 1 MΩ in parallel with 3 pF. Trace memory depth is 8k bits/channel, and the internal clock period is selectable in a 1-2-5 sequence from 5 nsec to 5 msec. As an alternative, you can



externally clock the analyzer at frequencies as high as 50 MHz. A single trigger word, in which you can specify logic 0, 1, or don't-care states, triggers the analyzer. There is also a trigger filter that you can set between 1 and 15 clock periods, and you can position the trigger point on any 512-sample boundary in the trace memory. You can display and annotate any 16 input channels on the PC, smooth-scroll through the trace memory, and make timing measurements with screen cursors. You can also store trace data on disk or dump it to a printer. The analyzer has trace search and trace compare facilities. Approximately SFr 2800.

Fast Digital Systems SA, 48 route de Divonne, 1260 Nyon, Switzerland. Phone (022) 621021. TLX 419851.

Circle No 429

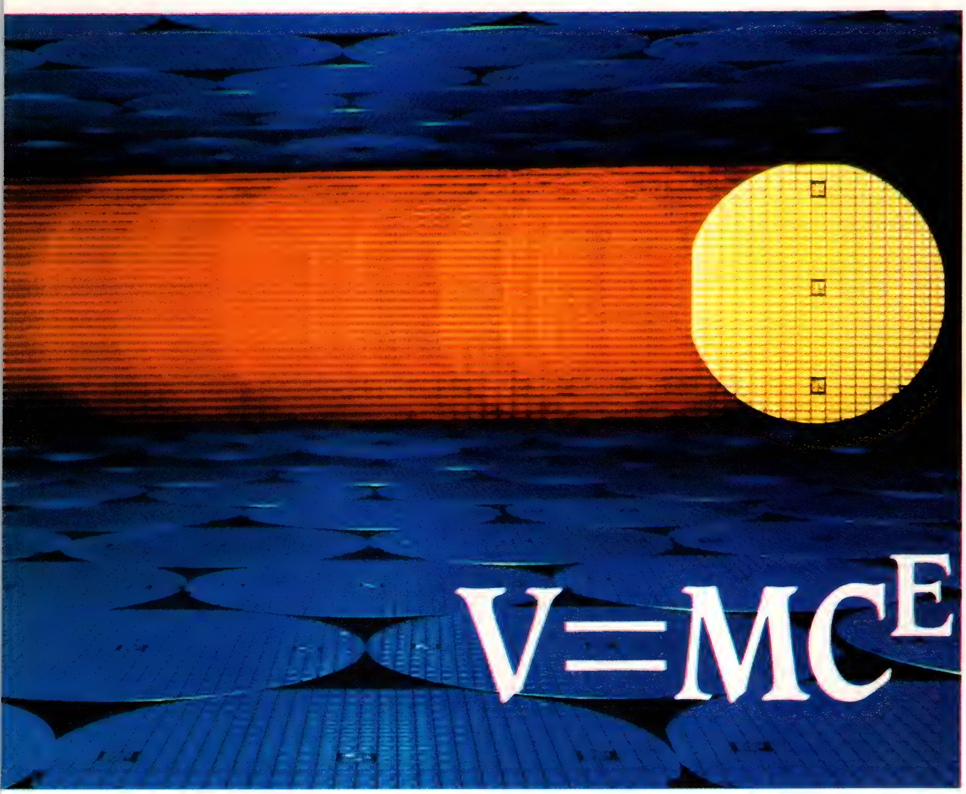
ACQUISITION BOARDS

- *Perform A/D and D/A conversion*
- *Also perform timing I/O and digital I/O*

The AT-MIO-16, AT-DIO-32F, and AT-DIO-24 data-acquisition cards work with the IBM PC/AT 16-bit bus. The AT-MIO-16 performs analog, digital, and timing I/O tasks. The vendor supplies the AT-MIO-16 with 12-bit A/D converters in three speed grades—9, 15, and 25 μsec/conversion. The AT-DIO-24 is a low cost, 24-bit-wide, parallel digital interface for use where the speed of interrupt-driven processing is sufficient. The AT-DIO-32F is a high speed 32-bit-wide digital interface that makes use of DMA. AT-DIO-24, $245; AT-DIO-32F, $595; AT-MIO-16, $1195 to $1495.

National Instruments, 12109 Technology Blvd, Austin, TX 78727. Phone (800) 531-4742; in TX, (800) 433-3488. TLX 756737.

Circle No 430

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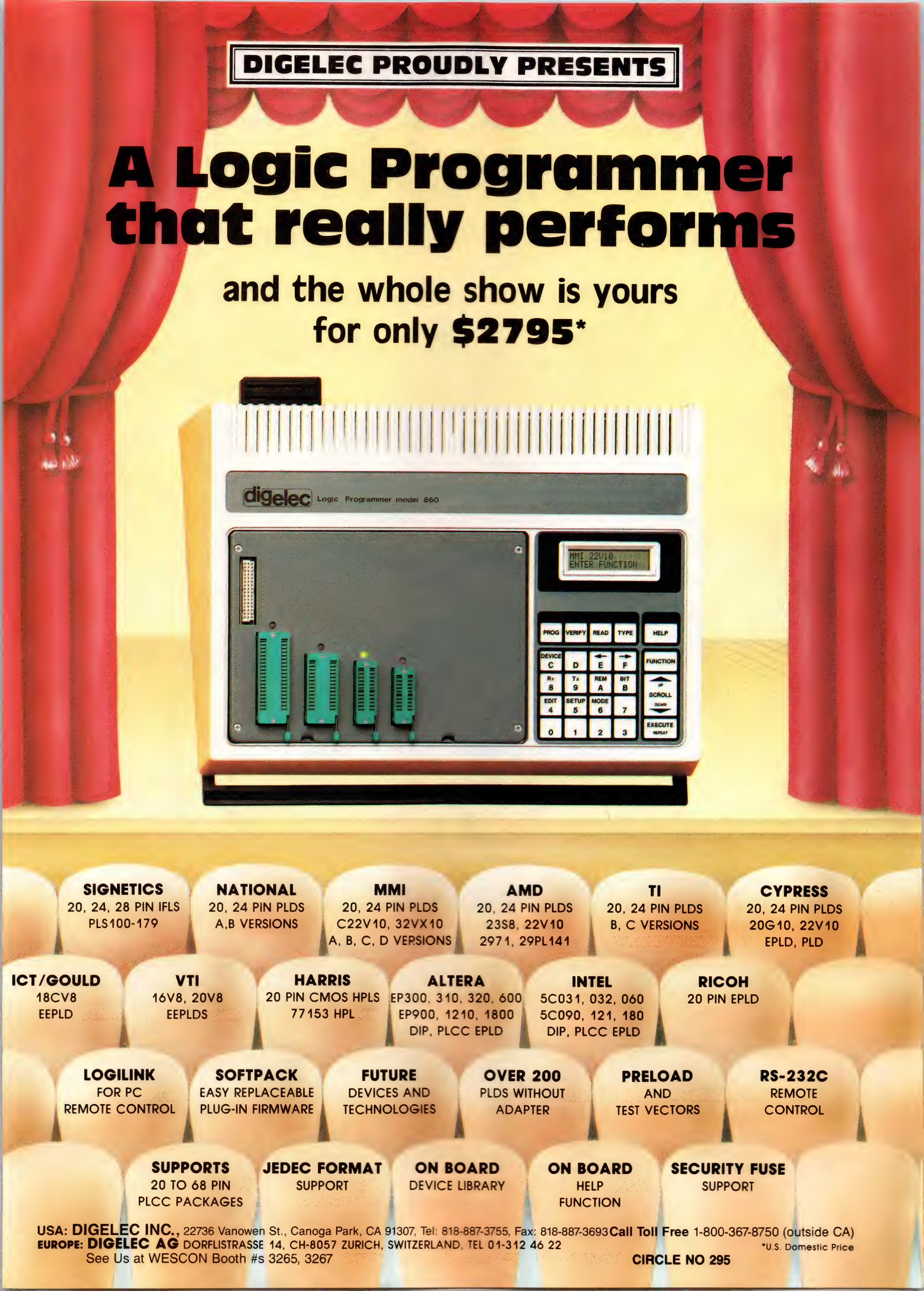
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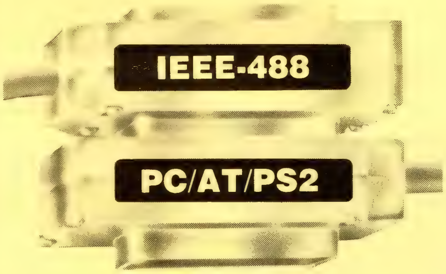

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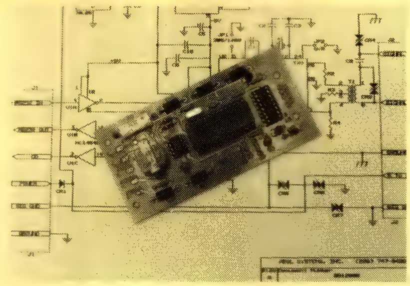

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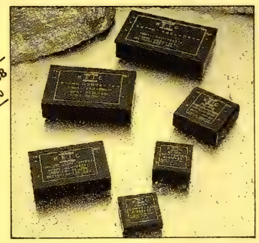

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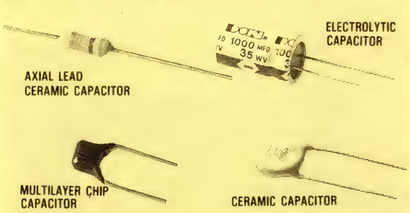

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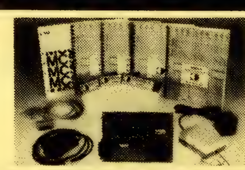

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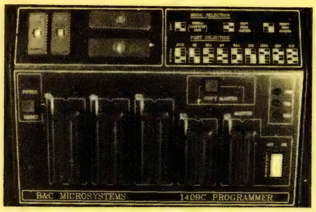

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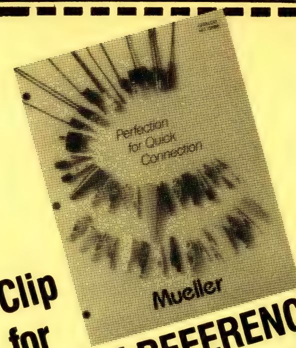

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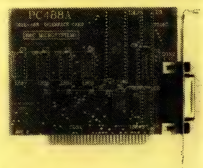

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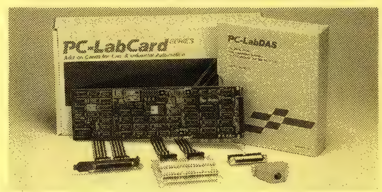

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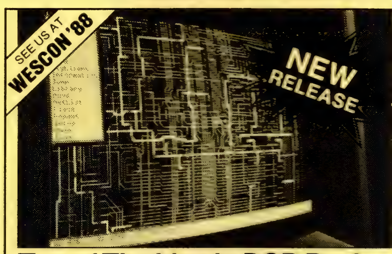

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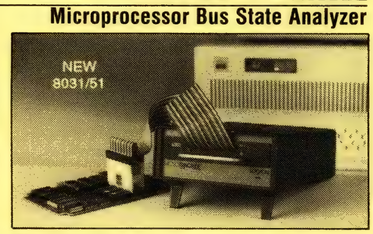

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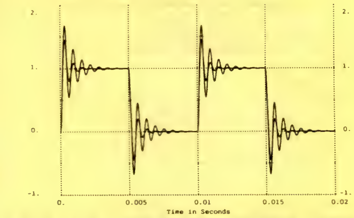

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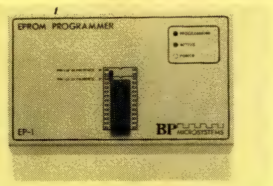

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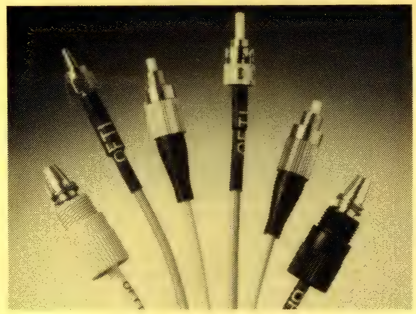

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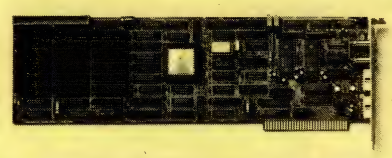

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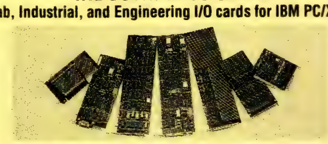

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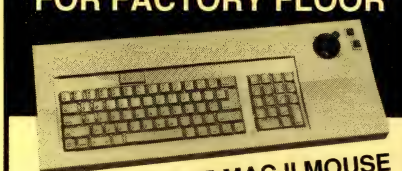

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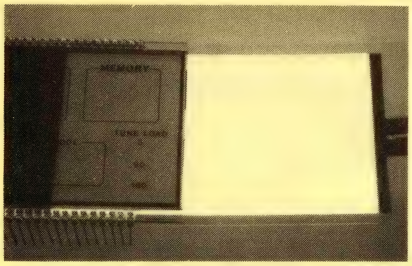

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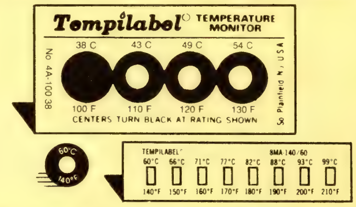

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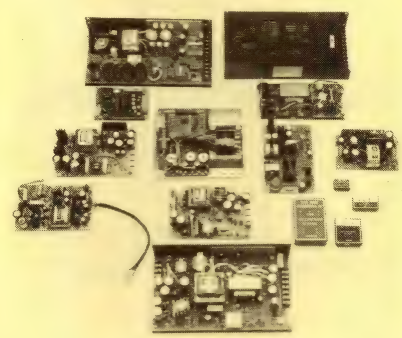

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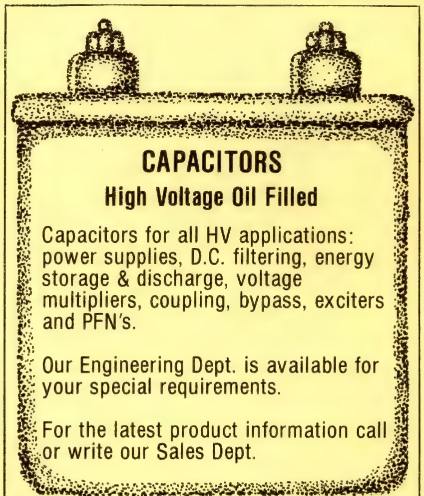

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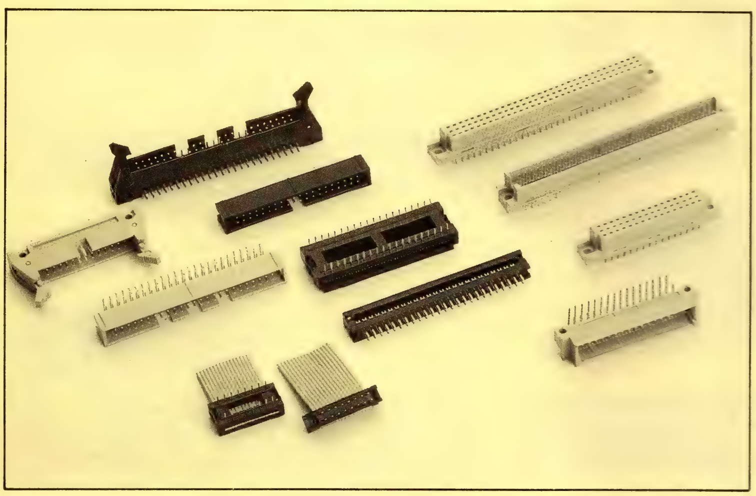

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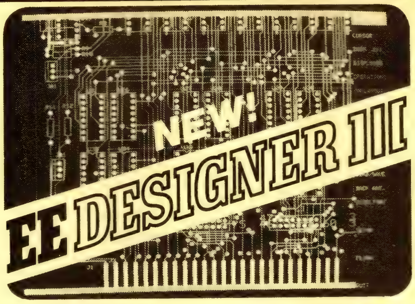

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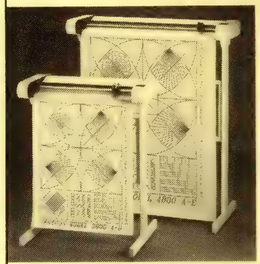

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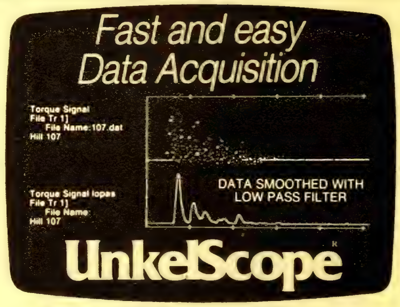

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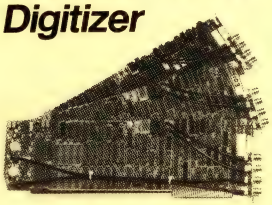

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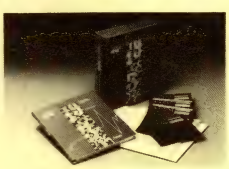

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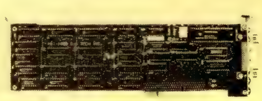

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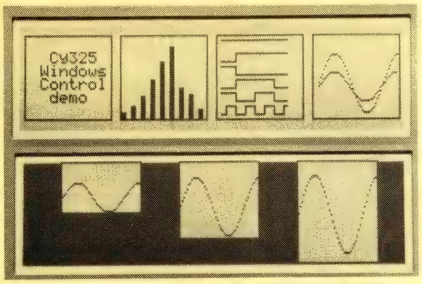

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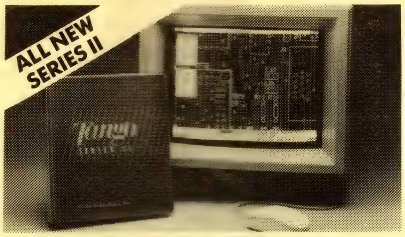

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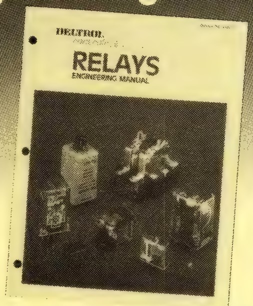

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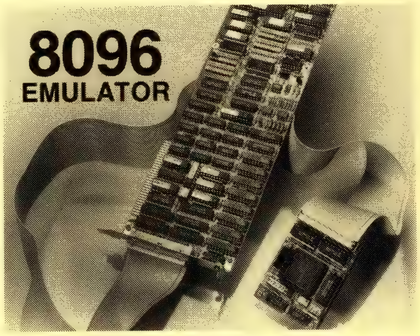

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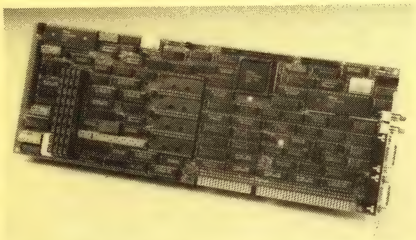

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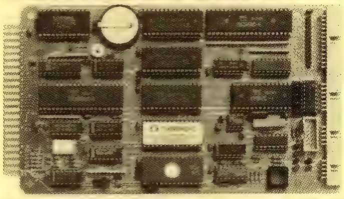

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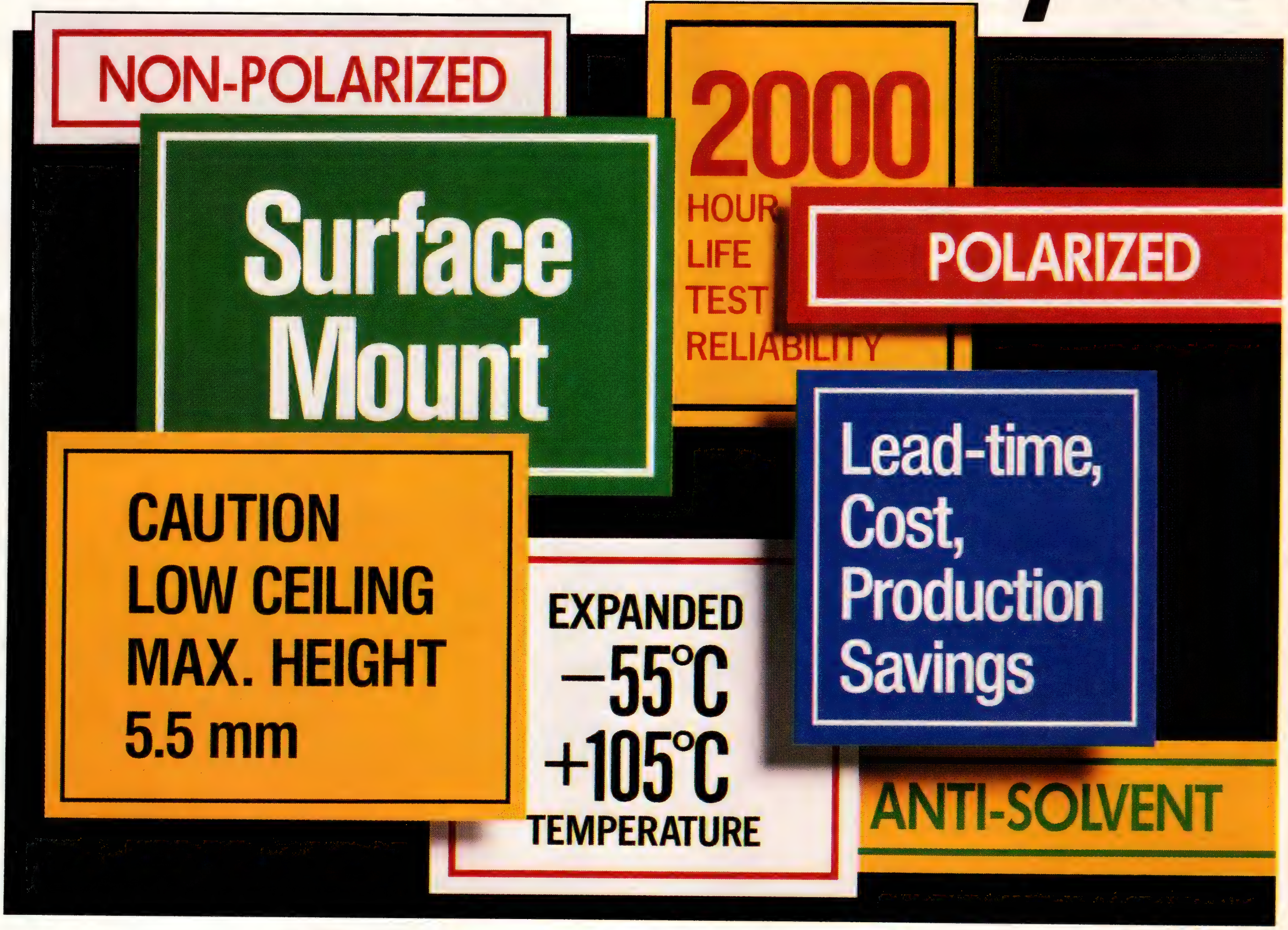

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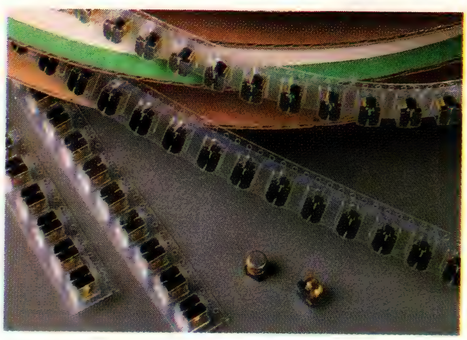
More Nichicon advantages.

Your real bottom line though is still capacitor performance. And with four tantalum equivalent Nichicon surface mount electrolytic capacitor series to choose from, your chances of finding your capacitor choice are better than ever.



SERIES	FEATURE
UP	Non-polarized/ −40°C~+85°C 6.3~50V/0.1~47μF
WX	2,000 hour life/5.5mm max. ht. 4~50V/0.1~220μF
UT	−55°C~+105°C 4~50V/0.1~100μF
MX	2,000 hour life/6.3mm max. ht. 4~50V/0.1~220μF

Of course, each series is carrier-taped and reeled and features Nichicon's anti-solvent design.

For your free Nichicon Surface Mount Electrolytic Capacitor data sheet or more information, call one of our customer service representatives at (312) 843-7500. Or, call your local Nichicon representative or distributor.

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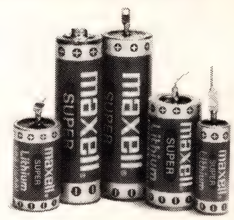

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*Recognized under the Component Program of Underwriters Laboratories.

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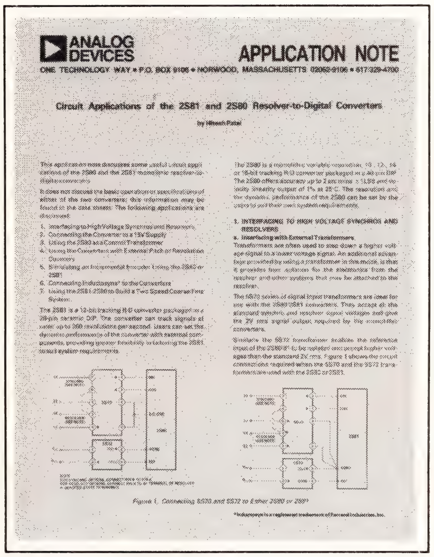
Data sheets describe simulators and accelerators

The vendor offers a set of data sheets for its testability tools, logic simulator, cosimulator accelerator, memory and logic cosimulator accelerators, and timing verifier. The data sheets present characteristics, specifications, and diagrams of the products. The publications are targeted at large-system designers working for higher simulation speed and capacity, and high testability requirements.

AIDA, 5155 Old Ironsides Dr, Santa Clara, CA 95054.

Circle No 435


ANALOG DEVICES APPLICATION NOTE

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Circuit Applications of the 2S81 and 2S80 Resolver-to-Digital Converters

by Hitesh Patel

App note explains use of converters

The 6-pg application note, *Circuit Applications of the 2S81 and 2S80 Resolver-to-Digital Converters,* explores the use of these two monolithic R/D converters. The note discusses interfacing to high-voltage synchronizers and resolvers; connecting the converters to a 15V supply; using the 2S80 as a control transformer; and using the converters with external pitch or revolution counters. Block diagrams and circuit diagrams illustrate the text.

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021.

Circle No 436

Information about coating-thickness standards

In these three pages, you can use the vendor's 7-point check list to determine whether you need recertification and replacement of your coating-thickness standards. The standards are suitable for testers operating on the eddy-current, beta-backscatter, and magnetic-induction principles. The publication lists the vendor's inventory of reference standards, which are traceable to the National Bureau of Standards. The inventory also includes certified shims for nonmagnetic/nonconductive coatings.

CMI International, 2301 Arthur Ave, Elk Grove Village, IL 60007.

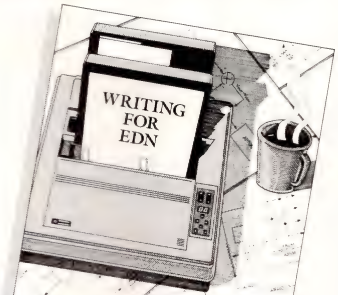
Circle No 437

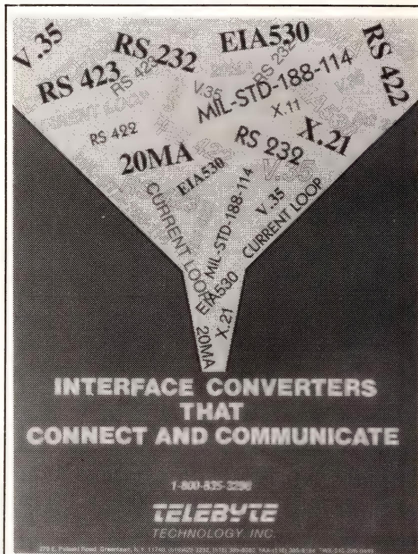
Catalog addresses users of IBM PCs and compatibles

The 164-pg *Industrial Computer Source-Book 1989* contains more than 500 IBM PC-related products used in industrial and educational laboratories, factory automation, and process measurement and control industries. According to the vendor, the publication is recognized in industry as the single source for industrial computers, data acquisition, industrial control, and communications products for the IBM PC, PC/XT, and PC/AT. The vendor has expanded the product offering to a complete line of industrial computers that includes the 9500 Industrial Tower Series, the 8500 Series of rack-mounted computers, the 7500 Series of industrial chassis, the 7500 XC diskless computer/expansion chassis, and the PC node diskless computer. The new 26-pg software section includes data acquisition, operating-system, languages, CAD, and data-analysis packages.

Industrial Computer Source, 5466 Complex St, Suite 208, San Diego, CA 92123.

Circle No 438





Interface converters categorized

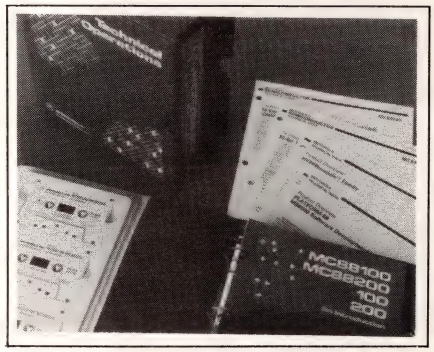
The vendor's 16-pg catalog describes 22 interface converters in an attempt to organize the overflow of worldwide interface standards,


CASIO fx-5000F
SCIENTIFIC FORMULA 128
SCIENTIFIC CALCULATOR

which include RS-422, Current Loop, RS-485, V.35, MIL-STD-188, MIL-STD-188-114, and EIA-530. The publication mentions that these converters provide an electrical transformation in terms of voltage, impedance and timing, and the mechanical hardware connector transformation. It goes on to say that, because RS-232C is the universal interface, most of the vendor's converters provide conversion from some specific interface to RS-232C, thus permitting the coupling of two converters to achieve a specific hardware conversion that may not exist as a standard product.

Telebyte Technology Inc, 270 E Pulaski Rd, Greenlawn, NY 11740.

Circle No 439



Audio cassette introduces RISC course

The M88000 family audio-cassette course, *An Introduction to the MC88100/MC88200 Reduced Instruction Set Computer (MTTA6)*, provides three tapes, containing approximately 4½ hours of material; illustrated course notes; and related support literature. The modular-formatted course material has clearly stated objectives and features exercises and evaluations for each module. The package is aimed at designers experienced in the use of 32-bit micro-, mini-, or mainframe processors. $125.

Motorola Inc, Literature Distribution Center, Box 20924, Phoenix, AZ 85063.

Circle No 440

Listings survey software funded by NASA

Describing more than 1200 computer programs, the Cosmic (Computer Software Management and Information Center) catalog offers more than 1200 computer programs, as well as services such as developing exclusive user case histories and making inquiries of key people in NASA. The publication includes a NASA update of MIMS, the Medical Information Management System developed by the Goddard Space Flight Center; Comp-Size, an analytical tool that can make a preliminary composite analysis to verify sizing choices for structural members; and Clips 4.2, the Johnson Space Center's expert system shell.

Cosmic, The University of Geor-

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The VL Series Power Supplies utilize surface mount technology. And since we now have in-house surface mount capabilities, you get the total "Made in America" quality you've come to expect from Converter Concepts, at a competitive price.

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See us at the Wescon Show, Booth #1515, 1517

CIRCLE NO 305

gia, 382 E Broad St, Athens, GA 30602.

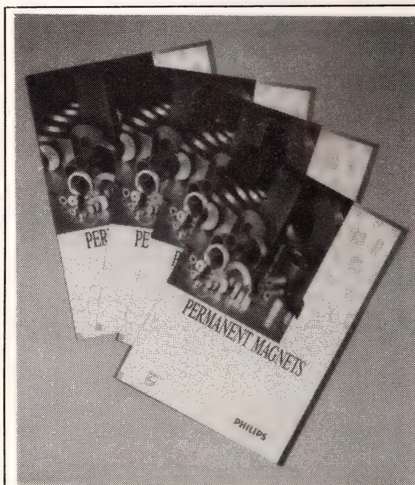
Circle No 441

Brochure describes control systems and instruments

The 40-pg product directory, *Instruments & Systems for Process Measurement and Control,* sums up an abundance of products pertaining to recorders and data acquisition; conductivity/resistivity; dissolved oxygen; process control; sodium ion; humidity; gas- and fine-particle analysis; process transmitters; temperature; and instrument test and calibration. The publication also deals with parts and supplies, and total equipment and system services. Photographs and figures illustrate the directory, and a numerical index and a listing of worldwide distributors complete the publication.

Leeds & Northrup, Mail Drop 246, Sumneytown Pike, North Wales, PA 19454.

Circle No 442



Booklet surveys permanent magnets

The vendor's 4-color, 16-pg brochure offers a wide range of permanent magnets, consisting of two major groups: hard-ferrite magnets and rare-earth magnets. The booklet presents an overview of many applications, such as automotive, consumer electronics, industrial, telecommunications, and data processing. It also reports on quality-control procedures, material specifications, customer support, and ordering information. The section on product specification briefly outlines the variety of magnet shapes and sizes.

Philips Components Div, Box 523, 5600 AM Eindhoven, The Netherlands.

Circle No 443

Ferroxcube Corp, Kings Highway, Saugerties, NY 12477.

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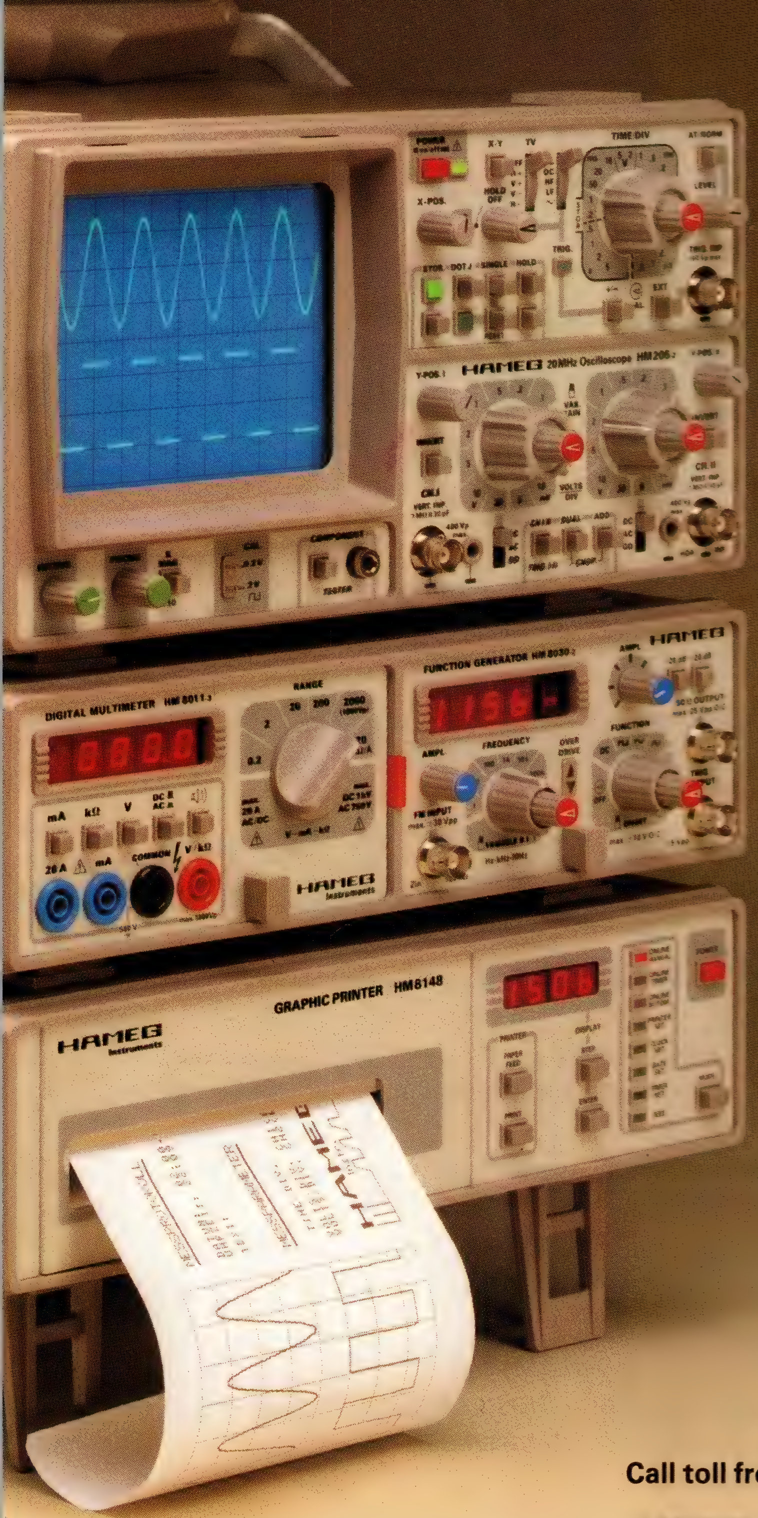

Digital Storage Scope HM 205-2:

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2.0 kV*

Metallized plastic film capacitors

4.5 kV*

Rifa metallized paper capacitors

In the power supplies or household appliances that you manufacture, RFI capacitors have two primary purposes. (1) eliminating the harmful effects of radio frequency interference, RFI. (2) protecting your equipment against transients from the mains.

In most applications, an RFI cap has to take a lot of punishment.

To define the various kinds of disturbances and irregularities in the voltage wave, UNIPEDE recently carried out an interesting survey. On two separate occasions, measurements were taken in most European countries.

The results may come as a surprise to you.

On average, the transients occur more than ten times a day, and their pulse steepness is acute, approximately 200–2,000 V/µs. Of all categories, 80 percent of the transients have a duration of 1 to 10µs, and an amplitude of up to 1,200 V.

However, transients up to 6,000 V were recorded during thunderstorms.

This is the most realistic picture so far presented of what RFI caps are exposed to, or what they are expected to withstand during the life of your product.

In many cases, the cap you choose is the determining factor for length of life.

Now, there are two primary types of RFI capacitors. (1) metallized plastic film caps. (2) metallized paper caps. Out of five major makes tested at the Rifa labs, the poorest performing samples start breaking down at 2.0 kV.

At the level where even the toughest ones give in, Rifa caps still maintain a safe margin, not starting until 4.5 kV.

QUALITY IN OUR BOOK

In our book, QUALITY means meeting your customer's performance requirements, and he certainly doesn't expect your product to break down or cause interference to radio frequencies, does he?

Rifa capacitors are made to meet the needs of practical applications, not just to come up to a standard.

So if you want all your products to perform faultlessly in any country, which capacitor do you choose?

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) Starting level for failures caused by transients

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CAREER OPPORTUNITIES

1988 Editorial Calendar and Planning Guide

EDN

Issue Date	Recruitment Deadline	Editorial Emphasis	EDN News
Nov. 24	Nov. 3	Microprocessor Technology Directory Graphics, CAE	
Dec. 8	Nov. 16	Product Showcase—Vol. I, Power Sources, Software	Closing: Nov. 21 Mailing: Dec. 15
Dec. 22	Dec. 1	Product Showcase—Vol. II, Computers & Peripherals, Test & Measurement	

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West Coast: Mary Beth West (213) 826-5818
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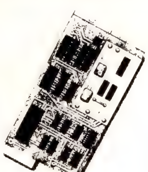

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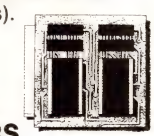
COMMUNICATIONS SYSTEMS ENGINEER

- BSEE/CS, 4+ years communications system integration and development.
- Broad knowledge of communications protocols (LAN, WAN, ISO/OSI) and systems, ability to write specifications and applications programs.

SOFTWARE ENGINEER

- BSEE/CS, 4+ years software development, communications protocol and interfaces (ISO/OSI, LANs, WANs).
- Programming micro/mini for real time, "C" and Motorola 68000/ 68020.
- Operating Systems (UNIX, VMS, MS-DOS).



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Research & Development Projects

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- Sub-Micron CMOS Transistors
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- Source, Drain and Poly Self-Aligned Silicide
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- Advanced Metrology
- Hi-Energy Implantation
- Ultra-Thin Dielectric Technology
- 3D Technology
- Zero SER Technology
- Facility Automation

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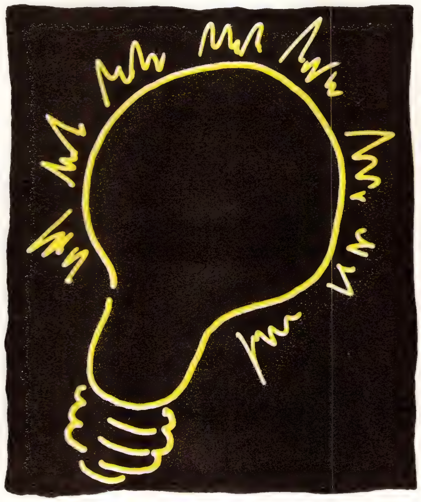
Challenge your expertise in logic design and/or microprocessor system design using flow charts and timing diagrams for digital design and detailed design analysis. Your experience should include vendor libraries, test vector generation, simulation checkout and TTL emulators for gate array standard cell design. Familiarity with CAE systems used in logic design, test vector generation, simulation checkout and documentation is also necessary. You must have five years' related experience plus a BSEE or equivalent degree. An MSEE degree is preferred.

Electrical Design Engineers

Responsibilities include development and evaluation of new mass storage products, principally flexible drives. You'll perform specification, design review, test, failure analysis and product support functions. In addition, you'll monitor as required, the start-up phase of vendors production line



to assure process controls, test capabilities, etc. Your BSEE should be complemented with five to seven years' experience.

Electrical R&D Engineers

Develop and evaluate new mass storage products, principally Winchester drives. Strong knowledge of all phases of Winchester disk drives design, especially Interface, Read/Write, Servo. Familiarity with MS-DOS, Assembly and "C," along with a BSEE and five years' experience are required.

Systems Architects

You'll design new products by investigating and evaluating system compatibility and performance of design alternatives and new technologies. You'll develop hardware compatibility tests and performance analysis tools.

Quality with a BSEE, MSEE preferred, and three years' hardware background with a knowledge of microprocessor-based systems software. In addition, experience with CPUs/Memory/Bus architecture, numeric co-processors, file subsystems, network communications, graphic subsystems and state machines is required.

Systems Software Engineers

You'll evaluate, design and develop firmware, operating systems, device drivers and utility software for PC systems. Along with your BSEE/BSCS, you'll need four years' related experience in PC software development, 8086/286/386 Assembly/"C" language programming in MS-DOS, OS/2 and/or UNIX/XENIX operating system environments.

CAE System Engineers

You'll bring on-line new design methodologies, develop and execute benchmarks and install new software/hardware. Your experience should include simulation accelerators, fault grading and scan technology, modelling techniques, and mainframe and/or super minis. Exposure to ASIC and/or UNIX environments is desirable. You'll need a BSCS or BSEE, MSCS or MSEE preferred, and five years' CAE development experience.

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Put your design and development talents to the test improving structural software. You'll help increase the reliability of personal computer systems and operating systems software. Five years' software quality assurance or test development experience should complement your BSEE/BSCS. Experience in "C" and 8086/286/386 Assembly language is essential.

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As a Compaq Packaging Engineer, you'll help improve the quality of Compaq products. You'll need a BS in Packaging Engineering or equivalent degree, plus three to ten years' experience in a computer or electronic component manufacturing environment. Your expertise should include shock and vibration testing as well as evaluation of packaging cushioning materials. International packaging and project management experience is desirable.

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- ☐ Systems Analyst
- ☐ Artificial Intelligence Engineer
- ☐ System & Unit Design Engineer

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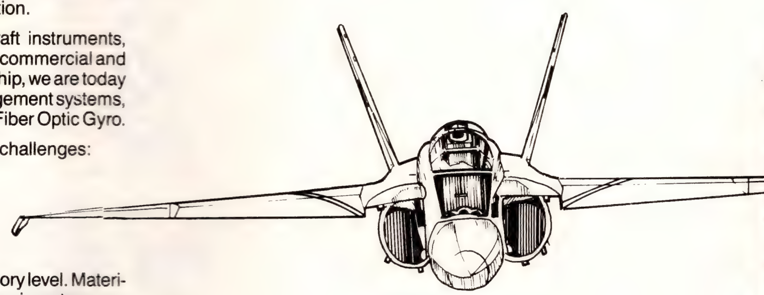
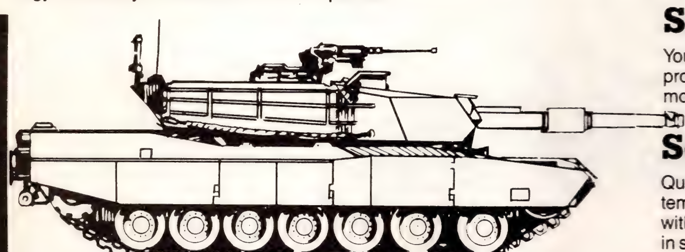


Materials Engineering Section Manager

Requires 7+ years experience, to include some at the supervisory level. Materials engineering experience in an aerospace instrument or electronic systems environment is preferred, with knowledge of printed wiring board fabrication and assembly, metal finishing, heat treatment and general metallurgy. BS in Metallurgy, Chemistry or Materials Science expected.



Structural Engineer

You will participate in on-site installation of aircraft modifications; some travel involved. Requires 10+ years structural design experience on military aircraft, including onboard cockpit design and layout. Must know MIL-STD-100 and MIL-D-1000 drawing formats and, preferably, aerodynamic/flutter and divergence analysis. Familiarity with stress and fatigue analysis, and fabrication of sheet metal assemblies also necessary. BSME or equivalent required.

Quality Engineer

Requires quality-oriented experience in hybrid microelectronic manufacturing, with knowledge of applicable MIL-Specs and Standards.

Senior Engineer/ Project Manager

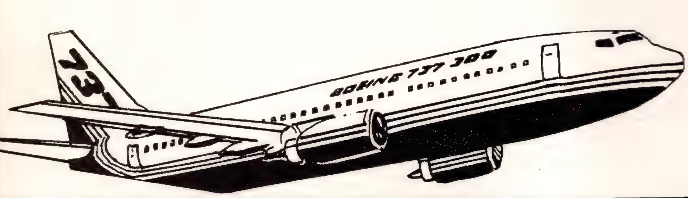
Requires a minimum of 6 years experience in project management and use of tools (Pert, Gantt, etc.) You must be familiar with advanced airborne hardware. BSEE or equivalent.

Marketing Manager

You must have experience in either marketing flight data recorders, inertial reference systems or flight management systems.

CM/DM Supervisor

Requires significant experience in data management and hardware/software configuration, as well as MIL-specs familiarity. Supervisory experience is a must; degree preferred.



Senior Manufacturing Engineer

You should have at least 5 years experience with guided wave optics and IC processing, OR in control theory with knowledge of light propagation in single mode wave guides.

Senior Data Systems Engineer

Qualifications include a minimum of 5 years experience in military avionics system design, with strong hardware and software experience. You must be familiar with MIL-490 and MIL-2167 system requirements documentation; background in structural analysis is preferred, as is the ability to formulate interface control documents, white papers, proposals, etc. BSEE or equivalent.

Mechanical Engineer

Your challenges will demand at least 6 years experience in the design, development and testing of dynamically tuned gyros, with an orientation toward project responsibility. BSME required.

Guided Wave Optics Engineer

Senior position responsible for augmenting optical rate sensor development for a passive Fiber Optic Gyro. Requires solid hands-on development experience in single-mode guided wave optics. Proven leadership, communication, organizational and analytical abilities are a must. MSEE or MS Physics with applied electro-optic orientation required; PhD preferred.

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- Simulation and modeling software written in a generalized simulation language (such as GPSS) to model operation of I/O subsystems.

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Design and develop advanced intelligent caching disk controllers or high speed intelligent tape/disk controllers.

To qualify for these design positions you should have a BSEE and 2 years experience in logic design and/or CMOS gate array design of microprogrammed tape and/or disk controllers. A subsystem architecture background is desirable as is knowledge of high performance mainframe storage systems.

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Join the team who's developing the next generation Data Storage Control Unit. Responsibilities include the architecture, specification, design and development of the entire power system. Experience in linear and switching power supplies, DC power distribution, redundant and battery back-up systems, three phase AC power distribution and protection required. Knowledge in power system packaging and UL/CSA/IEC/FCC requirements also a must.

The ideal candidate should have a BSEE and 9 years experience in power systems design including a minimum of 5 years in tape or disk controller or computer power systems.

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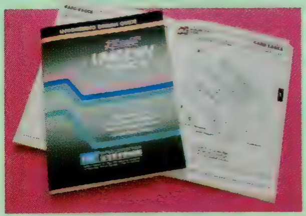

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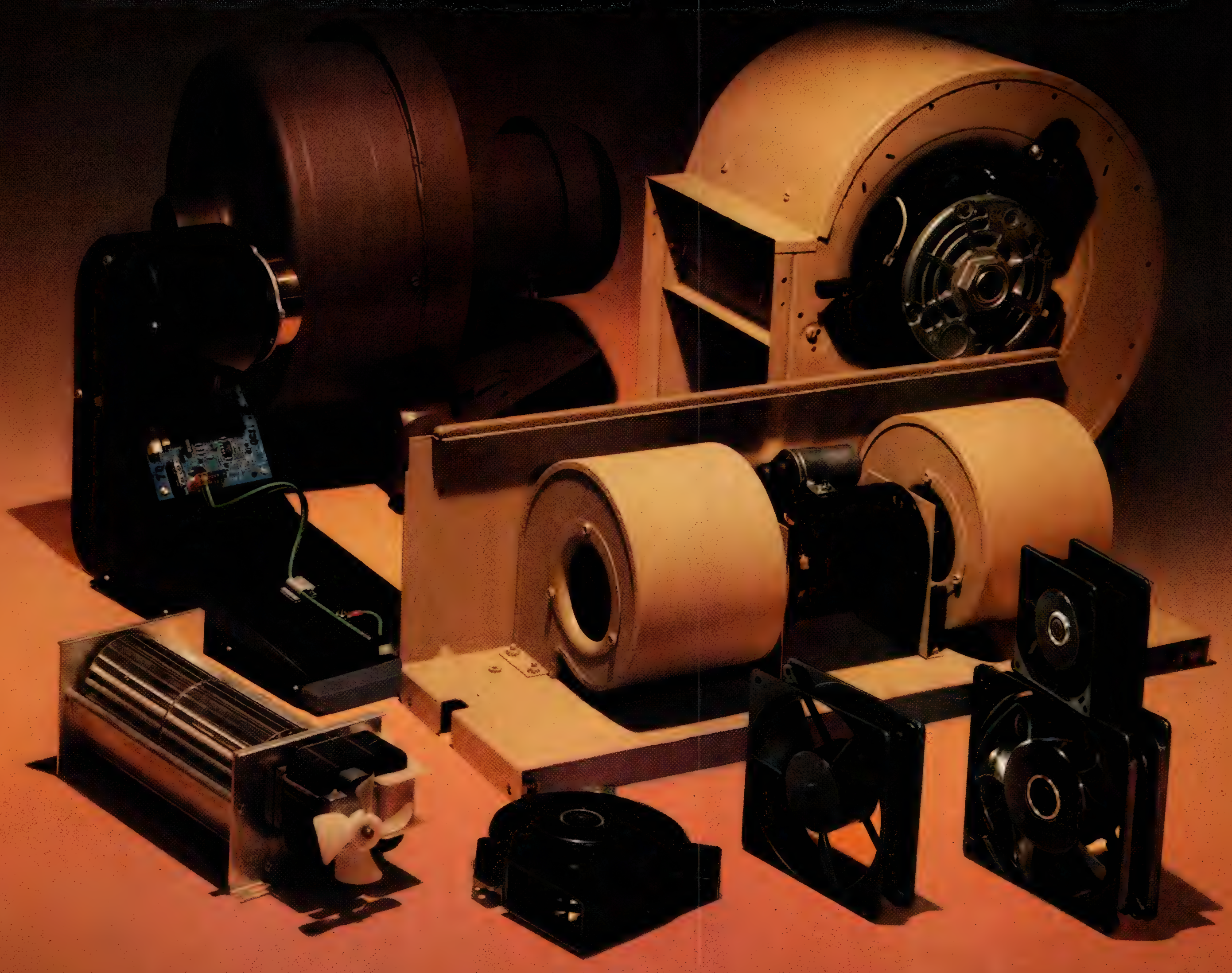

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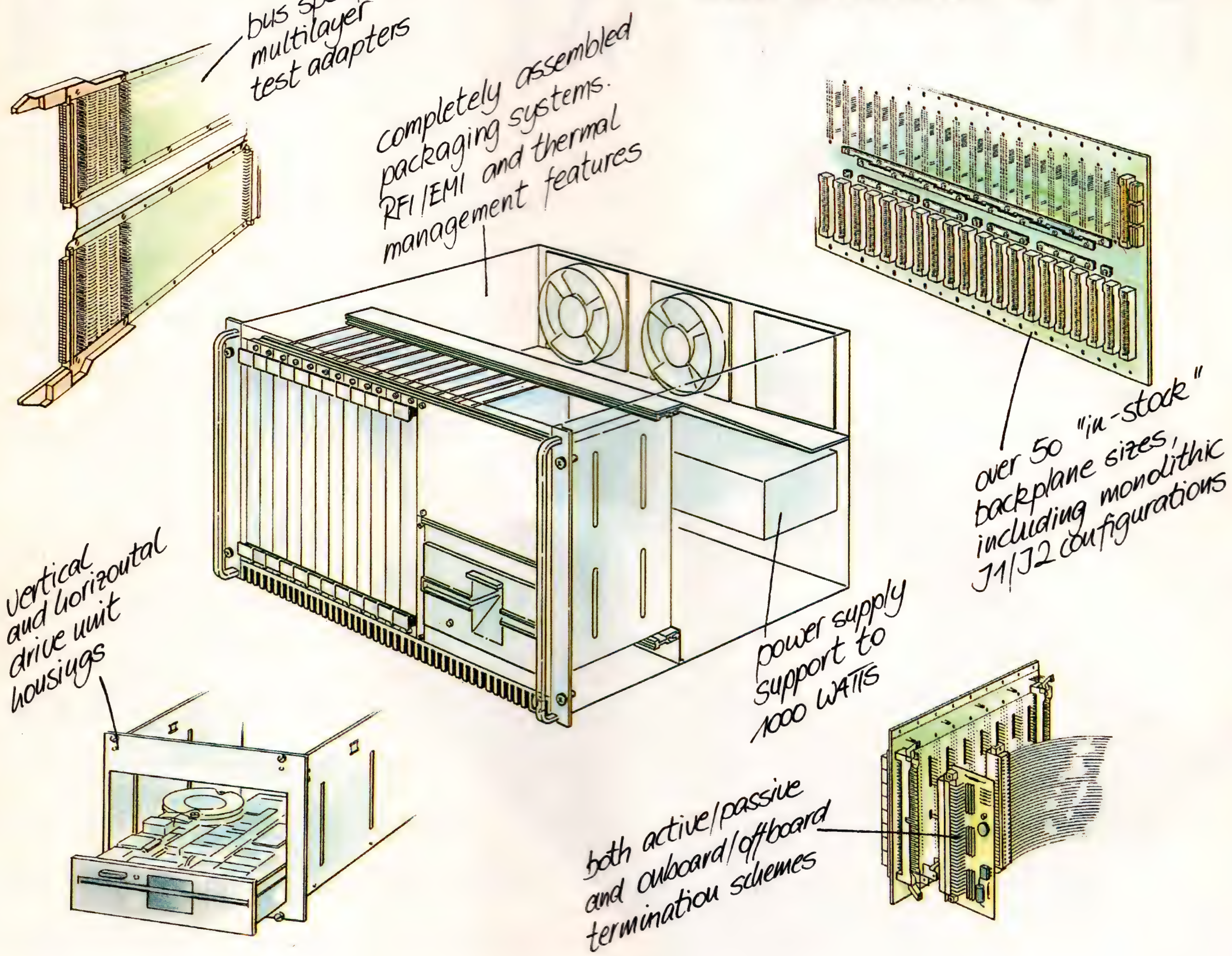

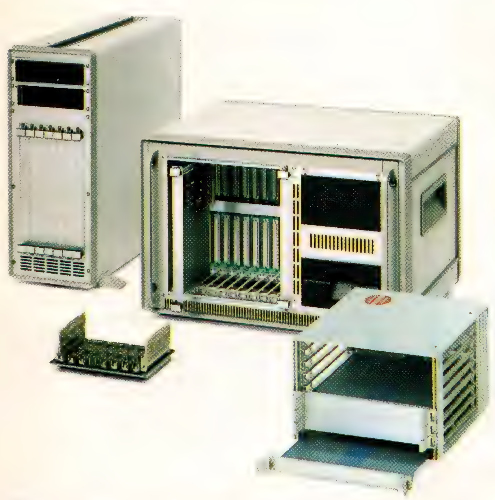

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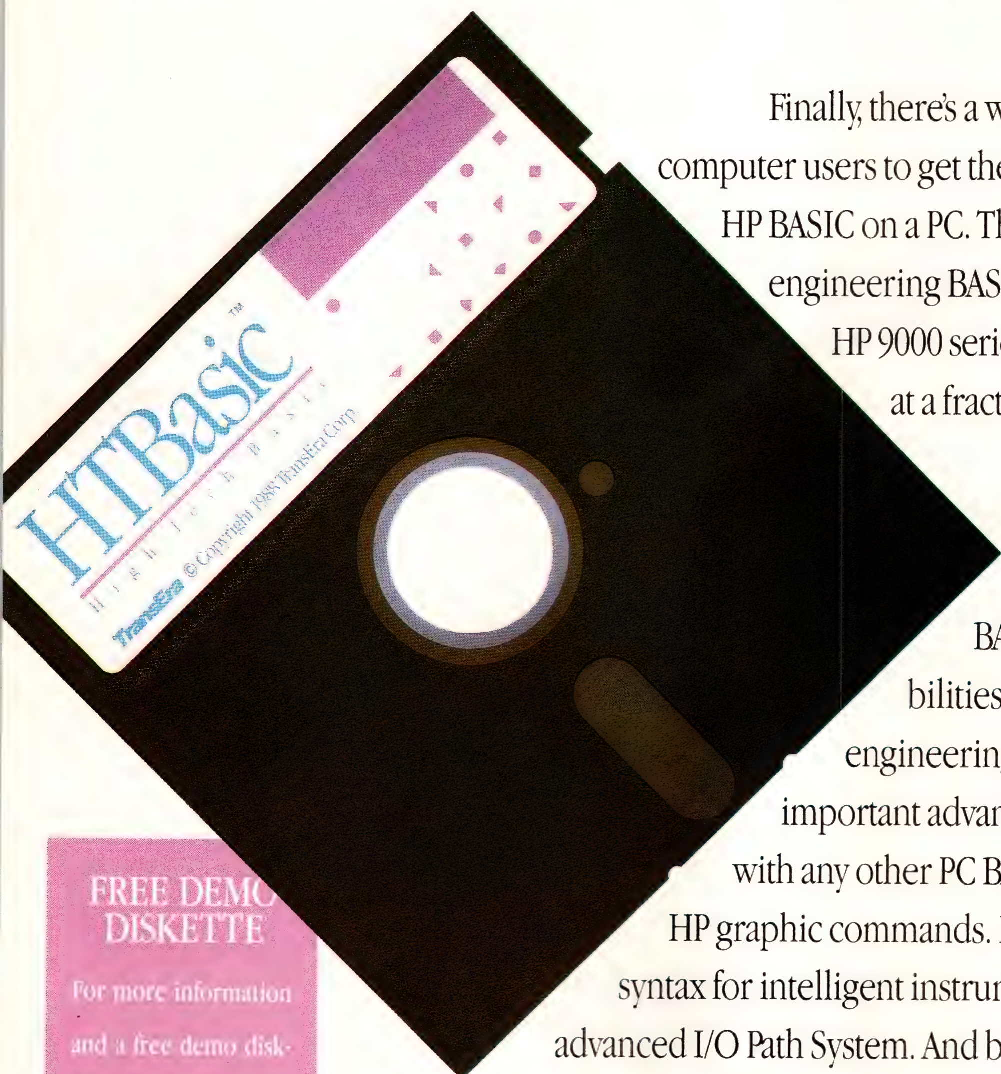

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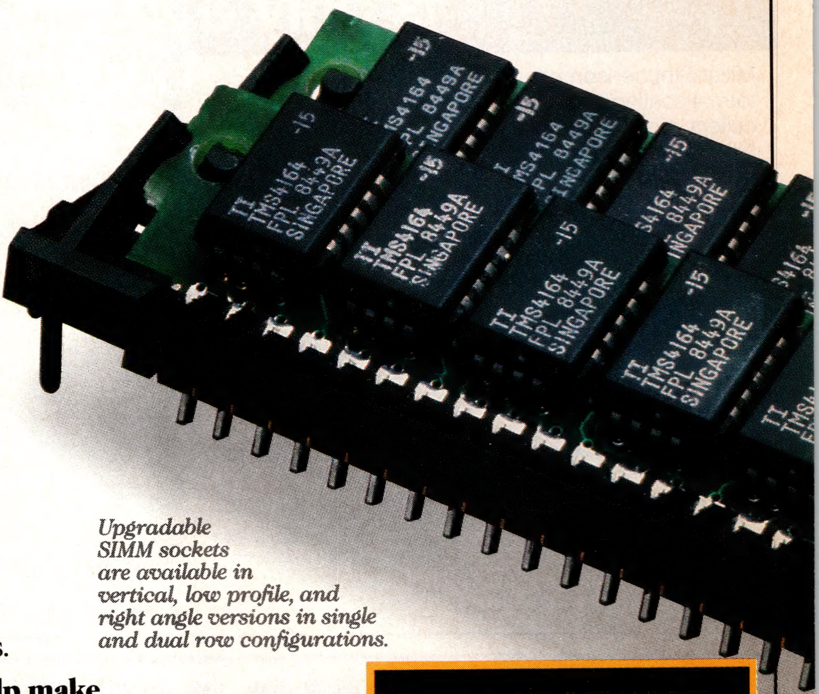

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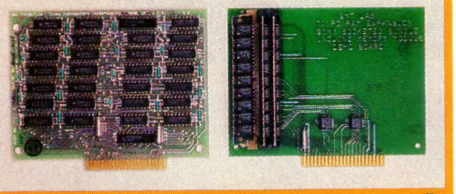
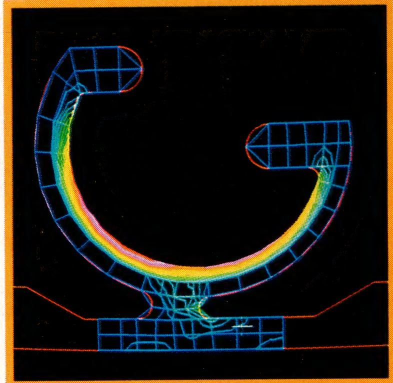


Molex SIMM socket (right) takes up dramatically less board space than DIP packaging (left).



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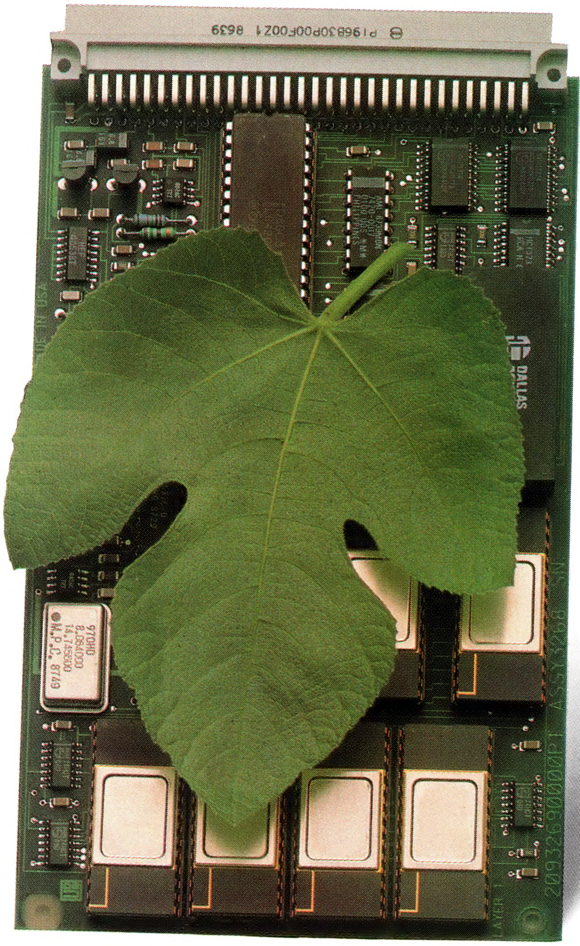

V.32

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While the data pump is functionally identical to the industry standard UDS V.32 modem, it has been stripped of its on-board power supply and DAA. These functions can be easily imported via the board edge connector.

For the bare facts about technical details and quantity pricing, contact Universal Data Systems, 5000 Bradford Drive, Huntsville, AL 35805. Telephone 205/721-8000; Telex 752602 UDS HTV.

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